Site-Controlled SiN/SiO_2 Single Photon Sources Coupled to Silicon Nitride Integrated Photonics

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Abstract: We demonstrate an industrially scalable fabrication process for the integration of SiN/SiO_2 single photon emitters into on-chip nanophotonic structures with sub-diffraction limited placement accuracy.

For photonic quantum information systems and technology (QIST), photons are the basic information-carrying units. One of the major approaches for generating single photons useful for QIST applications is solid-state single-photon sources (SS-SPS), which are mechanically stable, bright, on-demand, and potentially ultra-compact emitters of singlephotons. However, integrating such emitters into nanophotonic structures is generally very challenging from a fabrication point of view [1–4]. One of the major reasons for this challenge is the difficulty of embedding emitters into the nanophotonic structures at a precise location. There have been many approaches explored; however, many of them are either not able to align emitters with sub-diffraction limited accuracy or suffer from low fabrication yields and are not easily scaled to industrial levels. Additionally, many of these approaches require the heterogeneous integration of the emitter hosting materials with materials suitable for low-loss on-chip integrated photonics. Recently, a new type of SS-SPS formed at the interface between silicon nitride (SiN) and silicon oxide (SiO_2) was discovered [5]. These emitters have proven to be bright, stable, and, importantly, native to the SiN/SiO_2 system. This allowed for demonstrations of their monolithic integration with SiN nanophotonic circuitry [6]. However, these demonstrations were done with no control over the position of the emitter within the photonic circuitry [6]. This position uncertainty severely limits the types of structures that can be realized since many photonic structures require sub-diffraction limited placement of the emitter within the structure to function efficiently. For example, Figure 1a shows the structure

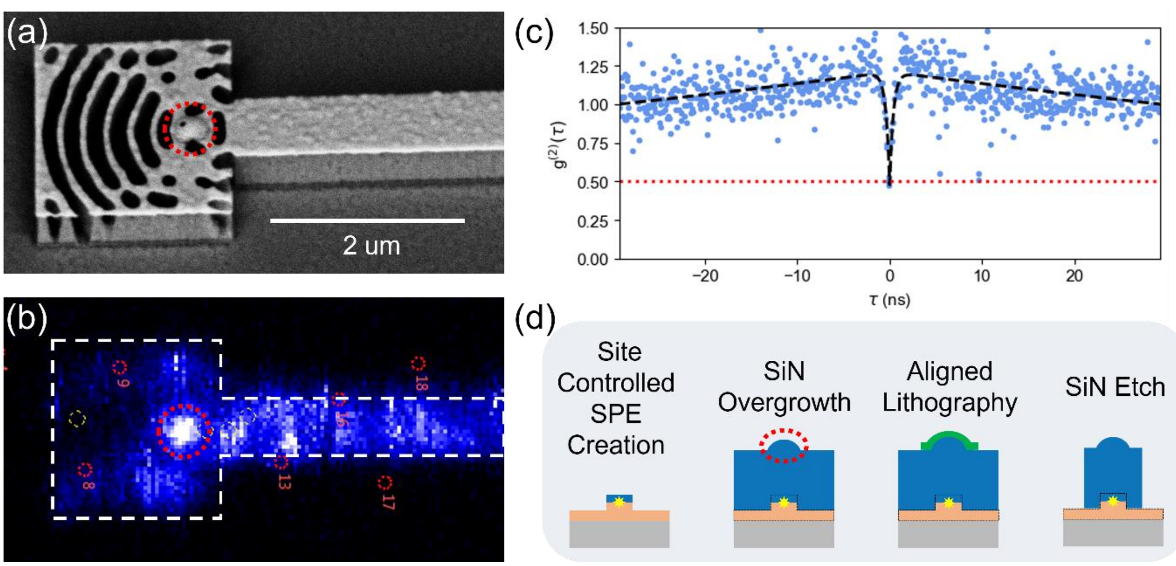

Figure 1 a) A scanning electron microscopy (SEM) image of a demonstration topology optimized (TO) coupler. The red circled bump is where the nanopillar was encapsulated in the SiN that forms the waveguide. b) A photoluminescence map generated with a custom confocal setup of the TO coupler. The red-circled bright spot corresponds to the location of the bump shown in 1a. c) The autocorrelation measurement of the light emitted at the bright spot, excited and collected directly above the spot. d)The fabrication process used to realize SiN/SiO_2 SS-SPS integration with nanophotonic elements.

of a topology-optimized coupler. The performance of this device degrades significantly if the emitter is displaced even 100 nm away from its optimal position [7].

Another recent key discovery is that the emitters can be formed within nanopillars with high yield (67%) and a lateral placement accuracy < ±85 nm by thermally processing them [8]. As this process of forming emitters is lithographically defined, this processing allows for multi-mask lithographic alignment techniques such as the one developed as part of this work for the first time. The overall objective was to align the SS-SPS-containing nanopillars with SiN nanophotonic circuitry. A summary of the fabrication process steps is shown in Figure 1d. The first step shown is preceded by the fabrication and activation of the nanopillar SS-SPSs. The rest of the steps outline the aligned, integration fabrication process used to create the aligned photonic structure around the emitter.

Executing this fabrication process results in structures such as the one shown in Figure 1a, the red circled bump is where the nanopillar was overgrown with the SiN waveguide coupler. Figure 1b) shows the photoluminescence map of the structure from 1a). The PL map shows what was expected: the red-circled pillar position and the bright spot in the PL map are well-aligned and near the design location. This spot is then directly measured using a home-built Hanbury-Brown-Twiss setup using 532 nm continuous laser excitation at room temperature. The measured $g^{(2)}(0)$ value at the bright spot is ~0.5, indicating that the emission is strongly non-classical and mostly likely dominated by one emitter. Particularly considering the relatively strong background, which limits the achievable $g^{(2)}(0)$ dip as background correction is not performed here.

All of this indicates that this is the first process capable of aligning SiN/SiO_2 single photon emitters with complex nanophotonic elements such as the topology-optimized coupler shown. One of the most attractive features of this process is that the nanopillars are relatively large (~170 nm) and, as a result, are compatible with modern industrial wafer-scale photolithography. Additionally, all the other processing steps are standard in the semiconductor fabrication industry. Thus, we believe that the demonstrated fabrication protocol provides an easily industrially scalable approach to the integration of SiN/SiO_2 SS-SPSs with nanophotonic circuitry. Indeed, even in this demonstration work, ~5000 SS-SPS nanophotonic structures were simultaneously fabricated with similar results to those shown here.

Another key element of such processes is the yield. Previous work shows that approximately 67% of these pillars can contain emitters, which is a high yield [8]. Furthermore, the maximum error in the emitter placement is limited by the diameter of the nanopillar, i. e., < ±85 nm [8]. This accuracy is already sufficient for efficient optical integration with many nanophotonic structures. In short, we have developed and demonstrated a fabrication process of integrating SiN/SiO_2 SS-SPSs nanophotonic elements with high-yield and high-placement accuracy at industrial wafer-scales.

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4. References

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