A Heuristic Method to Minimize Switching Actions for Y-Matrix Modulated SC-MMC

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***Abstract*—It is widely recognized that the number of switching turn-on/off actions is proportional to the switching loss. However, Y-Matrix Modulated (YMM) based Modular Multi-level Converter (MMC) has a significantly larger number of switching actions in each fundamental cycle compared to phase shift and level shift modulation methods in order to achieve self-voltage balancing. Given the large amount of switching patterns provided by high level MMCs, the analytical methods make it hard to find the optimal switching scheme. In this paper, a general approach for finding the *N*-level switched capacitor MMC (SC-MMC) optimal switching scheme using Genetic Algorithm (GA) is proposed. The main objective is to propose a heuristic method to minimize the switching actions with self voltage balancing for SC-MMC. Case studies have been implemented on four-level, eleven-level, and fifty-level SC-MMCs. The optimal solution has also been evaluated in terms of the computational complexity, capacitor voltage ripple, and total harmonic distortion (THD) to validate the effectiveness of the proposed method. The simulation results demonstrate the computational efficiency of the proposed algorithm in comparison to the analytical method. Moreover, the proposed algorithm can achieve a substantial 22% reduction in switching actions compared to the original switching pattern.**

Keywords—Modular multi-level converter, Y-matrix modulation, Genetic Algorithm

I. Introduction

Switched Capacitor Modular Multi-level Converter (SC-MMC) has shown promising advantage over the conventional MMC in terms of self-voltage balancing and passive component reduction [1]. However, to secure a self-voltage balancing, the SC-MMC needs to be operated at high switching frequency (a few tens kilohertz), which leads to a significant increase of switching loss compared to conventional MMCs that are operated at fundamental frequency. It is widely recognized that the switching losses of a converter is proportional to the number of switching turn-on/-off events of the converter.

Conventional methods of reducing switching events rely on evaluating the low frequency components of the current and calculating the voltage ripple of the capacitor [2]. This method is generally valid for conventional MMC with a relatively large arm inductor that can filter out the switching-frequency harmonics. However, for Y matrix modulated SC-MMC [3] or other switching-cycle based MMC [4], the switching loss reduction greatly depends on the simulation results due to the rich switching-frequency harmonics in the arm inductor currents. Because of the challenges in modeling the high frequency harmonics in arm inductors, no analytical methods, to the best of our knowledge, have been developed for the switching actions reduction of switching-cycle based SC-MMC.

To address this issue, a reduced switching-frequency voltage balance algorithm has been proposed in [5]. However, it does not account for potential deviations in the submodule (SM) voltage that may occur during each control period. Although reduced switching frequency (RSF) voltage balancing algorithm has also been introduced in [6], [7], and [8], there is still room for improvement in reducing capacitor ripple. In order to reduce the power loss of YMM based SC-MMC while ensuring capacitor voltage balancing, one needs to carefully select the Y matrix of the SC-MMC so that the minimal switching events can be achieved.

However, conventional analytic methods may not be applicable to high-level SC-MMCs. In [9], an analytical approach has been proposed for identifying the optimal switching strategy with the goal of minimizing switching frequency. While this method ensures voltage balancing under specified constraints, it is noted for its time-consuming nature. MMCs, especially high-level MMCs widely used in HVDC systems, have an astronomical number of switching states. For instance, a 100-level MMC may have approximately 2.5×10^{57} feasible switching states to generate an output voltage at level 50. In high-voltage DC (HVDC) transmission applications, MMCs are typically constructed with 200 to 400 levels [10]. As the MMC level increases, the number of feasible switching states expands exponentially, making it nearly impossible for analytical methods to determine the optimal switching patterns.

To overcome the limit of the analytical methods in processing the large pool of feasible switching patterns of high-level SC-MMCs, this paper proposes a heuristic method with self voltage balancing to minimize the switching actions for SC-MMC. The simulation results show the proposed algorithm can reduce 22% switching actions compared to the original switching pattern [1].

The rest of the paper is organized as follows: Section II introduces the basic principle of a four-level SC-MMC and then expand to *N*-level SC-MMC. The Y matrix modulation technique has also been introduced in this section. Section III formulates SC-MMC optimal switching scheme using GA. Section IV presents the case studies results for four-level, eleven-level, and fifty-level SC-MMCs in terms of the computational complexity, capacitor voltage ripple, and THD values. The conclusion of this paper is summarized in Section V.

II. YMM-Based N-Level SC-MMC Capacitor Voltage Balacing

A. Basic principle of MMC

Fig. 1 shows the topology of a three-phase SC-MMC [1]. The MMC normally converts the DC system to three-phase AC system, and feeds an ac load. In the MMC, the three-phase AC system connects to the mid-point of each leg (v_a, v_b, v_c). Each leg of the MMC is divided into the upper arms and lower arms. The upper arms connect to the positive rail, and the lower arms connect to the negative rail. Each arm contains a series of SMs and an inductor (L). The arm inductor, connected in series with the SMs, serves to limit the current resulting from the instantaneous voltage difference between the SMs and the DC system.

For a N=4-level SC-MMC, there are N-1=3, and only three, out of 2N-2=6 SMs at inserting mode at any instant. The other three SMs are at by-pass mode meanwhile. The pole voltage v_a of a four-level MMC can either be $3V_{dc}$, V_{dc}, or $-V_{dc}$, $3V_{dc}$, if all capacitor voltages are V_{dc}. If the voltage drop on arm inductors could be neglected, the sum of the voltages of the three inserting-mode SMs are clamped to the dc source voltage.

For a four-level SC-MMC, there is a total of $C_6^3 = 20$ possible states when there are half SMs at inserting mode. The capacitor voltage of six possible states can be formulated as:

$$\begin{cases} 3V_{dc}=V_{C4}+V_{C5}+V_{C6} \\ 3V_{dc}=V_{C1}+V_{C4}+V_{C5} \\ 3V_{dc}=V_{C2}+V_{C4}+V_{C5} \\ 3V_{dc}=V_{C3}+V_{C4}+V_{C5} \\ 3V_{dc}=V_{C1}+V_{C4}+V_{C6} \\ 3V_{dc}=V_{C2}+V_{C4}+V_{C6} \\ 3V_{dc}=V_{C3}+V_{C4}+V_{C6} \\ 3V_{dc}=V_{C1}+V_{C5}+V_{C6} \\ 3V_{dc}=V_{C2}+V_{C5}+V_{C6} \\ 3V_{dc}=V_{C3}+V_{C5}+V_{C6} \end{cases} , \begin{cases} 3V_{dc}=V_{C1}+V_{C2}+V_{C4} \\ 3V_{dc}=V_{C1}+V_{C2}+V_{C5} \\ 3V_{dc}=V_{C1}+V_{C2}+V_{C6} \\ 3V_{dc}=V_{C1}+V_{C3}+V_{C4} \\ 3V_{dc}=V_{C1}+V_{C3}+V_{C5} \\ 3V_{dc}=V_{C1}+V_{C3}+V_{C6} \\ 3V_{dc}=V_{C2}+V_{C3}+V_{C4} \\ 3V_{dc}=V_{C2}+V_{C3}+V_{C5} \\ 3V_{dc}=V_{C2}+V_{C3}+V_{C6} \\ 3V_{dc}=V_{C1}+V_{C2}+V_{C3} \end{cases} . \quad (1)$$

The 20 possible states of (1) can be re-written into matrix form below:

$$\begin{bmatrix} 3V_{dc} \\ \vdots \\ 3V_{dc} \end{bmatrix}_{20\times1} = \mathbf{Y}^{(4)} \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \\ V_{C6} \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_1^{(4)} \\ \hline \mathbf{Y}_2^{(4)} \\ \hline \mathbf{Y}_3^{(4)} \\ \hline \mathbf{Y}_4^{(4)} \end{bmatrix}_{20\times6} \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \\ V_{C6} \end{bmatrix}_{6\times1} , \quad (2)$$

where $\mathbf{Y}_1^{(4)}$ and $\mathbf{Y}_4^{(4)}$ are 1-by-6 matrices, $\mathbf{Y}_2^{(4)}$ and $\mathbf{Y}_3^{(4)}$ are 9-by 6 matrices with a rank of 5. The switching patterns of every SM in a single phase leg are provided by the **Y** matrix, where 1 denotes the inserting and 0 denotes the bypass mode. The number of inserted SMs in each phase leg is always (N-1) since the total of all the items in each row of the **Y** matrix equals (N-1). The 4 submatrices can be expressed as the following matrix form:

$$\mathbf{Y}_1^{(4)} = [0 \quad 0 \quad 0 \quad 1 \quad 1 \quad 1] , \ \mathbf{Y}_4^{(4)} = [1 \quad 1 \quad 1 \quad 0 \quad 0 \quad 0] ,$$

$$\mathbf{Y}_2^{(4)} = \begin{bmatrix} 1&0&0&1&1&0 \\ 0&1&0&1&1&0 \\ 0&0&1&1&1&0 \\ 1&0&0&1&0&1 \\ 0&1&0&1&0&1 \\ 0&0&1&1&0&1 \\ 1&0&0&0&1&1 \\ 0&1&0&0&1&1 \\ 0&0&1&0&1&1 \end{bmatrix} , \ \mathbf{Y}_3^{(4)} = \begin{bmatrix} 1&1&0&1&0&0 \\ 1&1&0&0&1&0 \\ 1&1&0&0&0&1 \\ 1&0&1&1&0&0 \\ 1&0&1&0&1&0 \\ 1&0&1&0&0&1 \\ 0&1&1&1&0&0 \\ 0&1&1&0&1&0 \\ 0&1&1&0&0&1 \end{bmatrix} . \quad (3)$$

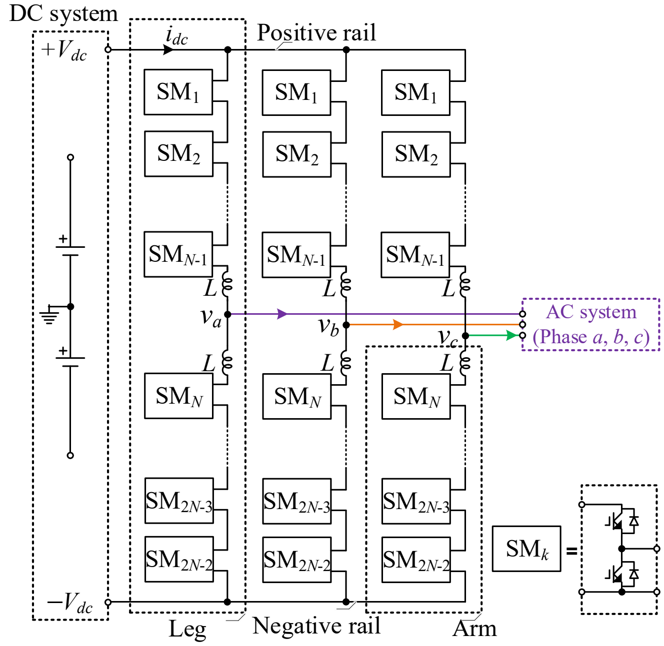

Fig. 1. The topology of a three-phase SC-MMC [1].

The rank of each two adjacent matrices is 6. Therefore, to reduce the number of switching events, $\mathbf{Y}_2^{(4)}$ and $\mathbf{Y}_3^{(4)}$ should be able to extract the 5-by-6 core submatrices which hold the same rank 5. Extract 5 rows from $\mathbf{Y}_2^{(4)}$ and $\mathbf{Y}_3^{(4)}$ to maintain the full rank condition, we can obtain:

$$\hat{\mathbf{Y}}_2^{(4)} = \begin{bmatrix} 0&0&1&0&1&1 \\ 0&1&0&0&1&1 \\ 0&0&1&1&0&1 \\ 1&0&0&1&0&1 \\ 0&1&0&1&1&0 \end{bmatrix} , \ \hat{\mathbf{Y}}_3^{(4)} = \begin{bmatrix} 1&0&1&0&1&0 \\ 1&1&0&0&1&0 \\ 1&0&1&1&0&0 \\ 1&0&1&0&0&1 \\ 0&1&1&0&1&0 \end{bmatrix} . \quad (4)$$

If **Y** matrix is in full rank, Y is linearly independent, the capacitor voltage has no more than one solution. When any of two adjacent levels are in full rank, the unique solution for $\boldsymbol{V_C}$ is:

$$\begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \\ V_{C6} \end{bmatrix} = \begin{bmatrix} V_{dc} \\ V_{dc} \\ V_{dc} \\ V_{dc} \\ V_{dc} \\ V_{dc} \end{bmatrix} \quad (5)$$

Therefore, the capacitor voltages in the four-level MMC are naturally balanced.

B. N-level SC-MMC

Fig. 2 shows a signle-phase N-level SC-MMC with different pole voltage for 1st level, 2nd level, and Nth level [11]. For each level, there are N – 1, and only N – 1, out of 2N – 2 SMs at inserting mode at a time. The other N – 1 SMs are at bypass mode meanwhile.

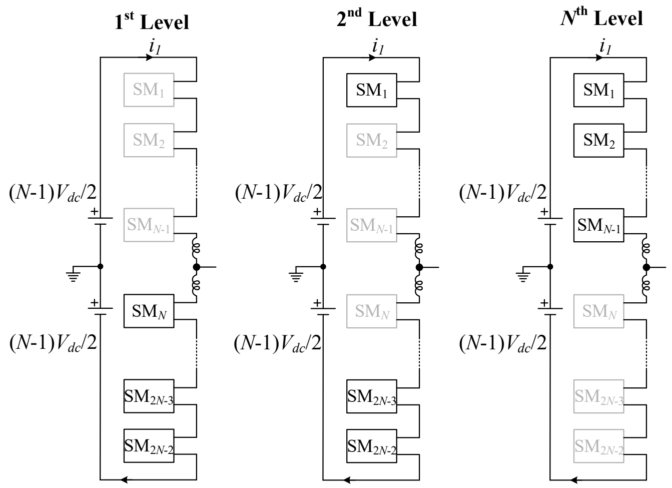

Fig. 2. N-level SC-MMC with pole voltage of (a) (N – 1) V_{dc} (Level 1); (b) (N – 3) V_{dc} (Level 2); and (c) – (N – 1) V_{dc} (Level N) [11].

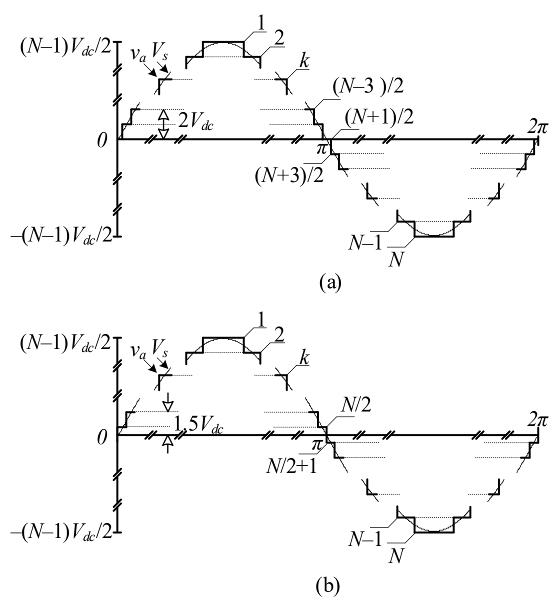

Fig. 3 Numbering of levels in an N-level MMC, when (a) N is an odd number; and (b) N is an even number [11].

There are N levels for pole voltage v_a. Assume that all capacitor voltages are V_{dc}. The pole voltage v_a of an N-level MMC is an element of { $(N–1)V_{dc}/2$, $(N–3)V_{dc}/2$, $(N–5)V_{dc}/2$, …, V_{dc}, 0, $–V_{dc}$,…, $–(N–3)V_{dc}/2$, $–(N–1)V_{dc}/2$}, if N is an odd number. The pole voltage v_a of an N-level MMC is an element of {$(N–1)V_{dc}/2$, $(N–3)V_{dc}/2$, $(N–5)V_{dc}/2$, …, $V_{dc}/2$, $–V_{dc}/2$,…, $–(N–3)V_{dc}/2$, $–(N–1)V_{dc}/2$}, if N is an even number. Fig. 3 [1] shows the numbering of levels in an N-level MMC, starting from the first level to the Nth level when N is an odd and even number. It is noted that the pole voltage v_a can be zero when N is an odd number.

The Y matrix contains N submatrices, starting from $\mathbf{Y}_1$ to $\mathbf{Y}_N$. All capacitor voltage balancing could be formulated as:

$$\begin{bmatrix} (N-1)V_{dc} \\ \vdots \\ (N-1)V_{dc} \end{bmatrix}_{(m_1+m_2+\cdots+m_N)\times 1} = \begin{bmatrix} (\mathbf{Y}_1)_{m_1\times(2N-2)} \\ (\mathbf{Y}_2)_{m_2\times(2N-2)} \\ \vdots \\ (\mathbf{Y}_k)_{m_k\times(2N-2)} \\ \vdots \\ (\mathbf{Y}_N)_{m_N\times(2N-2)} \end{bmatrix} \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ \vdots \\ V_{C(2N-2)} \end{bmatrix}_{(2N-2)\times 1} \quad (6)$$

where $m_k = C_{N-1}^{k-1} C_{N-1}^{N-k} = \left(C_{N-1}^{k-1}\right)^2$, $1 < k < N$.

C. Y Matrix Modulated SC-MMC

One equation in (6) is satisfied at a time when MMC visits one SM pattern. MMC is considered to have completed one iteration when it has visited every SM pattern in the **Y**. The voltages of MMC capacitors should converge after a number of iterations. This chapter focuses on developing an effective modulation, namely Y-Matrix Modulation (YMM) [11] and [12], to realize the self voltage balancing feature for MMC.

The N-level MMC modulation can also be explained in Fig. 4 [1]. For example, when the pole voltage v_a at first level, the level pointer pointes to level 1, $\mathbf{Y}_1^{(N)}$ is chosen as the sub-module pattern to implement this first-level pole-voltage. Similarly, When the pole voltage v_a at kth level, where $2 \le k \le N – 1$, the level pointer pointes to level k, $\mathbf{Y}_k^{(N)}$ is chosen as the sub-module patterns to implement this kth level pole voltage. The rank of $\mathbf{Y}_k^{(N)}$ is $2N–3$, which means $\mathbf{Y}_k^{(N)}$ only has $2N – 3$ linearly independent rows. To reduce the number of switching events, $\mathbf{Y}_k^{(N)}$ should be able to extract the core submatrix $\hat{\mathbf{Y}}_k^{(N)}$ while maintaining the same rank.

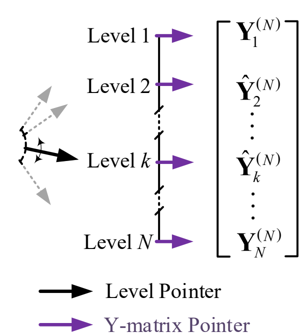

Fig. 4 **Y**-matrix modulation strategy for N-level MMC [11].

The procedure of YMM for N-level MMC can also be summarized as below:

(1) Determine the level of v_a by level shifted modulation (LSM);

(2) Assign the level number to the level pointer at every switching cycle;

(3) Locate the Y-matrix pointer that the level pointer pointes to;

(4) Read the row (SM pattern) which the Y matrix pointer points to;

(5) Generate the gating signal for each SM that corresponds with the SM pattern;

(6) Reassign the Y-matrix pointer to the next row and wait for the next call from level pointer.

III. *N*-Level SC-MMC Optimal Switching Scheme Via GA

As the SC-MMC level increases, **Y** matrix expands rapidly. The analytical methods make it hard to find the optimal switching scheme. Genetic Algorithm (GA) [13] is a heuristic optimization algorithm inspired by the principles of natural selection and genetics. It is used to find optimal solutions to complex problems by simulating the process of natural evolution. GA is well-suited for optimizing MMC switching scheme because of the ability to efficiently search large, complex spaces for optimal solutions. GAs mimic natural evolutionary processes such as selection, crossover, and mutation to evolve solutions towards greater fitness, which in the case of MMCs would involve optimizing the switching to minimize switching losses and ensure voltage balance. The benefits of using GAs for this purpose include the capability to handle the complex and large-scale optimization problems typical in high-level MMCs without exhaustive searching. This approach is particularly advantageous when the search space is vast and not easily navigable by traditional analytical methods.

GA evolves towards finding the optimal value through a series of iterative processes, each designed to mimic natural evolutionary mechanisms [14]. The process begins with a randomly generated population of potential solutions, known as individuals. Each individual represents a possible switching scheme for the MMC and is evaluated using a fitness function that measures its performance based on criteria such as minimizing switching losses and ensuring voltage balance.

The evolution process in GA involves several key steps [15]:

(1) **Selection:** Individuals are selected based on their fitness scores, with higher fitness individuals having a greater chance of being chosen. This mimics natural selection where the fittest individuals are more likely to reproduce and pass on their genes.

(2) **Crossover**: Selected individuals are paired, and parts of their solution representations (genes) are exchanged to create new offspring. This process introduces new combinations of genes, potentially leading to better solutions.

(3) **Mutation:** To maintain genetic diversity within the population and to avoid local optima, some genes in the offspring are randomly altered. This mutation step ensures that the algorithm explores a wider search space.

(4) **Replacement:** The new generation of individuals (offspring) replaces the old generation. The process of selection, crossover, and mutation is repeated over many generations, with each generation ideally having individuals that are more fit than the previous one.

Through these iterative processes, the population of potential solutions evolves over time, converging towards an optimal or near-optimal switching scheme for the MMC. This evolutionary approach allows GA to efficiently navigate large and complex search spaces, making it a powerful tool for solving optimization problems that are intractable for traditional analytical methods.

Define the objective function as the minimum number of switching actions denoted by N_{sw} during one switching cycle T_c. For each submodule, if the switching state changes, then one switching event occurs. Consider one phase of the SC-MMC which has 2*N*-2 SMs, then the objective function can be written as:

$$obj = \min N_{sw} = \sum_{\alpha=0}^{T_C/T_{switching}} \sum_{\beta=1}^{2N-2} \left| s_{\alpha+1,\beta} - s_{\alpha,\beta} \right|, \tag{7}$$

$$\text{s.t. } rank[\mathbf{Y}_k \quad \mathbf{Y}_{k+1}] = 2N-2 , \tag{8}$$

where $s_{\alpha,\beta}$ represent the switching state of β^{th} SM in the α^{th} control period. $T_{switching}$ is the switching period.

Since $\mathbf{Y}_1^{(N)}$ and $\mathbf{Y}_N^{(N)}$ are 1-by-(2*N* – 2) matrices. There is no need to extract submatrices from these two. Therefore, we only need to find the remaining (*N*-2) levels' submatrices $\mathbf{Y}_k^{(N)}$. The dimension for the (*N*-2) levels' submatrices $\mathbf{Y}_k^{(N)}$ is m_k-by-(2*N*-2). Since the rank for each submatrix $\mathbf{Y}_k^{(N)}$ is (2*N*-3), to make sure each submatrix $\mathbf{Y}_k^{(N)}$ is in full rank and reduce the number of switching events, we only need to find the core matrix $\hat{\mathbf{Y}}_k^{(N)}$, which dimension is (2*N*-3)-by-(2*N*-2).

In order to find the core matrix $\hat{\mathbf{Y}}_k^{(N)}$, we have to extract (2*N*-3) rows from submatrix $\mathbf{Y}_k^{(N)}$. Since we only need to find the core matrices for the remaining (*N*-2) levels. The decision variable $\boldsymbol{x}$ is thus defined as the row indicator, which is a (*N*-2)-by-(2*N*-3) matrix shown in (9). $x_{k,j}$ is the j^{th} indicator for k^{th} level. There are (2*N*-3) decision variables for each k^{th} level submatrix $\mathbf{Y}_k^{(N)}$. The upper bound for the decision variable $x_{k,j}$ for each submatrix $\mathbf{Y}_k^{(N)}$ is $m_k = (C_{N-1}^{k-1})^2$. Since we have to determine the remaining (*N*-2) levels' core submatrices $\hat{\mathbf{Y}}_k^{(N)}$ from 2nd level to (*N*-1)th level. There are a total of (*N*-2) × (2*N*-3) decision variables. To secure the self voltage balancing for *N*-level SC-MMC, the rank for each core matrix $\hat{\mathbf{Y}}_k^{(N)}$ after selection should be (2*N*-3), and any two adjacent submatrices $[\hat{\mathbf{Y}}_k^{(N)} \quad \hat{\mathbf{Y}}_{k+1}^{(N)}]$ should be in full rank (2*N*-2).

$$\boldsymbol{x} = \begin{bmatrix} x_{2,1} & \cdots & x_{2,j} & \cdots & x_{2,2N-3} \\ \vdots & & \ddots & & \vdots \\ x_{k,1} & \cdots & x_{k,j} & \cdots & x_{k,2N-3} \\ \vdots & & \ddots & & \vdots \\ x_{N-1,1} & \cdots & x_{N-1,j} & \cdots & x_{N-1,2N-3} \end{bmatrix} \begin{matrix} \rightarrow 2^{nd} \text{ level} \\ \\ \rightarrow k^{th} \text{ level} \\ \\ \rightarrow (N-1)^{th} \text{ level} \end{matrix} \tag{9}$$

where $2 \le k \le N-1,\ 1 \le j \le 2N-3$.

Fig. 5 is an example to show the k^{th} level decision variable $\boldsymbol{x}_k$ vector, which consists of (2*N*-3) decision variables. For the k^{th} level submatrix $\mathbf{Y}_k^{(N)}$ which dimension is a m_k-by-(2*N*-2). GA helps randomly select (2*N*-3) rows and assign the row number to $x_{k,j}$. The value of $x_{k,j}$ should not exceed m_k. The rank for each core matrix $\hat{\mathbf{Y}}_k^{(N)}$ after selection should be (2*N*-3).

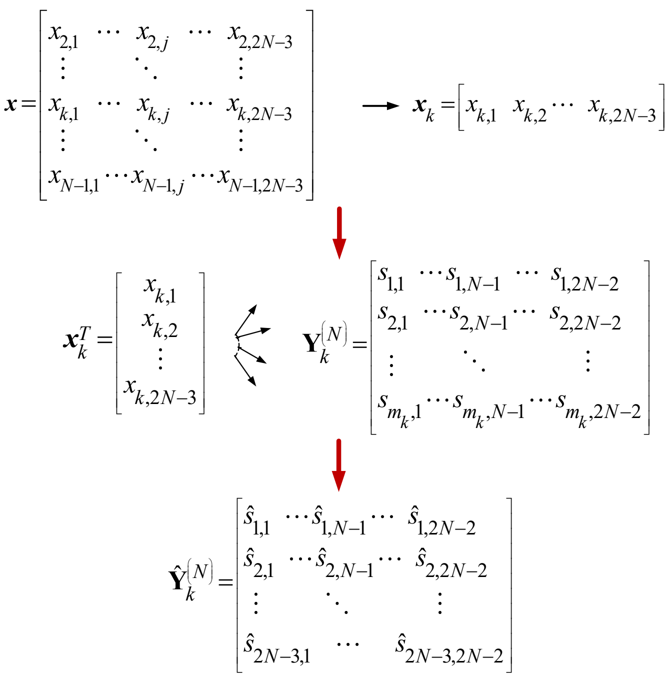

Fig. 5 The k^{th} level core matrix selection process.

where *s* is the switching state, '0' represents switching off, and '1' represents switching on.

Take the 4-level MMC as an example, for the 1st and last 4th level, there are only one row for these two submatrices. For the 2nd and 3rd level, where $m_2 = m_3 = (c_3^1)^2 = 9$. The dimension of $\mathbf{Y}_2^{(4)}$ and $\mathbf{Y}_3^{(4)}$ shown in (3) is m_k-by-(2*N*-2) which equals to 9×6. When *N*=4, the decision variable $\boldsymbol{x}$ is a 2×5 matrix. Following is an example to show how GA find the core submatrix $\hat{\mathbf{Y}}_2^{(4)}$. When *k*=2, $\boldsymbol{x}_2^T$ is a 5×1 matrix. Once GA randomly determined the initial row indicator to $\boldsymbol{x}_2^T$ such as shown in (10), then take the row from $\mathbf{Y}_2^{(4)}$ according to each element in $\boldsymbol{x}_2^T$, the core submatrix $\hat{\mathbf{Y}}_2^{(4)}$ can be selected as (11). Each element in $\boldsymbol{x}$ should not exceed the total row number of submatrix $\mathbf{Y}_2^{(4)}$ which is m_2=9. The assigned value to $\boldsymbol{x}_2^T$ should make $\hat{\mathbf{Y}}_2^{(4)}$ to full rank, which is 2*N*-3=5.

$$\boldsymbol{x}_2^T = \begin{bmatrix} 9 \\ 8 \\ 6 \\ 4 \\ 2 \end{bmatrix} \rightarrow \mathbf{Y}_2^{(4)} = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \tag{10}$$

$$\hat{\mathbf{Y}}_2^{(4)} = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 \end{bmatrix} \tag{11}$$

When *k*=3, $\boldsymbol{x}_3^T$ is a 5×1 matrix. Once GA randomly determined the initial row indicator to $\boldsymbol{x}_3^T$ such as shown in (12), then take the row from $\mathbf{Y}_3^{(4)}$ according to each element in $\boldsymbol{x}_3^T$, the core matrix $\hat{\mathbf{Y}}_3^{(4)}$ can be selected as (13). Each element in x should not exceed the total row number of submatrix $\mathbf{Y}_3^{(4)}$ which is m_3=9. The assigned value to $\boldsymbol{x}_3^T$ should make $\hat{\mathbf{Y}}_3^{(4)}$ to full rank, which is 2*N*-3=5.

$$\boldsymbol{x}_3^T = \begin{bmatrix} 1 \\ 2 \\ 3 \\ 5 \\ 7 \end{bmatrix} \rightarrow \mathbf{Y}_3^{(4)} = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix} \tag{12}$$

$$\hat{\mathbf{Y}}_3^{(4)} = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 \end{bmatrix} \tag{13}$$

Then $\boldsymbol{x}$ can be formulates as a 2×5 matrix, which is given in (14). The core submatrices from the 2nd level to (*N*-1)th=3rd level are thus selected. Then the algorithm goes to GA iteration to calculate the number of switching events according to objective function (7).

$$\boldsymbol{x} = \begin{bmatrix} 9 & 8 & 6 & 4 & 2 \\ 1 & 2 & 3 & 5 & 7 \end{bmatrix} \tag{14}$$

The corresponding steps of YMM-based *N*-level MMC using GA are as follows:

Step 1: Initialize (*N*-2) × (2*N*-3) decision variables $\boldsymbol{x}$ matrix, the value of $x_{k,j}$ should not exceed m_k.

Step 2: Select (2*N*-3) rows from each submatrix $\mathbf{Y}_k^{(N)}$ in a random manner, and make sure it is in full rank. If it is not in full rank, back to initialization.

Step 3: Start GA iteration, and run the YMM based SC-MMC simulation, calculate the objective function for each level according to (7).

Step 4: Update decision variables for the entire (*N*-2) × (2*N*-3) matrix, then return to Step 3 and recalculate the fitness value according to (7) until reaches the maximum generations.

Step 5: Save the optimal switching pattern results for each submatrix.

The corresponding steps of YMM-based N-level MMC using GA can also be explained with the aid of Fig. 6.

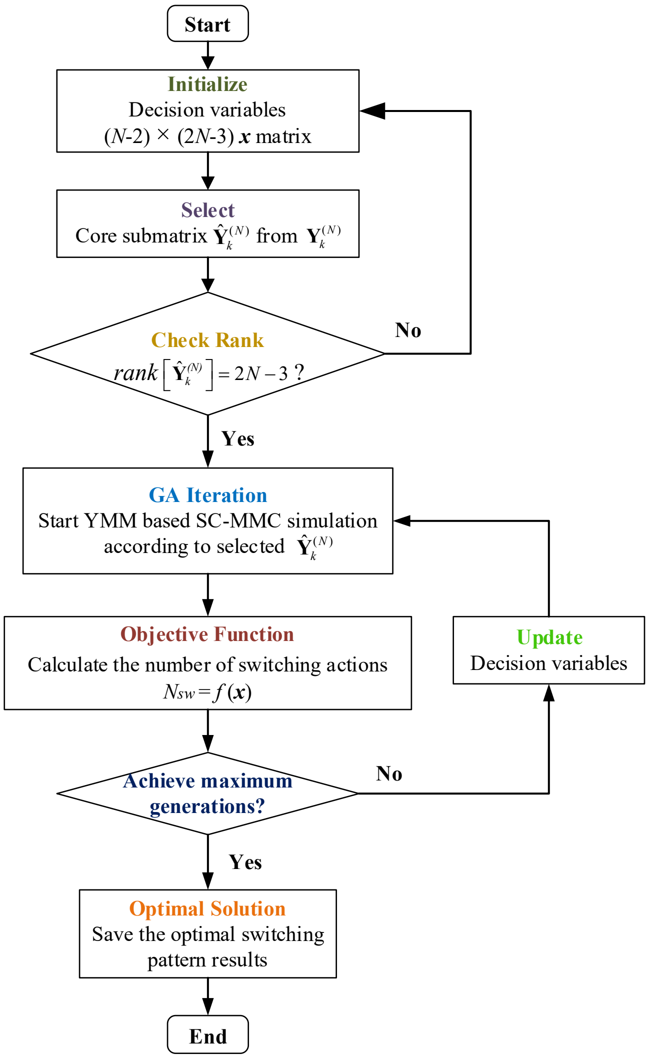

Fig. 6. The flow chart of the optimization algorithm.

IV. Case Studies

A. YMM Based Four-Level SC-MMC

The simulation was conducted in Matlab/Simulink. There are 6 SMs in each phase for this 4-level SC-MMC. The switching frequency is 30 kHz. The key parameters are summarized in Table I [1]. After 500 iterations, the minimum number of switching actions during one cycle is 2044. Compared to the original switching pattern [1] which has 2527 switching actions, the optimal switching scheme can lead to a reduction of 23.63%. All **Y** submatrices are in full rank. The optimization algorithm was completed in 0.84 hours. However, by using the analytical method, there are 6561 full-rank combinations. Among them, there are 14400 permutations in each combination, which takes 122.95 h to find the optimal solution.

The optimal Y submatrices are as follows:

$$\mathbf{Y}_1^{(4)} = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix},\ \mathbf{Y}_4^{(4)} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 \end{bmatrix}$$

$$\hat{\mathbf{Y}}_2^{(4)} = \begin{bmatrix} 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix},\ \hat{\mathbf{Y}}_3^{(4)} = \begin{bmatrix} 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix}, \quad (15)$$

TABLE I
FOUR-LEVEL MMC SIMULATION KEY PARAMETERS

Apparent Power, S	150 kVA
Fundamental Frequency, f_0	60 Hz
Switching Frequency, f_{sw}	30 kHz
DC-Bus Voltage, V_{dc}	1000 V
Phase Voltage, V_a, V_b, V_c	964 V
Line Current, I_a, I_b, I_c	52 A
Load Resistance, R_{load}	18.6 Ω
Line Inductance, L_{line}	1 mH
Arm Inductance, L_{arm}	0.1 μH
Submodule Capacitance, C_i	171 μF
Number of Submodules per Arm	3

where i = 1, 2, …, 18.

The load phase voltage and load line current are shown in Fig. 7. The total harmonic distortion (THD) is 1.99% for load phase voltage and line current.

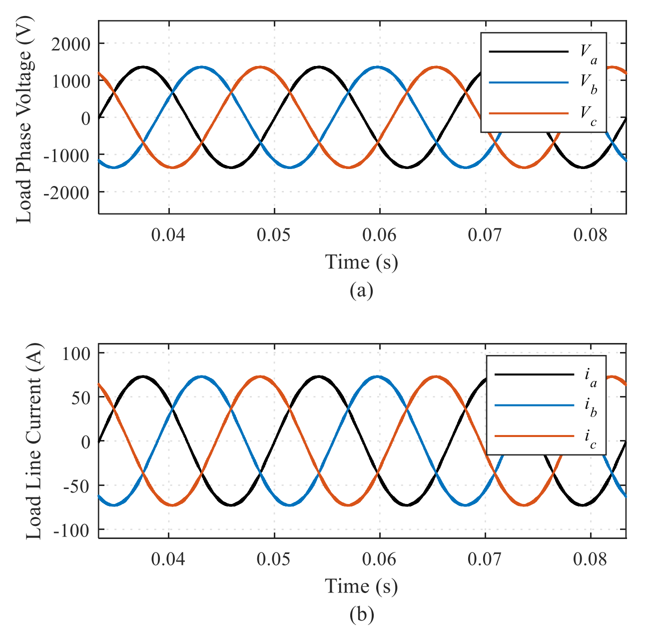

Fig. 7. Four-level MMC (a) load phase voltage and (b) load line current.

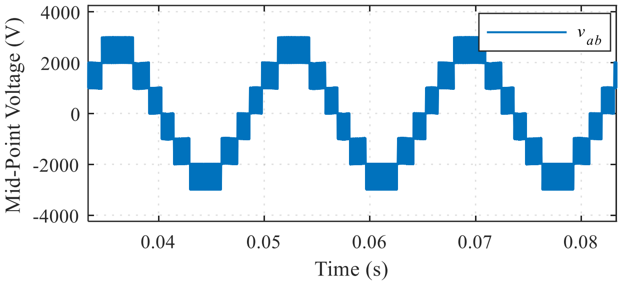

Fig. 8. Four-level MMC mid-point voltage v_{ab}.

The mid-point voltage v_{ab} shown in Fig.8 has seven levels. Although the mid-point voltage of any single phase, v_a v_b or v_c, has only four levels, the differential voltage of any two phases, v_{ab} v_{bc} or v_{ca}, has seven levels.

The submodule capacitor voltage V_{C3} is shown in Fig.9. The capacitor voltage ripple is within 4.8%. The capacitor voltage is well balanced to the expected value (1000 V). However, the fundamental ripples still exist, which are introduced by the arm inductor and stray resistance.

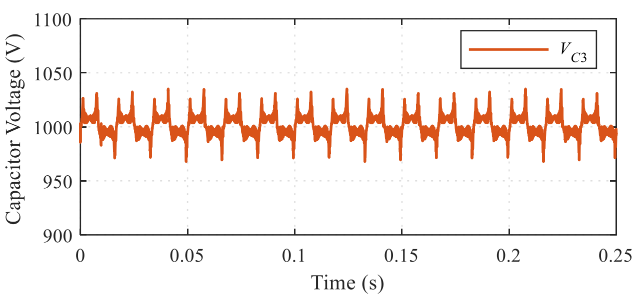

Fig. 9. Four-level MMC submodule capacitor voltage V_{C3}.

B. YMM Based Eleven-Level SC-MMC

Even when randomly select $2N$-3 rows from 11-level submatrix $\mathbf{Y}_2^{(11)}$, there could be 1.3234×10^{20} combinations. Such massive data become impossible for computers to process using analytical method. Hence, we proposed an approximate estimation for higher level SC-MMC by randomly pick 5000 full-rank samples, and run 100 times to find an approximate estimation results. The key parameters for eleven-level SC-MMC are summarized in Table II [1].

TABLE II
ELEVEN-LEVEL MMC SIMULATION KEY PARAMETERS

Apparent Power, S	500 kVA
Fundamental Frequency, f_0	60 Hz
DC-Bus Voltage, V_{dc}	1000 V
Phase Voltage, V_a, V_b, V_c	3200 V
Line Current, I_a, I_b, I_c	52 A
Arm Inductance, L_{arm}	0.1 µH
Submodule Capacitance, C_i	770 µF
Number of Submodules per Arm	10

where $i = 1, 2, \ldots, 60$.

The minimum number of switching actions during one cycle is 6514. The dimension of eleven-level $\mathbf{Y}$ matrix is 173×20. Compared to the original switching pattern [1] which has 7992 switching actions, the optimal switching scheme can lead a reduction of 22.69%. The load phase voltage and load line current are shown in Fig. 10. The THD value is 0.75% for load phase voltage and line current. The mid-point voltage of eleven-level SC-MMC v_{ab} given in Fig.11 has 17 levels. The capacitor voltage ripple shown in Fig.12 is within 5%. The capacitor voltage is well balanced and converging to the expected value (1000 V).

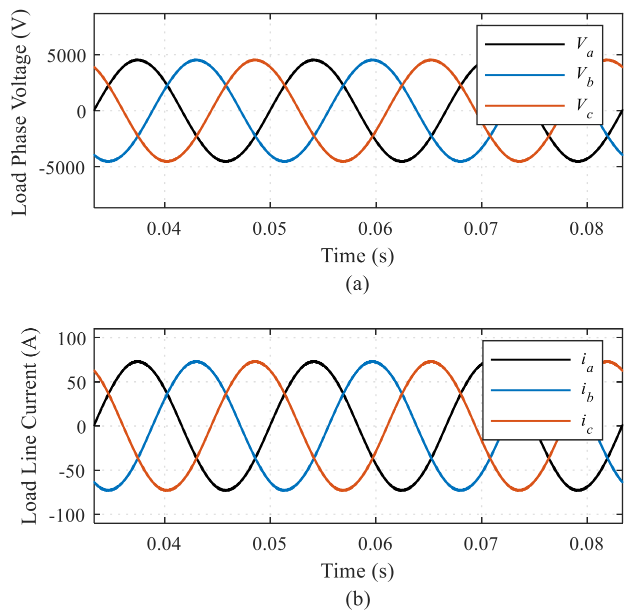

Fig. 10. Eleven-level MMC (a) load phase voltage and (b) load line current.

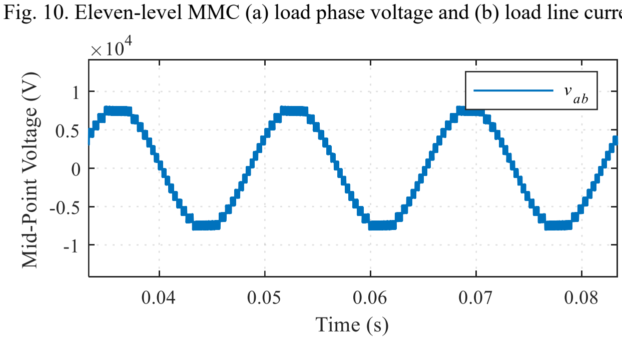

Fig. 11. Eleven-level MMC mid-point voltage v_{ab}.

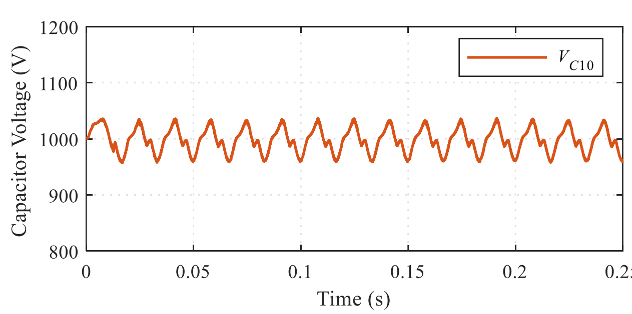

Fig. 12. Eleven-level MMC submodule capacitor voltage V_{C10}.

C. YMM Based Fifty-Level SC-MMC

A 50-level SC-MMC has also been tested and demonstrated the effectiveness of proposed method. There are 98 submodules in each phase for this fifty-level SC-MMC. The dimension for submatrix $\mathbf{Y}_{24}^{(50)}$ is (1.3234×10^{20})-by-98. A matrix of such large dimensions is impossible for computers to process using analytical methods. The key parameters for fifty-level SC-MMC are summarized in Table III.

TABLE III
FIFTY-LEVEL MMC SIMULATION KEY PARAMETERS

Apparent Power, S	2500 kVA
Switching Frequency, f_{sw}	100 kHz
DC-Bus Voltage, V_{dc}	1000 V
Phase Voltage, V_a, V_b, V_c	15.71 kV
Line Current, I_a, I_b, I_c	52 A
Arm Inductance, L_{arm}	0.1 μH
Submodule Capacitance, C_i	4.1 mF
Number of Submodules per Arm	49

where $i = 1, 2, \ldots, 294$.

It achieves a significant reduction in switching actions by approximately 22.33%. Additionally, the load phase voltage shown in Fig.13 has a low THD value of 0.89%, and the capacitor voltage ripple presented in Fig. 14 is within 5%.

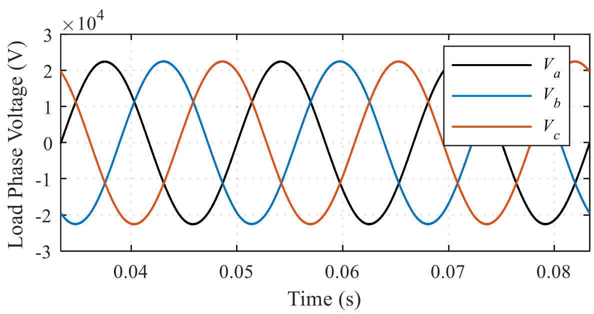

Fig. 13. Load phase voltage of fifty-level MMC.

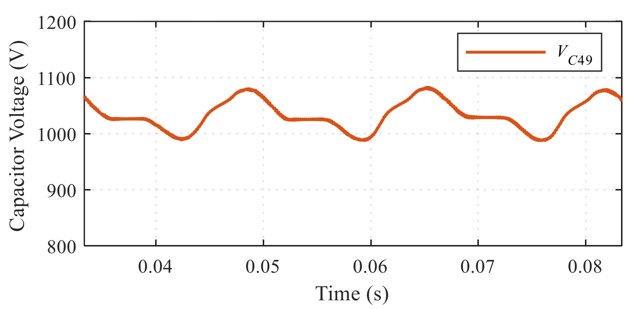

Fig. 14. Fifty-level MMC submodule capacitor voltage V_{C49}.

V. CONCLUSIONS

This paper proposed a general approach to find the optimal switching scheme for SC-MMC using heuristic algorithm GA. A mathematical analysis of the converter switching pattern considering Y matrix modulation has been conducted to formulate an optimization problem for minimizing the number of switching actions of SC-MMC. Case studies have been implemented on different levels of SC-MMC. Compared to the analytical method which cannot handle the massive data, the heuristic method can find the optimal solution within an acceptable time 1 h for four-level SC-MMC. As a result, compared to the original switching pattern, the proposed method can reduce around 22% switching actions. The harmonic analysis confirms the proposed method can result THD value is below 1%. The capacitor voltage deviation is maintained below 5% of the nominal value.

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