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New method of fabrication of suspended metallic single electron transistor (SET)

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Mohammad Istiaque Rahaman ; G. P. Szakmany ; A. O. Orlov ; G. L. Snider

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Mohammad Istiaque Rahaman,[a] G. P. Szakmany, A. O. Orlov, and G. L. Snider

AFFILIATIONS

Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556

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[a]**Author to whom correspondence should be addressed:** mrahaman@nd.edu

ABSTRACT

Charge sensing applications utilizing single electron transistors (SETs) as electrometers face challenges due to nearby background charge movements. In this study, we present an innovative fabrication method for creating suspended Al-AlO_x-Al SETs positioned above a cavity. These suspended SETs exhibit significantly reduced flicker noise with $\frac{1}{f^{\alpha}}$ noise spectral density when compared to their substrate-based counterparts. This noise reduction can be attributed to the elimination of the substrate beneath the SET island. Consequently, our fabricated suspended SETs are highly suitable for demanding charge sensing applications and provide a promising platform for in-depth investigations into the sources of charge noise in such devices.

I. INTRODUCTION

single electron transistors (SETs) are widely recognized for their exceptional charge sensing capabilities, making them useful in diverse applications such as readout charge sensing of qubits in quantum computers[1] and detecting bistable charge states in molecular quantum-dot cellular automata (mQCA).[2] However, the high charge sensitivity of SETs is also its own nemesis. Unpredictable device performance instability can occur due to random charge fluctuations, leading to deviations from the intended bias point. These fluctuations, known as charge noise, exhibit $\frac{1}{f^{\alpha}}$ noise spectral power density in metal–insulator–metal (MIM) SETs. Commonly, charge defects or traps near the SET islands are believed to be the primary hosts for these offset charges. The time-dependent, nonequilibrium relaxation of these charge defects causes offset charges to drift within the defects, resulting in time-dependent variations in MIM SET performance.[3] Identifying and eliminating these charge defects are crucial for ensuring the reliable performance of SETs as charge detectors.

Offset or stray charges can be trapped in three primary locations: within the dielectric tunnel barriers,[3] the insulating region surrounding the SET island,[3,4] and at the metal–substrate interface and substrate.[5] Different theories[3,4] exist regarding the stochastic occupation of charge traps in these varied locations. Although consensus is lacking on the predominant source of charge detect hosts in Al-AlO_x-Al SETs, the primary objective remains minimizing charge noise. Fabricating SETs that are less susceptible to nearby charge fluctuations is crucial, enhancing their suitability for highly sensitive charge sensing applications.

The pursuit of reducing charge noise in metallic single electron transistor (SET) fabrication has led to two primary research avenues. The first focuses on enhancing the dielectric tunnel barrier, and the second aims to improve the interface between the metal and the substrate. In the former approach, various dielectric tunnel barriers have been explored, coupled with different pre- and postanneal steps to passivate offset charge traps.[6,7] However, these efforts still resulted in trap sites and parasitic oxides within the barrier dielectric and the metal–dielectric interfaces, leading to significant random electrical noise.

In the latter direction, research has been conducted on stacked[4] and suspended SETs[8,9] to mitigate charge noise. For suspended SETs, the devices were initially fabricated on a sacrificial layer of SiNx[8] or polymer[9] on a silicon substrate. In the final step, the SiNx or polymer layer was etched or ashed away, suspending the SET island at a relatively small distance of 300 and 50 nm above the substrate. Previous studies either did not mention the charging energy[4] or reported low values, such as 800 μeV at

30 mK[9] and 13.5 μeV at 200 mK.[8] Additionally, none of the aforementioned works[4,8,9] provided insights into the gate-dependent charging characteristics of the SETs.

In this study, we adopted an innovative approach to eliminate charge noise arising from both the metal–substrate interface and the substrate itself by removing the underlying substrate of the SET. We introduce a new fabrication technique to create "suspended" Al-Al_2O_3-Al SETs. The SETs were suspended by etching away the substrate underneath the SET island, resulting in approximately 5 μm diameter cavity. The charging energy of our suspended SETs measured approximately 1.5 meV, significantly higher than those reported in previous studies.[4,8,9]

To evaluate the impact of substrate removal, we conducted comparative measurements between the "suspended" SETs and "reference" SETs where the substrate remained intact. The "reference" SETs displayed markedly higher random offset charge noise compared to the "suspended" SETs. Details regarding the fabrication and measurements can be found in Sec. II, with the study's findings discussed in Sec. III.

II. DEVICE FABRICATION AND MEASUREMENT

A scanning electron micrograph (SEM) of a representative "suspended" SET is presented in Fig. 1. A highly resistive (>2 kΩcm) silicon wafer was used as the substrate. Initially, to remove any native SiO_2, the substrate underwent a 10:1 buffered hydrofluoric acid (BHF) treatment for 30 s. The SET patterns were defined on polymethyl methacrylate (PMMA-950C2) with polymethylglutarimide (PMGI-SF5) as the underlying layer, placed on the substrate. This exposure was carried out using a Raith EBPG 5200 100 keV Electron Beam Lithography (EBL) system. Subsequently, the aluminum SETs were fabricated through a standard dual-angle shadow evaporation process[10] in a thermal evaporator. The chamber's base pressure at the beginning of both aluminum evaporation was 0.4 μTorr. The first aluminum layer was oxidized *in situ* before the deposition of the second aluminum layer. The intermediate oxidation process was conducted for 15 min at 7 μTorr at 20 °C. Oxygen was introduced into the chamber during the oxidation process through a parallel combination of a needle valve and a leak valve. The thicknesses of the two aluminum layers were 15 and 40 nm, respectively.

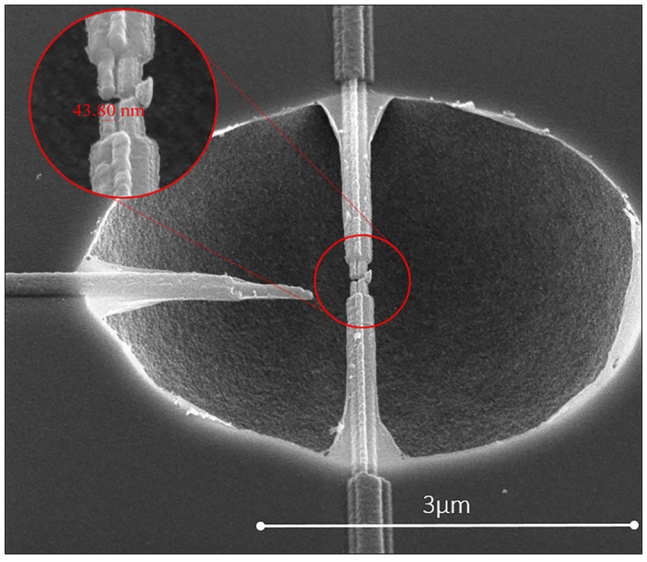

FIG. 1. SEM image of a suspended aluminum SET with the gate also suspended above the cavity on the left side. The top and bottom electrodes are interchangeable as the source or drain of the SET. An aluminum Island is positioned between the source and the drain, separated by two Al_2O_3 tunnel barriers. The inset provides a magnified view of the SET.

Following the fabrication of the SETs, additional electron beam exposure was performed on PMMA to create cavities underneath the selected SETs. The cavity exposure patterns on PMMA were exclusively applied to specific SETs, protecting the remaining SETs with PMMA. The "suspended" configuration was achieved by selectively etching the silicon substrate through the PMMA openings using XeF_2 with He as the carrier gas.[11] This static etching of silicon was carried out using a MemsStar's BT001 dry release etching system. Notably, XeF_2 exclusively reacts with silicon, preserving the SET performance. Subsequently, PMMA was removed using a radio frequency plasma asher system. The resulting etched cavity had a diameter of approximately 5 μm around the SET island. SETs protected by PMMA without any cavities underneath were designated as "reference" SETs. These "reference" SETs were utilized for performance comparison with the "suspended" SETs.

Upon completing the device fabrication, the devices were wire bonded onto a chip carrier and cooled to 2.7 K inside a dry pulsed tube He_3 cryostat. The differential conductance ($G_{SET} = dI_{ds}/dV_{ds}$) of the SETs was measured using the Sanford Research Systems SR830 lock-in amplifier with an AC probing voltage of 0.2 mV at 1.5 kHz. To measure the noise power spectral density, Pico Technology's PicoScope 4226 spectrum analyzer was connected at the output of the transimpedance amplifier. Importantly, both the "suspended" and "reference" devices presented in this study were fabricated on the same substrate in a single process run, utilizing identical computer-aided design (CAD) layouts for both configurations.

III. RESULTS AND DISCUSSION

The Coulomb blockade oscillation (CBO) characteristics of both suspended and reference SETs are displayed in Fig. 2. These CBO patterns were obtained by plotting the differential conductance ($G = dI_{ds}/dV_{ds}$) against the gate voltage, V_g, while maintaining $V_{ds} = 0$ V at a temperature of 2.7 K. The gate voltage was swept from 0 to 1 V twice, with 1-s delay between acquisitions. Figure 2(a) illustrates the CBO of the reference device, displaying a significant shift of the conductance peak within the same gate voltage range. This shift is attributed to time-dependent nonequilibrium offset charge movements near the SET island. These stochastic offset charge movements, drifting into trap or defect sites, cause the uncontrolled hysteric nature of the CBO shift.

In contrast, Fig. 2(b) shows the CBO pattern of the suspended SET, which exhibits a minimal shift in the peaks of conductance. This minimal shift is achieved by eliminating one of the primary sources of stray or offset charges: the metal–substrate interface and substrate beneath the SET island. In this configuration, the

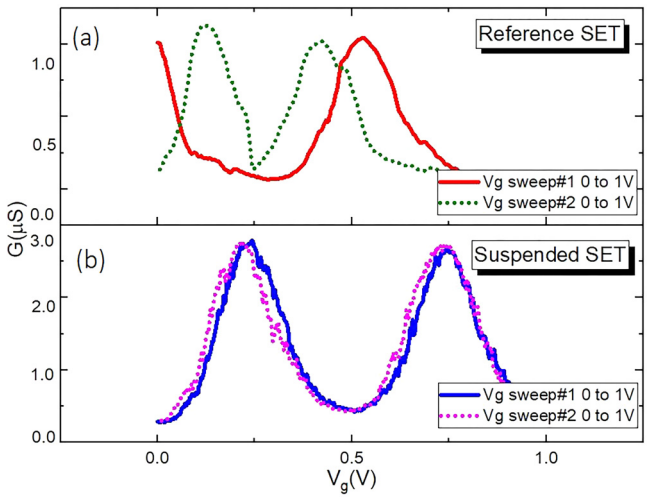

FIG. 2. CBO patterns of (a) the reference SET and (b) the suspended SET at 2.7 K. The differential conductance, G_{SET}, is plotted against gate voltage, V_g, while maintaining $V_{ds} = 0$ mV. The gate voltage was swept from 0 to 1 V twice, with a 1-s delay between the sweeps.

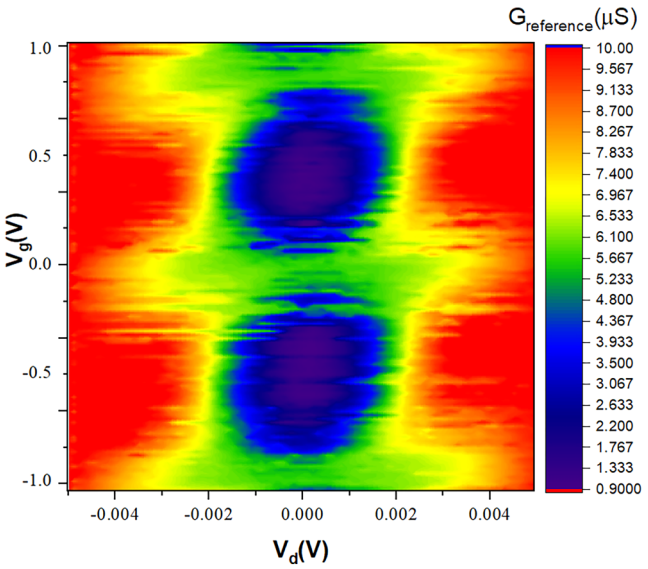

FIG. 4. Stability diagram of reference SET. Differential conductance, $G_{reference}$, is plotted by sweeping both V_d and V_g at 2.7 K.

substrate has been completely etched, and the SET is suspended on a cavity with an approximate diameter of 5 μm.

The stability diagrams, also known as Coulomb diamond plots, for both the suspended and reference SETs are presented in Figs. 3 and 4, respectively. These diagrams are obtained by plotting the differential conductance, G_{SET}, while varying both the gate voltage, V_g, and the drain voltage, V_d. Initially, V_g was swept in the range of -1 to 1 V while maintaining a fixed V_d. Subsequently, V_d was changed to a different value and V_g was swept again from -1 to 1 V. This process was repeated for the entire range of V_d from -5 to 5 mV. The Coulomb diamond plot of the suspended SET (Fig. 3) remains stable across the entire scanning range. In contrast, the charging diagram of the reference SET in Fig. 4 reveals the presence of large charge noise, evidenced by the random fluctuations in its differential conductance.

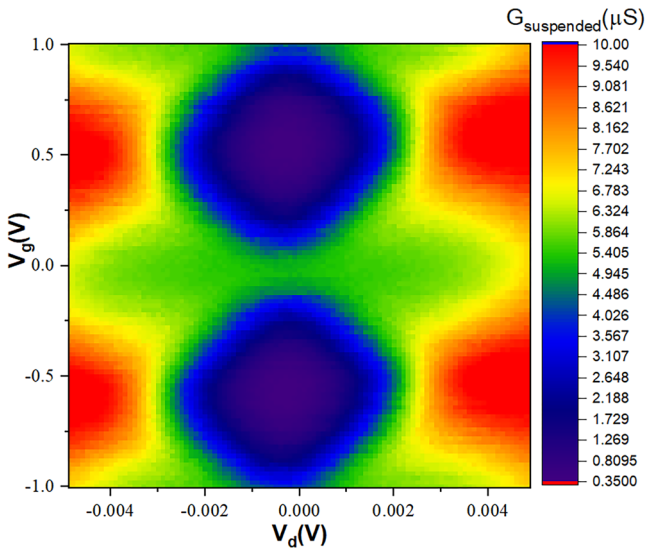

FIG. 3. Stability diagram of suspended SET. Differential conductance, $G_{suspended}$, is plotted by sweeping both V_d and V_g at 2.7 K.

The equivalent circuit diagram for both the reference and suspended SET is illustrated in Fig. 5. To determine SET parameters, a simulation based on the orthodox Coulomb blockade theory[12] was fitted to the measured stability plot (Fig. 3) of the suspended SET. The extracted values of the circuit parameters for the suspended SET are $C_g = 1.48$ aF, $C_d = 27.6$ aF, $C_s = 18.4$ aF, and $R_d = R_s = 0.5$ MΩ. Notably, similar values of circuit parameters were extracted for the reference SET.

The charging energy of a SET is defined as the energy required to add an excess electron to the island from the source. It is calculated using the formula $E_c = \frac{e^2}{2C_\Sigma}$, where e represents the charge of an electron, and C_Σ, the total capacitance, is the sum of C_g, C_d, and C_s. The charging energy for the suspended SET and reference SET has been determined to be approximately 1.5 and 0.5 meV, respectively. These values are extracted from their respective charging diagrams shown in Figs. 3 and 4. For the suspended SET, the calculated charging energy from the simulated circuit parameters, mentioned earlier, is 1.6 meV, which aligns well with the experimental observation.

The observed increase in charging energy for the suspended SET (1.5 meV) compared to the reference device (0.5 meV) can be attributed to two factors. First, the removal of the silicon substrate beneath the suspended SET reduced its total capacitance, leading to a higher charging energy. Second, the overlap between the source and drain with island of the SET was greater in the reference SET

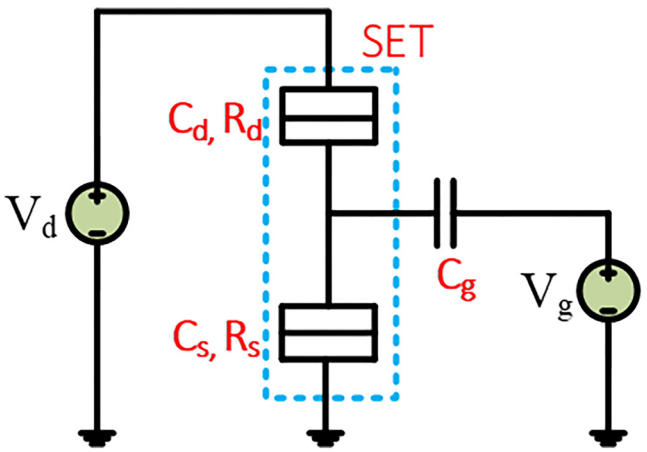

FIG. 5. Equivalent circuit diagram for the reference and suspended SET. Here, C_g, C_d, C_s, R_d, and R_s represent the gate capacitance, drain-to-island junction capacitance, source-to-island junction capacitance, drain resistance, and source resistance, respectively.

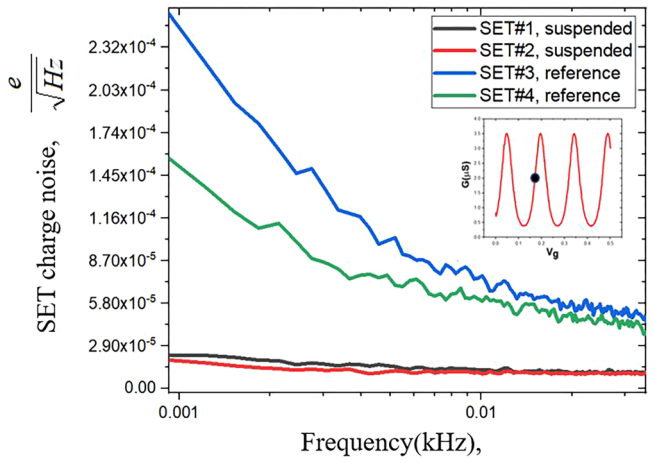

FIG. 6. Equivalent charge noise in $\frac{e}{\sqrt{Hz}}$ for two representative reference SETs and two suspended SETs, measured at $V_{ds} = 0$ V at their most sensitive bias points. The inset figure shows a representative bias point of a SET indicated by a black dot on its CBO curve. The charge sensitivities for SET-1 (suspended), SET-2 (suspended), SET-3 (reference), and SET-4 (reference) were determined as 9.87, 8.21, 3.56, and 4.51 $\frac{nA}{e}$, respectively, obtained from their respective CBO. Output noise power was measured using the PicoScope 4226 spectrum analyzer.

(SEM not shown), resulting in a higher total capacitance and, consequently, a decreased charging energy. This overlap variation is influenced by the thickness variations of the bottom resist, PMGI-SF5, due to the nonuniform spin coating process. As the thickness of PMGI-SF5 decreases, the overlap increases, leading to a reduction in charging energy.

In the context of noise measurement, it is crucial to bias the SET at the midpoint of either its rising or falling slope of CBO, where the sensitivity of the SET is at its peak, and maintain this bias point consistently throughout the noise measurement process. An exemplary bias point for noise measurement is indicated as a dot in the inset of Fig. 6.

Charge noise, expressed as $S_Q = \frac{S_I}{\eta}$,[4] was calculated for both the reference and suspended SETs within the frequency range of 0–0.05 kHz at 2.7 K, as illustrated in Fig. 6. Here, η represents the charge sensitivity of the SET under test in $\frac{nA}{e}$, and S_I denotes the output noise power of the SET in $\frac{nA}{\sqrt{Hz}}$. The equivalent charge noise for two representative suspended SETs exhibited lower $\frac{1}{f^\alpha}$ noise when compared to two representative reference devices. Remarkably, our extensive testing, conducted on more than 25 reference and suspended SETs, consistently yielded similar outcomes. This higher charge noise in reference SETs is primarily attributed to contributions from the substrate.

Despite the lower equivalent charge noise exhibited by suspended SETs compared to the reference SETs, the suspended devices still displayed characteristic charge offset drifts and long-term charge instability, similar to other Al-AlO_x-Al SETs.[3] These performance instabilities arise from defects in the oxide tunnel barriers and the peripheral native oxide of the aluminum SETs. The presence of OH^- ions trapped in the oxide, mechanical stress in the insulating film, and metal droplets within the oxide are believed to be the primary sources of these charge defects.[3] Additionally, we harbor concerns regarding two specific fabrication steps that may contribute to the performance instability in the suspended devices. First, the silicon etching process using XeF_2 to suspend the SETs might create an interfacial layer of AlF in the suspended SETs, potentially hosting additional defects. Second, the O_2 plasma ashing steps used for removing the PMMA may result in plasma-induced damage to the SETs.

IV. CONCLUSION

In this study, we have presented an advanced fabrication process for developing suspended MIM SETs. These suspended SETs exhibit reduced $\frac{1}{f^\alpha}$ charge noise compared to their counterparts fabricated on silicon substrates. This improved fabrication technique eliminates substrate-induced contributions to charge noise, allowing for in-depth exploration of the origins of charge noise in MIM SETs. Due to its unique structure, this device holds significant potential as a Nano MEMS device and enable investigations into the interactions between single charge transport and oscillations in nearby suspended structures.

ACKNOWLEDGMENTS

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Mohammad Istiaque Rahaman: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Investigation (lead);

Methodology (lead); Validation (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (equal). **G. P. Szakmany:** Resources (equal). **A. O. Orlov:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Software (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal). **G. L. Snider:** Formal analysis (equal); Funding acquisition (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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