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ORIGINAL RESEARCH ARTICLE

Comparative Study of E-beam and Optical Probing Approaches in Attacking the ICs

Elham Amini · Jörg Jatzkowski · Tuba Kiyan · Lars Renkes · Thilo Krachenfels · Shahin Tajik · Christian Boit · Frank Altmann · Sebastian Brand · Jean-Pierre Seifert

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Abstract Optical probing methods through the chip backside have been demonstrated to be powerful attack techniques in the field of electronic security. However, these attacks typically require specific circuit conditions, such as enforcing gate or register switching at certain frequencies or repeating measurements over multiple executions to achieve an acceptable signal-to-noise ratio (SNR). Meeting these requirements can pose challenges, such as low-frequency switching or inaccessibility of the control signals. This study evaluates these requirements for contactless electron- and photon-based probing attacks by performing extensive experiments and discussing the advantages and drawbacks of each approach. Our findings demonstrate that E-beam probing has the potential to outperform optical methods in scenarios involving static or low-frequency circuit activities. Nevertheless, E-beam probing requires the assistance of optical techniques for area localization and requires aggressive thinning and trenching to the STI level.

Keywords E-beam probing · Optical probing · Photon emission · IC security · IC Backside

Introduction

The development of signal probing techniques through the integrated circuit (IC) back side has been both beneficial for fault isolation and a significant threat to chip security. Contactless probing through the front side of the ICs became impossible due to multiple metal layers. However, with the introduction of flip-chip packages, a new era began enabling probing from the chip backside.

E-beam techniques faded away until recently since the signal lines were not reachable from the thick silicon on the back side. Therefore, optical techniques, such as Photon Emission Microscopy (PEM), as well as Laser Voltage Probing (LVP), also called Electro-Optical Probing (EOP), and Laser Voltage Imaging (LVI) or Electro-Optical Frequency Mapping (EOFM) became the primary option for contactless probing, exploiting side-channel information, such as emitted photons or electro-optical effects, to extract sensitive data from ICs [1–3].

Optical side-channel attacks that are based on failure analysis (FA) techniques have proven powerful in extracting sensitive data, even with limited knowledge of the IC under attack and can be accomplished in a matter of days (from initial analysis of an IC's activity to full data extraction) [4–7]. However, optical techniques face challenges such as spatial resolution due to shrinking geometries and the long wavelengths of NIR light, as well

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E. Amini (✉) · T. Kiyan · L. Renkes · T. Krachenfels · C. Boit · J.-P. Seifert
Security in Telecommunications, Technische Universität Berlin, Berlin, Germany
e-mail: elham.amini@tu-berlin.de

J. Jatzkowski (✉) · F. Altmann · S. Brand
Fraunhofer Institute for Microstructure of Materials and Systems IMWS, Halle, Germany
e-mail: joerg.jatzkowski@imws.fraunhofer.de

S. Tajik
Worcester Polytechnic Institute, Worcester, MA, USA

as declining signal intensity with decreasing supply voltages [8, 9]. To improve signal-to- noise ratio (SNR), longer execution times, higher frequencies, or higher supply voltages are required, which may not always be feasible or helpful. Additionally, knowing the switching frequency is necessary for some optical techniques, such as EOFM, which may not be readily available or known to the attacker. In this work, we compare the optical probing techniques with the E-beam probing method in extracting IC structure signals through the chip backside. E-beam probing, which can achieve resolutions down to around 1 nm, offers advantages over side-channel attacks, where the optical resolution is at best about 200 nm with a Solid Immersion Lens (SIL) and 1 µm without [10]. We demonstrate the distinct advantages of E-beam probing over optical side-channel techniques. Through extensive experiments on a programmable logic device, we show its effectiveness in acquiring signals at lower frequency ranges where optical techniques counter limitations. E-beam probing is effective even in smaller technology sizes where optical techniques weaken due to decreasing supply voltages. While optical techniques may require increased acquisition time, frequency, or core voltage to obtain signals, which may not always be feasible or helpful, E-beam probing proves promising for hardware security, as it can probe signals for frequencies as low as 100 Hz, typically unachievable for optical techniques. Thus, E-beam Probing overcomes challenges faced by optical techniques, offering a robust solution for hardware security [11].

However, E-beam probing has drawbacks, such as the requirement to thin the silicon substrate to the STI level, leading to critical heat dissipation concerns. Thinning the entire IC to the STI level is time-consuming and expensive, necessitating thinning only in areas where signal extraction is needed. Optical techniques like PEM are essential for identifying the area of interest.

This paper is organized as follows: "Background" section describes the optical techniques and E-beam probing methods. The device under test and the setups used for the experiments are introduced in "Experimental Setup" section. "Results and Discussion" section explains the experiments and discusses the results. Finally, "Conclusions" section concludes the work.

Background

This section describes the contactless probing techniques, EOFM/EOP, PEM, and E-beam probing that are used in this work in more detail.

Optical Techniques

Photon Emission

Transistors have three modes of operation: cut-off, saturation, and linear. Photon emission can be strong enough in saturation because transistors have high drain-source voltages in this mode. That is the reason why a higher supply voltage is desired for a stronger PEM signal. On the other hand, transistors operate in saturation region for a very short time during switching from logic high to logic low transitions and vice versa. The rest of the time, they stay either off or operate in the linear region. Although these transitions happen in a very short amount of time, a photon emission signature can still be detected by a very sensitive camera if the signal frequency is high enough. Hence, the higher the switching frequency and the supply voltage are, the stronger the PEM signal will be. The PEM technique, along with EOFM and E-beam probing, is illustrated in Fig. 1. For our PEM measurements, we used a calibrated InGaAs camera, which was cooled to − 70 °C.

Optical Probing

In EOFM, a light beam scans an area of interest on the backside of a chip (see Fig. 1). The light beam travels through the backside and hits the active regions of transistors on the front side and gets reflected. The reflected light will have a modulated amplitude and phase depending on the operational mode of the transistors due to the absorption coefficient and refractive index changes [2]. The modulated light beam is then measured with a photodetector and converted into an electrical signal. After spectrum analysis of this signal, only signals switching at a chosen frequency are extracted and displayed as a 2-dimensional frequency map. As opposed to PEM and E-beam probing, it is required to know the internal switching frequency of the devices for EOFM [3]. For EOP, the light beam is parked on a desired position on the chip backside instead of scanning an area. And then, the modulations in the reflected light are detected just like EOFM to form a signal waveform in the time domain. Due to the low SNR of the reflected light signal, many iterations have to be integrated. Therefore, we need a reference signal from the device, for example, the clock or the input signal of the inverter chain for waveform acquisition. For EOP, it is not required to know the signal's frequency.

E-beam Probing

Electron beam probing is known as an FA technique that can generate scanning electron microscopy (SEM) images or voltage waveforms in the time domain of an internal IC

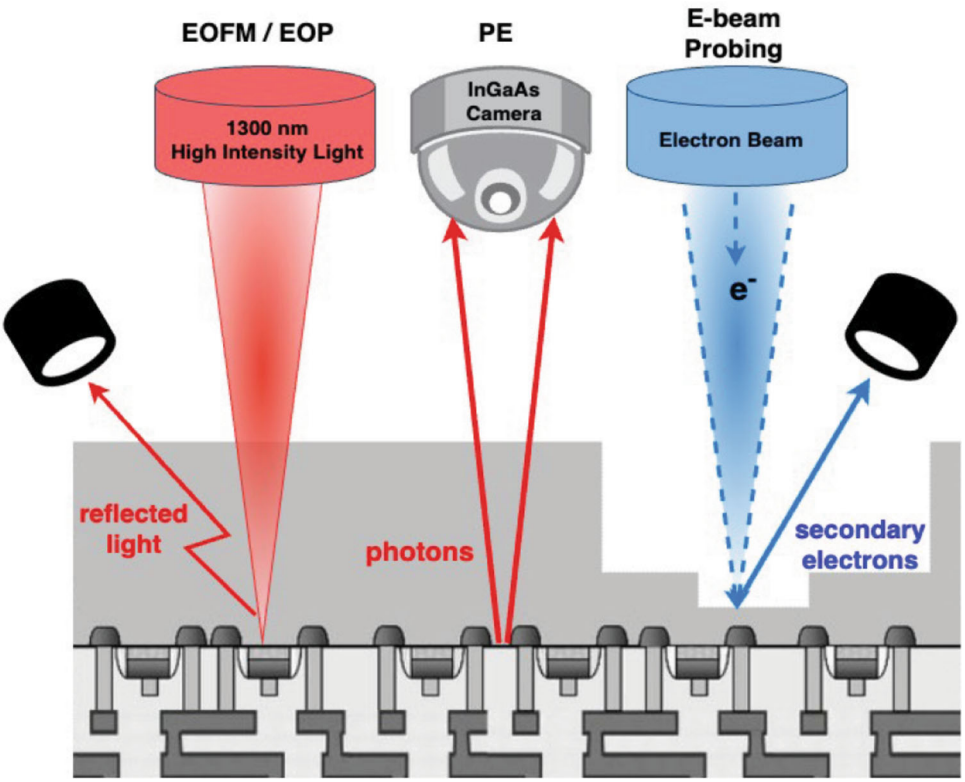

Fig. 1 Illustration of contactless optical and E-beam probing techniques on the backside of the chip. Photons are emitted from switching transistors and captured by a camera to acquire a PEM image. EOFM/EOP and E-beam map the activity of the structures by detecting the reflected light and secondary electrons, respectively

node. In an e-beam system, a high-energy electron source, typically an electron gun, emits a focused beam of electrons. These electrons are accelerated to high speeds using electromagnetic fields. As the accelerated electrons (primary beam) interact with a sample, various interactions occur with the atoms in the sample material, producing signals, such as secondary electrons, backscattered electrons, X-rays, and others, depending on the technique and the type of interaction. This process is illustrated in Fig. 2. These signals contain information about the sample's topography, composition, crystallography, and other properties. An SEM captures and analyzes these signals. By processing and interpreting the detected signals, generating images or other analytical data about the sample. For instance, Backscattered electrons (BSE) provide valuable information about the structural composition of the IC. BSE signals are particularly sensitive to the atomic number (Z) of elements in the sample. Heavier elements with higher atomic numbers tend to backscatter more electrons. Analyzing the intensity of BSE signals enables FA engineers to identify the presence and distribution of different elements within the IC. This helps in locating contaminants, defects, or foreign materials. In this research, we focus on Analyzing secondary electrons (SE), which are low-energy electrons emitted from the sample's surface when bombarded by the primary electron beam. Secondary electrons play a crucial role in localization and fault

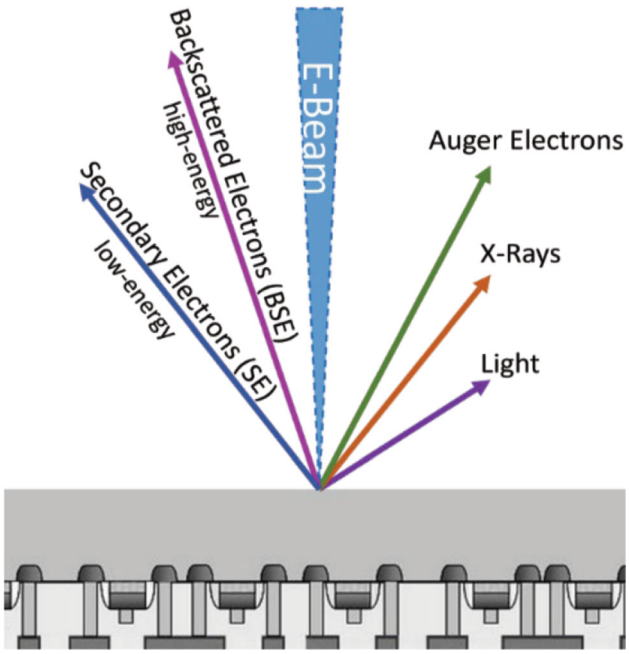

Fig. 2 Principle of E-beam probing: Primary electron beam interacts with the sample, and several different types of secondary signals are generated and detected for analysis

analysis in techniques such as Voltage Contrast Imaging (VCI) and Current-Contrast Imaging (CCI). Variations in voltage or current within an IC can influence the emission or reflection of secondary electrons. Detecting these

variations in secondary electron emission helps localize and identify regions with voltage differences, indicating faults or active regions within the IC.

While E-beam probing on the front side of the die has been widely utilized in the past, recent advancement in flip-chip technologies and increasing the number of metal layers up to ten have prompted FA engineers to explore this technique from the IC backside. E-beam probing through the chip backside has been proven as a very powerful method, relying on various contrast mechanisms generated by the electron beam, particularly low-energy secondary electrons [12, 13]. Contrast mechanisms, such as capacitive coupled voltage contrast (CCVC), enable the visualization of buried and biased structures, such as the Source/Drain or channel region of a transistor [14]. All these contrast mechanisms could only be visualized close to the active IC structure. Achieving backside access involves a preparation down to the shallow trench isolation (STI) level, typically accomplished through local Plasma-FIB trenching of the silicon substrate, see Fig. 3. The trench size must allow secondary electrons to leave and reach the detector. When scanning an electrically functional IC with the electron beam, an additional contrast is observed due to electrical potentials of single transistor structures. This introduces the possibility of using two different imaging methods to investigate the switching states of single transistors in functional ICs. In normal SEM mode, static levels or signals with a very low frequency can be imaged, while time-dependent measurements can be performed at higher switching frequencies in spot mode, where the E-beam stays at a defined position, and the detector signal is measured as a function of time [15].

Experimental Setup

Device under Test

The device used in these experiments is an Intel/Altera MAX V Complex Programmable Logic Device (CPLD) with part number 5M80ZT100C5N, manufactured in 180nm technology. This device was selected primarily due to its larger STI level, high availability, and cost-effectiveness. As test structures, we have implemented inverter chains on the MAX V, with the input and output of the inverter chains routed to I/O pins of the CPLD. An inverter chain consists of 10 inverters and is implemented into one Logic Array Block (LAB), which contains 10 Logic Elements (LEs).

Sample Preparation

To prepare a sample for E-beam probing, we need to thin down the silicon to the STI level. For this purpose, the die is first mechanically thinned down to 25 µm silicon thickness using diamond lapping films. Then, a local trench is milled by gas-assisted focused ion beam preparation down to approx. 3.5 µm remaining silicon at the trench bottom [16]. The final preparation for reaching down to STI level is done by a chemical mechanical polishing (CMP) process. The used technique was a standard CMP step for silicon with a colloidal silica/alumina solution with 50 nm particles and a pH level of 9.8. The schematic of sample preparation for E-beam probing is shown in Fig. 3. Figure 4 shows the FIB trench and silicon surface after CMP process. For the optical measurements, the silicon thickness of the die is thinned down to 60 µm.

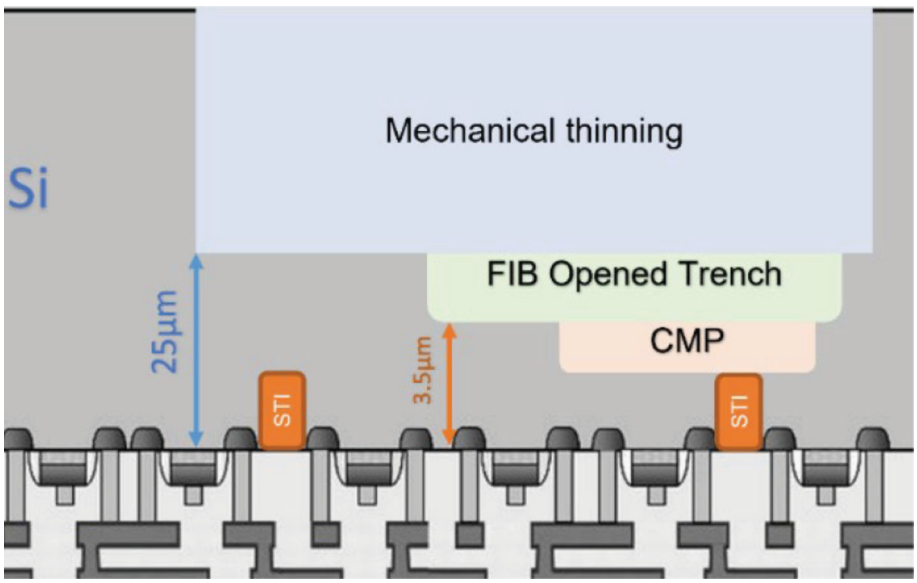

Fig. 3 Schematic of sample preparation for E-beam probing. The die is mechanically thinned down to 25 µm silicon thickness, and then a trench is opened by a FIB to approx. 3.5 µm remaining silicon. In the end, the STI level is reached using CMP

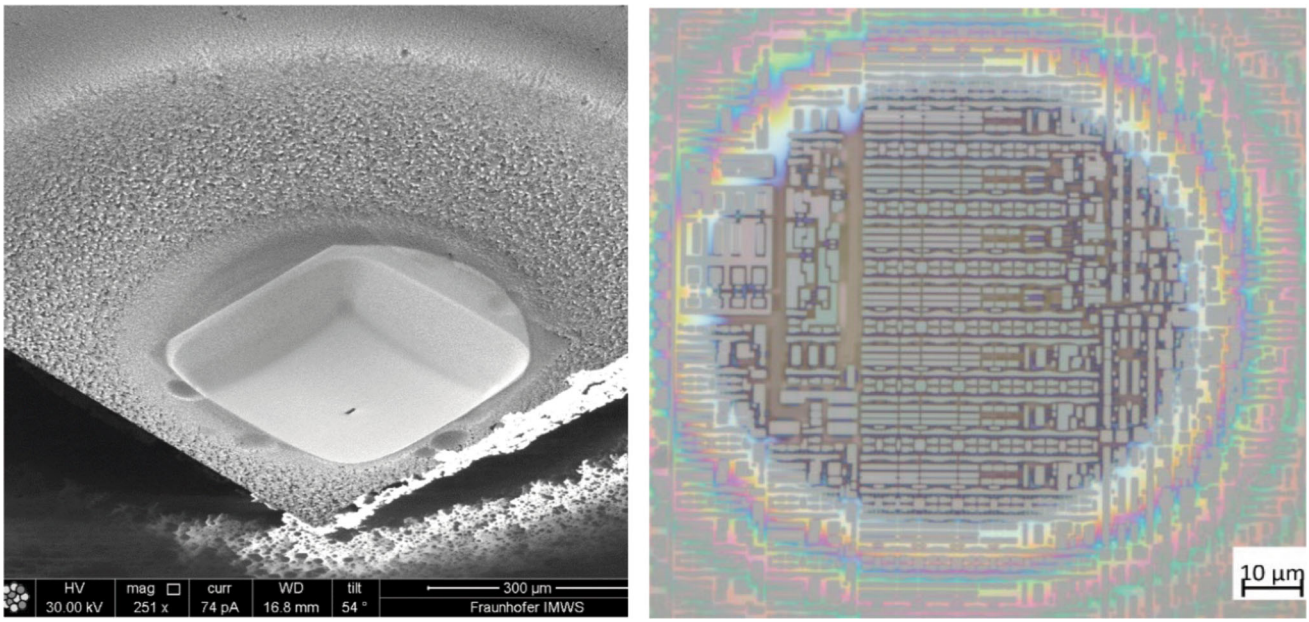

Fig. 4 (Left)Trench opened using gas-assisted focused ion beam, (Right) Thinning down to the STI level using CMP process

Optical Setup

In this work, a sophisticated FA tool, Hamamatsu PHEMOS 1000 is used for optical experiments. The photon emissions are captured by an InGaAs camera with and for EOFM/EOP experiments a 1300 nm high-intensity light source is used. For both sets of experiments, we used a 50x magnification lens.

E-beam Probing Setup

E-beam imaging is realized with a Zeiss Sigma 300 SEM. In addition to a low acceleration voltage, an energy-sensitive in-lens detector is used for high-contrast imaging. The electrical contacts inside the vacuum chamber are realized by electrical feedthrough. The input of the inverter chain is connected to an external function generator Keysight 33500B.

Results and Discussion

To assess the optical probing and E-beam probing, we have implemented inverter chains on two MAX V devices; one was used for optical and the other one for E-beam probing. The reason for implementing inverter chains for these experiments is that inverter chains are the basic blocks of several security primitives, such as delay based PUFs, RO-based TRNGs, etc. For comparing the methods, the same position on the devices has been investigated. In the following section, the results of each technique are presented.

Optical Techniques

Figures 5, 6 and 7 show the results of the optical measurements (PEM, EOFM, and EOP, respectively) performed using a Hamamatsu PHEMOS-1000 microscope. For each measurement, the input of the inverter chains has been connected to an arbitrary function generator, outputting a square wave with a 50% duty cycle for various frequencies (2 MHz, 1 MHz, 500 kHz, and 100 kHz). For all measurements, we see a decrease in the signal-to-noise ratio when we lower the switching frequency of the inverters.

Figure 5 shows the results of the PEM measurements overlaid on the pattern image of the IC. The measurements have been performed with 50x optical magnification and the resulting frame shows all ten LEs that form the inverter chain. It is observable that the signal strength weakens, and consequently, the background noise becomes dominant in frequencies lower than 100 kHz. Figure 6 shows the resulting frequency maps of the EOFM measurements. The measurement has been performed with 50x optical and 8x digital magnification and the resulting frame shows roughly one LE of the CPLD. Once again it is visible that for 100 kHz, the signal strength is already getting worse when compared to the higher frequency ranges. Figure 7 shows the resulting signal waveforms acquired by the EOP measurements. On the x-axis, the time is displayed in µs, and on the y-axis, the intensity of the signal is displayed in arbitrary units. It can be seen that high-frequency noise is added to the investigated waveform, although the waveform is still detectable. The emerging smaller node

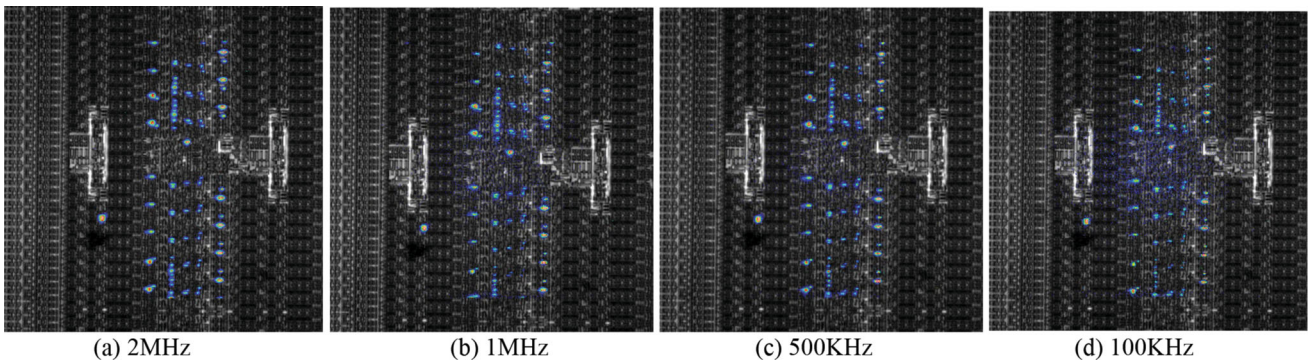

Fig. 5 PE images of the inverter chain at different frequencies. Emitted photons are captured by an InGaAs camera, with a 50x lens for 180 s

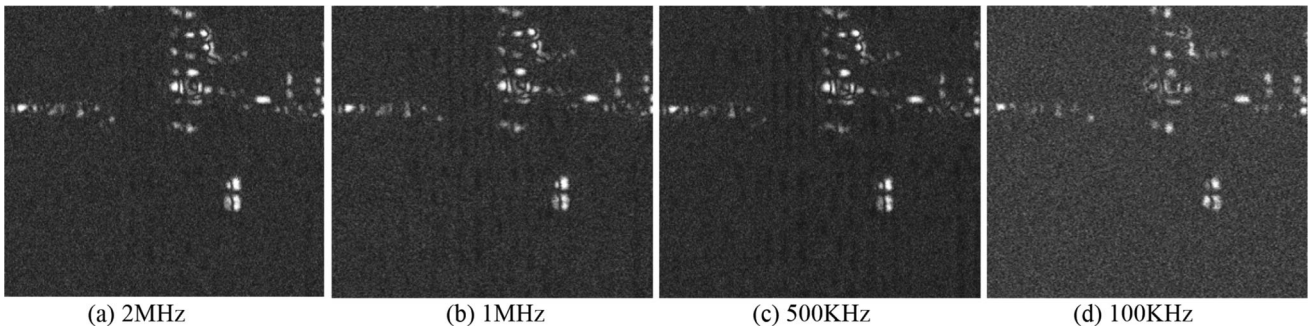

Fig. 6 EOFM at different frequencies. The images are acquired by a 50x lens with 8x digital zoom and with a scanning speed of 1 ms/pixel

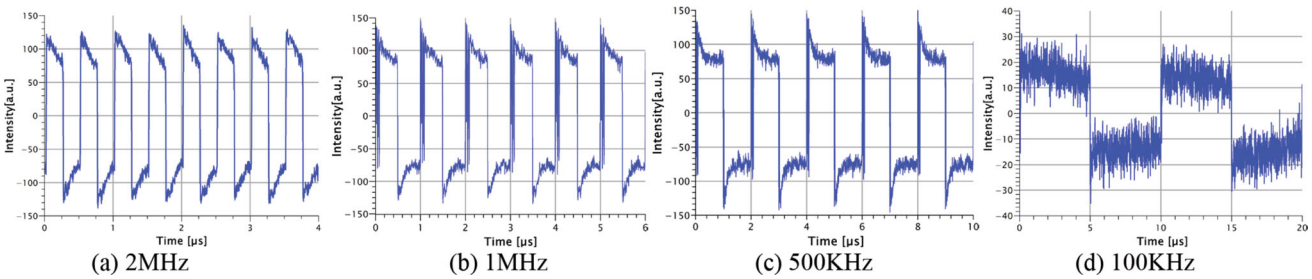

Fig. 7 EOP measurements at different frequencies. We used 50x lens and parked the laser beam on the area of interest

technologies, compared to the device under test in this research, offer lower operating voltages and higher operating frequencies. With lower operating voltages, EOFM and EOP measurements show more noise and PE becomes weaker. However, higher operating frequencies improve PE, with no significant impact EOFM/EOP, as long as the operating frequency remains lower than the sampling frequency.

E-beam Probing

The SEM images in Fig. 8 show the IC Structure before powering up and for static high and low input levels of the inverter chain. Without powering up the device, the silicon islands show only slight variation in contrast due to differences in size and electrical connections of the individual islands, resulting in slightly different charge-up by the electron beam during scanning. In the power-on state, this low charge is superimposed by the significantly higher potential of the individual transistors, resulting in different contrast values within individual silicon islands depending on the different transistor potentials. The different voltage levels of single Source-, Drain- or Channel areas generate varying voltage contrast levels. This contrast is independent from surrounding transistors, whether they operate at identical or different voltage levels or frequencies. Contrast is generated by a modification of secondary electron (SE) yield depending on the additional surface potential of the scanned area. However, if multiple transistor structures are within the interaction volume of the electron beam, there

could be an overlay and therefore an influence of neighboring structures could happen. At the utilized accelerating voltage of 1kV, the interaction volume is typically in the range of 35nm. Additionally, the used in-column detector further limits the detectable area further by focusing on secondary electrons of the first order (necessary to detect voltage contrast) which are only generated close to the primary beam. In general SEM parameters can be adjusted for higher resolution but require increased effort during sample investigation, which was not necessary for the used samples.

A static programming component is also required to realize the inverter chain, and these areas do not change the contrast value depending on the input signal (e.g., green marked area). However, transistors responsible for the dynamic signal processing change their logical state (marked in red) if the input signal changes from high to low.

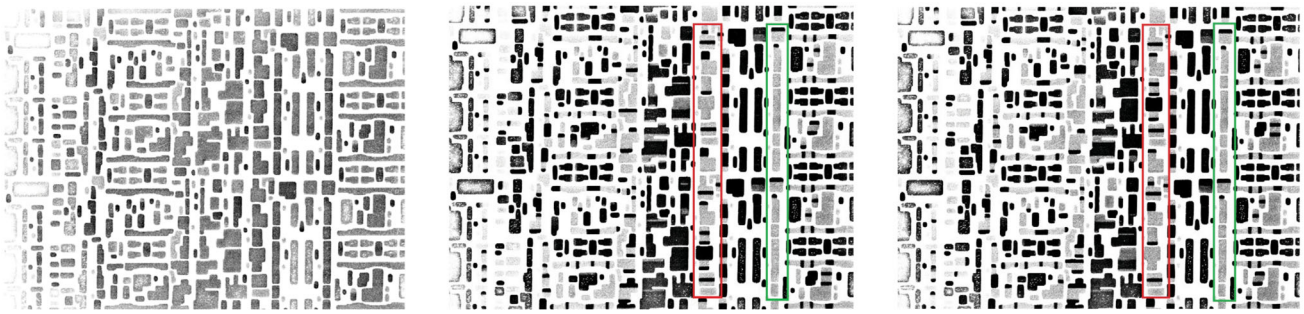

Fig. 8 E-beam images at different electrical static states of inverter chain

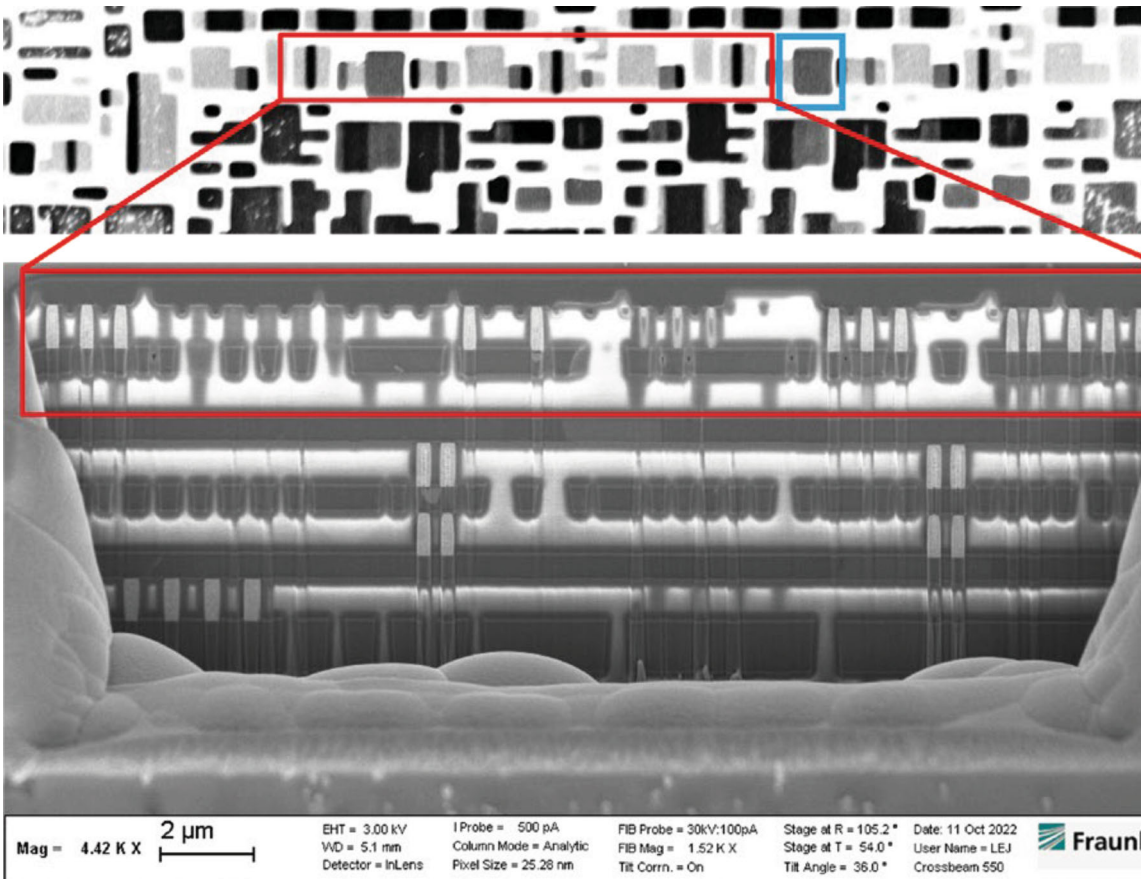

Fig. 9. E-beam image (top) and FIB cross section (bottom) of the structure

To realize E-beam images with "black and white" contrast, the electrical signals of single transistors must be constant during the scanning time, which is only possible for static signals with scanning times of several seconds for an SEM image. Figure 9 shows a correlation between static potentials and the transistor positions in the cross-section view, indicating the relationship between them. If dynamic signals are imaged, and local potentials change during the scanning time, a gray value depending on the duty cycle of the dynamic signal can be observed, as shown in Fig. 10 for different frequencies. This average value allows an easy localization of dynamic signals in an E-beam probing image. Dynamic signals could be visualized in the time domain by sample switching to spot mode, as shown in Fig. 10.

Comparing the results of optical and E-beam techniques, it is observed that optical techniques are limited to higher frequencies. Even for a frequency of 100 kHz, it is almost impossible to detect the signal out of the noise using optical techniques for the device under test. However, E-beam works well at all frequencies and provides clear images of the IC structures with higher resolution compared to optical techniques. Typically, an electrostatic beam blanker operates with a frequency range of 5-20Mhz. However, there are techniques available to overcome this limit, such as employing specific scan mechanisms coupled with undersampling techniques. For instance, in [15], measurements at 2GHz have been demonstrated using a Meridian E platform from Thermos Fisher Scientific (TFS). Current developments indicate that measurements up to 4 GHz range are achievable. This means the potential measurement frequency is high enough for current device technologies, thus not limiting the utilization of E-beam probing.

Although E-beam probing offers advantages over optical techniques, it also presents some drawbacks. One such drawback is that performing e-beam probing requires the sample to be thinned to the STI level. Thinning and opening trenches to the STI level pose several challenges, including thinning parallel to the structural elements, accurate determination of the endpoint, Controlling the size and geometry of the trench presents, and maintaining the device's integrity during sample preparation.

Furthermore, when a silicon substrate is very thin, typically a few microns or even less, heat dissipation becomes a critical concern. Thicker silicon dissipates heat generated within the IC more effectively through conduction and convection. However, thin silicon substrate has a limited capacity to absorb and dissipate heat efficiently, leading to localized overheating and potentially damaging temperature. High temperatures can induce changes in electrical properties and even physical damage to the IC components. Temperature variations can also induce mechanical stress in the silicon substrate, resulting in mechanical failures such as cracks, or warping of the substrate. Figure 11 illustrates the back surface of an IC where the silicon substrate was thinned down to 25 µm. After several cycles of IC operation, the silicon substrate develops cracks, resulting in the detachment of a piece of silicon. Consequently, the device failed due to the damage incurred.

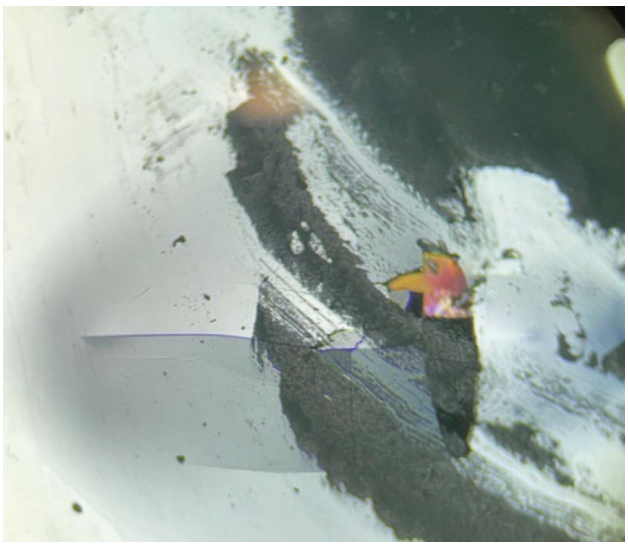

Fig. 11. Damage on the silicon back surface after thinning

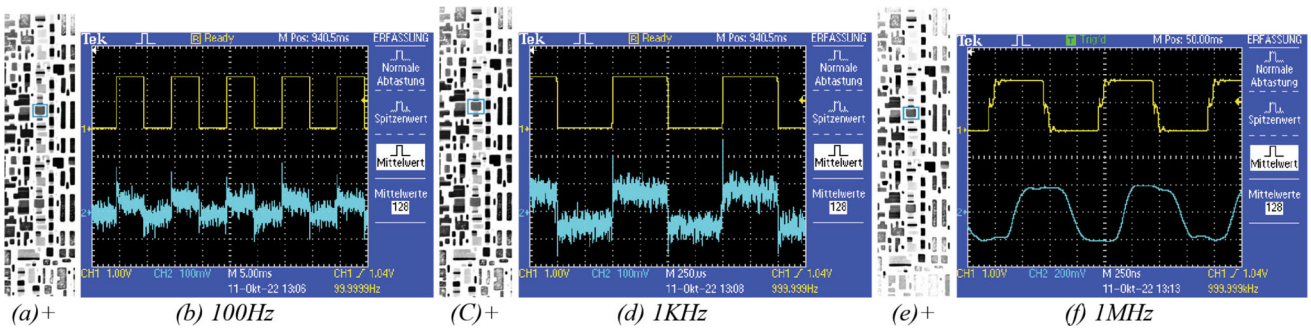

Fig. 10. E-beam images at different frequencies

Table 1 Comparative assessment of optical and E-beam techniques for IC signal tracking

Measures	Techniques	
	Optical techniques (PEM, EOFM, EOP)	E-beam probing
Technology node	$\geq$ 12 nm	$\geq$ 1 nm
Image quality	Limited in the resolution	Very clear image
Sample preparation	Access to the silicon back surface is enough.	Requires aggressive thinning and trenching to the STI level
Frequency	Limited to higher frequencies.	No limitation
	Required to be known for EOFM.	

Conclusions

This work assesses the requirements for optical and electron based contactless probing on the IC structure through the chip backside. It has been shown that the optical techniques are limited to high frequencies, and the signal strength weakens when the toggling frequency is decreased. So, these methods may be ineffective for low-frequency applications, whereas e-beam probing is very successful in imaging and acquiring the signals even for frequencies as low as 100 Hz. While for conducting optical techniques through the chip backside, accessing the silicon back surface is mostly enough, or depending on the application, a simple mechanical thinning of the silicon might be required. Conversely, E-beam probing requires aggressive thinning and trenching to the STI level so that the secondary electrons that show the voltage contrast can leave the IC back surface. However, this surface preparation needs only to be made in the area of interest, and the rest of the device can remain intact. Thinning down to the STI level is very critical and thin silicon may not dissipate the generated heat within the IC efficiently. This heat IC can cause changes in electrical properties and even physical damage to the IC components. A summary of the assessment is presented in Table 1.

All in all, even with shrinking feature sizes and downscaled supply voltages, E-beam probing is capable of imaging and acquiring the voltage waveforms of the nodes with a spatial resolution of about 1 nm. Therefore, more attention needs to be paid to the threat posed by this technique. Hence, to ensure the security of the devices against these attacks, IC backside needs to be protected. Any countermeasure designed to protect the IC against attacks through the chip back surface, particularly attacks involving silicon thinning, can effectively prevent E-beam probing. Examples of such countermeasures include backside polishing detector [17], active coating on the backside [18, 19], or backside shield [20].

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