Low Loss Chip-to-Chip Couplers for High Density Co-Packaged Optics

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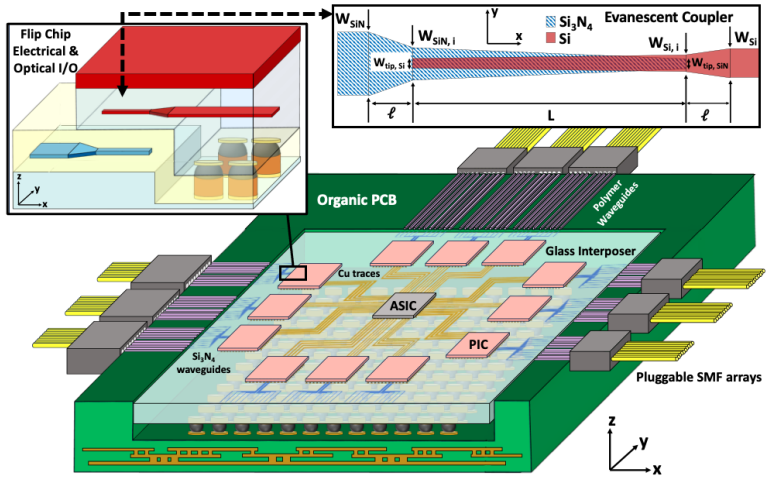
Abstract: An experimentally demonstrated, vertical chip-to-chip evanescent coupler between silicon nitride (Si_3N_4) and silicon (Si) is presented with the coupler loss measured to be 0.39 ± 1.06 dB at 1550 nm with a 1-dB bandwidth of 160 nm extending across the C-band, S-band, and L-band (1480-1640 nm). The average coupling loss was determined to be 0.73 dB for the 1480-1640 nm wavelength range with a ± 2σ tolerance of ± 0.92 dB. The 1-dB lateral alignment tolerance was 1.56 ± 0.14 μm at 1550 nm and the average tolerance was 1.38 ± 0.24 μm across the 1480-1640 nm wavelength regime. In addition, the average coupling loss varied by less than ± 0.35 dB and the average 1-dB alignment tolerance varied by less than ± 30 nm for temperatures varying from 23-60°C. Finally, the average coupling loss range was less than 1.5 dB range across four sets of identically packaged die. This is the first experimental demonstration of an inter-chip, passively assembled evanescent coupler using standard CMOS foundry processes for directly coupling between Si and Si_3N_4, overcoming a waveguide refractive index difference of Δn = 1.32 without requiring taper tip widths of less than 100 nm.

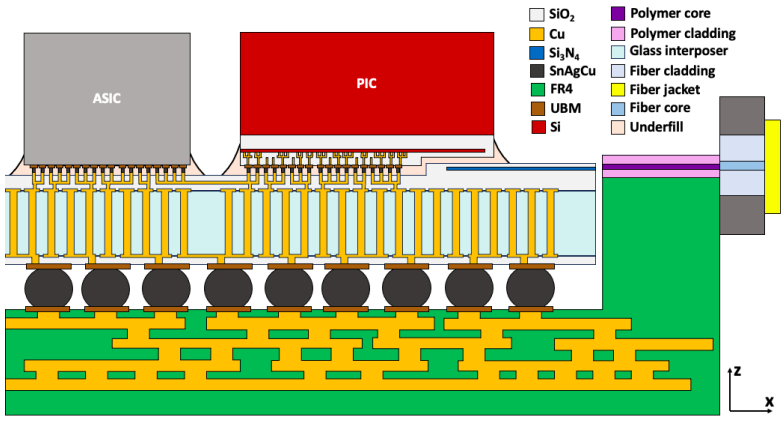
1. Introduction

By 2025, the global datasphere is estimated to grow to 175 ZB, with 46% of the world's stored data residing in public cloud environments [1]. To meet demand, data center top of rack (ToR) switch packages have doubled total bandwidth capacity every two years, with 51.2 Tbps ToR switch packages using 512 electrical input/output (I/O) channels, each operating at 106.25 Gbps per lane using the IEEE 802.3-ck standard, being commercially available [2, 3]. Further standardization of 200 Gbps per lane is already underway [4, 5]. However, the power consumed by centimeter long board level Cu traces and the limited pluggable transceiver pitch make continued scaling difficult [6, 7]. This is critical when considering the energy consumption of data centers. For example, data centers already accounted for 18% of all energy consumption in Ireland in 2022 and by 2031 roughly 15% of Denmark's energy consumption will be due to data center power usage [8].

The need to reduce Cu length has forced a transition to co-packaged optics (CPO) where the photonic integrated circuit (PIC) is on the same package substrate as the application specific integrated circuit (ASIC). Scaling using this architecture has its own challenges, such as the active alignment and bonding of bulky single mode fiber (SMF) arrays to PICs using UV-curable epoxies, increasing cost and limiting throughput. This problem is underscored by the fact that photonic packaging, assembly, and testing occupies 70-80 % of the total cost of PIC manufacturing [10–13]. The assembly challenge is further compounded by the potential need for > 10^3 SMFs to scale to Pbps bandwidth capacities by 2035 as required by current trends [2]. The limited PIC shoreline cannot be ignored either considering that SMFs operating near datacom (1310 nm) or telecom



(a)



(b)

Fig. 1. Schematics showing a CPO design scalable to Pbps I/O. In (a) a 3D view of the glass interposer with fully integrated optical I/O is shown. The callouts highlight the interposer-to-die evanescent coupler design from [9]. In (b) a cross section showing the optical and electrical fanout. The top and bottom side SiO_2 is colored differently to represent the redistribution layers deposited after through-glass-via (TGV) formation.

(1550 nm) wavelengths typically have minimum pitches of 127 μm, meaning a maximum density of only 8 fibers/mm is possible.

A scalable solution is to use integrated waveguide-to-waveguide couplers which connect PICs to interposers and interposers to boards. This solution increases optical I/O density at the die level while enabling higher fiber counts through optical fan-out by shifting the fiber interface to the edge of the interposer or board where there is a larger available shoreline. In addition, this solution allows for the passive assembly of PICs using automated pick-and-place technology where simultaneous electrical and optical connections could be made without active alignment or flyover fiber arrays [14]. A variety of prototypes illustrating the use of waveguide-to-waveguide couplers in CPO modules have been demonstrated [11, 15–17]. For example, in [18–21], a design using a glass interposer including TGVs and evanescent Si_3N_3-to-IOX waveguide couplers allowed for optical and electrical fan-out to SMF arrays and board level solder bumps. Others

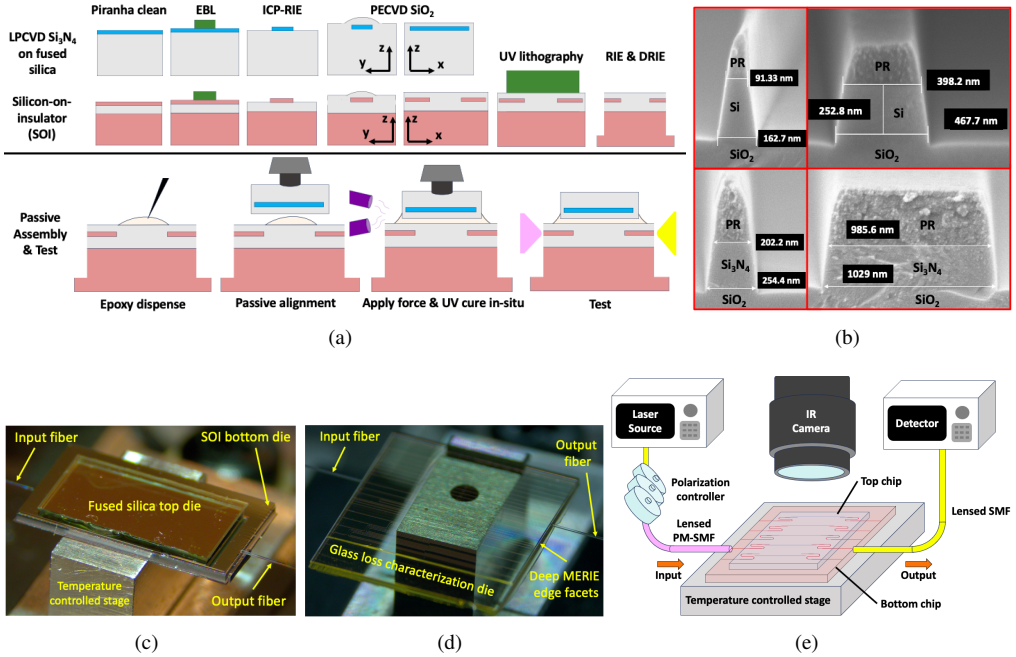


Fig. 2. Images detailing the fabrication process. In (a), the process flow used to fabricate and package the chip-to-chip coupling prototypes. In (b), cross sectional SEM images show the minimum and maximum feature sizes for the SOI and Si_3N_4. In (c) and (d), the chip-to-chip prototype and separate glass chip on the testing stage. In (e), a schematic of the testing setup.

have used polymer waveguides on organic package substrates with embedded SOI die to achieve optical fan-out and passive assembly [22–24], while separate proposed approaches make use of embedded glass die in organic substrates [25]. Prototypes using evanescent couplers have also been used on Si interposers to connect thin Si_3N_4 interposer waveguides with thin Si_3N_4 PIC waveguides with simultaneous Au-Au bonding for electrical connections [26].

To this end, an evanescent coupler design was previously presented in [9] which direct coupled between SOI PIC waveguides and interposer Si_3N_4 waveguides, allowing for lateral footprints at roughly an order of magnitude better that of polymer or IOX systems (and two orders of magnitude better than a SMF) due to the high refractive index contrast. This coupler was only one aspect of the broader 2.5D CPO design shown in Figure 1. Development of two technologies make this CPO design possible: a novel interposer-to-die evanescent coupler and a novel board-to-interposer expanded beam coupler. This study focuses on the fabrication, packaging, and testing of the evanescent coupler while the expanded beam coupler will be presented in future studies. Experiments were performed which measured the coupling loss, 1-dB and 3-dB lateral alignment tolerances, 1-dB wavelength tolerance, thermal stability, and repeatability across multiple packaged die. Moreover, Section 2.1 describes the prototype fabrication and packaging, Section 2.2 depicts the testing setup and mask layout, Section 3 presents the collected data, and Section 4 provides takeaways and a comparison to similar designs.

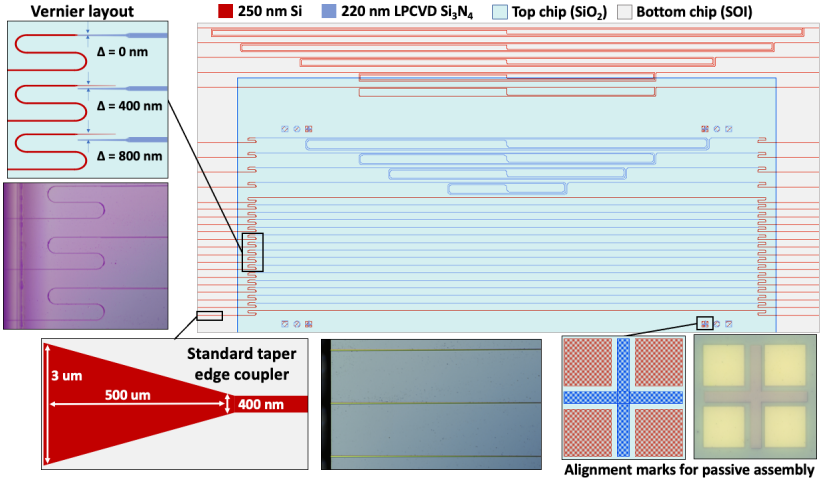


Fig. 3. The mask design showing chips in their post-bond positions. Key features include the Vernier layout, standard taper SOI edge couplers, and alignment features for sub-micron passive assembly.

2. Materials and Methods

2.1. Waveguide fabrication and packaging

For our interposer-to-die coupling prototype, the material for the upper chip was 500 μm thick fused silica with 220 nm Si_3N_4 grown using low pressure chemical vapor deposition (LPCVD) and the material of the lower chip was SOI with a 250 nm device layer and 5 μm buried oxide (BOX). While glass was the material of the interposer in our design, it was chosen to be the material of the die in this prototype in order to verify alignment accuracy during bonding, especially because this choice did not impact measurements of evanescent coupler performance. Waveguides were patterned using electron beam lithography (Elionix 50 keV HS-50) with a diluted AZ nLoF 2020 photoresist using the simplified fabrication process laid out in Figure 2(a) (see Section 1.A and 1.B of Supplemental 1). The 220 nm Si_3N_4 and 250 nm SOI on a films were etched using inductively coupled plasma reactive ion etching (ICP-RIE) on a Samco RIE-230iP. The cross sectional scanning electron microscope (SEM) images shown in Figure 2(b) demonstrate the minimum and maximum features sizes for the glass and SOI waveguides matching design values from [9] after ICP-RIE, but prior to photoresist removal. Following photoresist removal, the die and substrate were cladded with a 500 nm SiO_2 cladding using plasma enhanced chemical vapor deposition (PECVD) on a Samco PD220NL tool and annealed for 2 hours at 1000°C to remove excess hydrogen. The SOI required additional processing to form the edge facets prior to dicing (see Section 1.B of Supplemental 1). To form the facets, 5.7 μm thick AZ nLoF 2035 photoresist was patterned using 375 nm direct write UV lithography on a Heidelberg MLA 150 tool. Then, the 5 μm BOX layer was etched through using magnetically-coupled RIE (MERIE) on an Applied Materials Precision 5000 tool and the bulk Si was etched through using deep reactive ion etching (DRIE) on a STS Pegasus Pro ICP tool. The trench depth after DRIE was approximately 150 μm deep. The wafers were then diced to form approximately 9.1 mm by 5 mm glass die and 11 mm by 6.3 mm SOI substrates.

The packaging procedure consisted of using a 27 gauge syringe needle to apply a droplet of NOA61 UV curable epoxy to the center of the SOI chip [27]. Bonding was performed using a Finetech FINEPLACER® femto 2 high speed pick and place die bonder through passive alignment with machine vision only [28]. The alignment process involved passively locating the

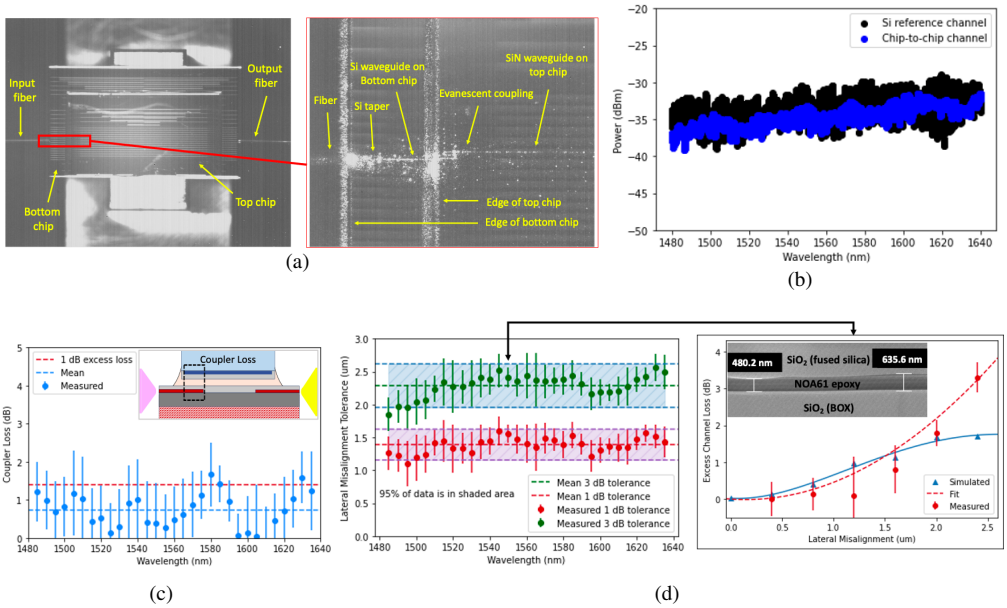


Fig. 4. Measured data for the evanescent chip-to-chip coupler. In (a), a top view using the IR camera showing 1550 nm light evanescently coupling between the two chips. In (b) the raw data is shown for a straight through Si channel and chip-to-chip channel. In (c), coupling loss is shown as a function of wavelength for one of the best-aligned channels. The red dotted line represents 1 dB of excess loss from the 1550 nm coupling loss. In (d) the 1-dB and 3-dB lateral alignment tolerances are shown, with the dashed line representing the average tolerance from 1480-1640 nm. The shaded zones represent $\pm\ 2\sigma$ from the average. On the right of (d), excess loss versus lateral misalignment is shown for 1550 nm light alongside 3D-EME simulation results.

alignment marks' centers on the SOI and placing the glass die with respect to those positions, allowing for sub-micron flip-chip bonding precision. The flip-chip bonding step also included the application of 40-100 N of force, during which the epoxy was cured in situ using a UV lamp pointed at the side of the die-substrate system. Cross sectional SEM measurements on bonded dummy samples showed epoxy bond line thicknesses on the order of 0.48-0.64 μm. The images found in Figure 2(c) are of the final packaged die positioned on the optical testing stage. Lastly, a separate Si_3N_4-on-fused silica chip was fabricated as a means of independently verifying the Si_3N_4 propagation and bending losses. The process flow for this chip was identical to that described above except for the cladding thickness, anneal time, and edge facet process (see Section 1.C in Supplemental 1). Specifically, the PECVD SiO_2 cladding thickness was increased to 2 μm instead of the 500 nm used for the chip-to-chip packages and the anneal time was increased to approximately 10 hours instead of 2 hours. Defining the glass edge facets involved patterning 44 μm thick AZ nLoF 2070 resist using 375 nm direct write UV lithography and etching using MERIE to achieve an SiO_2 trench depth of approximately 68 μm.

2.2. Device layout and testing

A schematic for the layout of the chip-to-chip coupling die and substrate after packaging can be found in Figure 3 (see Section 2.A and 2.B of Supplemental 1 for more details regarding the chip-to-chip prototype layout and glass loss die layout, respectively). The chip-to-chip evanescent coupler in this study used the optimized dimensions discussed in [9]. A Vernier waveguide layout

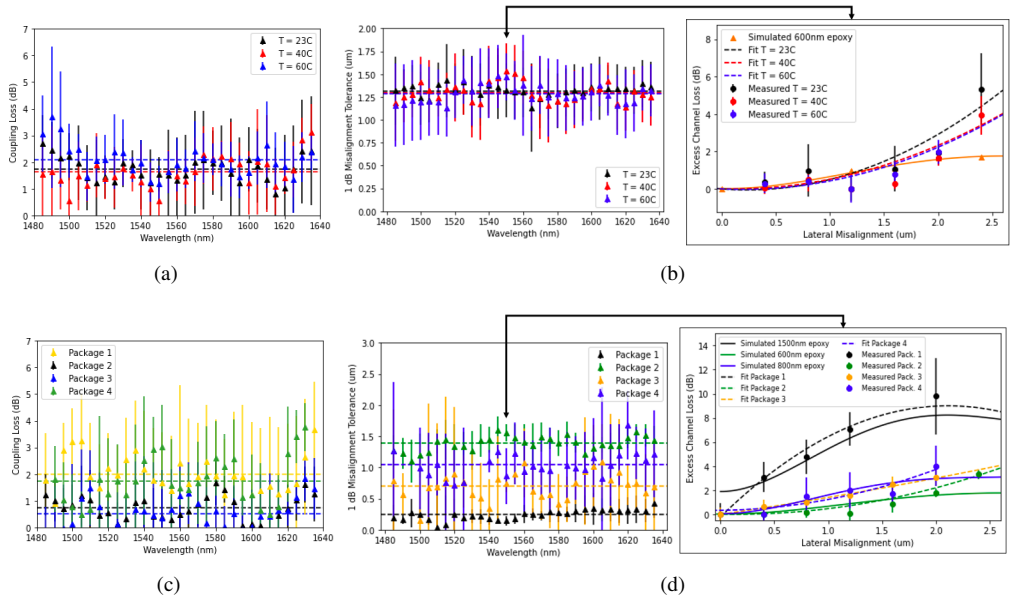


Fig. 5. Measured data showing the impact of temperature and repeatability across multiple packages. In (a) the dashed lines represent the mean coupling loss from 1480-1640 nm for each temperature while in the left plot of (b), they represent the mean 1-dB alignment tolerance for each temperature. Note that Package 2 was used for obtaining the thermal data. In (c) and (d), the dashed lines represent the same quantities, except for different packages instead of different temperatures.

was used to measure lateral alignment tolerance and post-bond alignment accuracy to within 400 nm precision. In the Vernier waveguide layout, the 14 Si waveguides on the substrate had a constant pitch of 127 μm while the 14 Si_3N_4 waveguides on the die had a constant pitch of 127.4 μm. Testing of the devices was done using a MapleLeaf Photonics system (see Section 3 of Supplemental 1 for more details). The testing setup consisted of a 1480-1640 nm laser injecting 1 mW of light into an SMF which connected to a polarization maintaining (PM), tapered, lensed fiber (8 μm core, 125 μm cladding, 3 μm working distance). The PM-SMF went through three polarization panels before being stripped and connected to a piezoelectric stage near the edge of the package. Light travelled from the PM-SMF to the SOI waveguides and then to the Si_3N_4 waveguides using the vertical coupler, and then back down onto the SOI using a second vertical coupler where it was collected using an edge coupled tapered, lensed SMF. The light was then fed into a photodetector with a lower limit sensitivity of -70 dBm. The testing stage could also be temperature controlled from room temperature (approximately 23°C) to a maximum of 60°C; therefore, all waveguides were re-measured at three different temperatures: 23°C, 40°C, and 60°C. Lastly, in order to determine coupler reproducibility, four sets of identically fabricated and packaged samples were measured.

3. Results

The image in Figure 4(a), taken using the mounted IR camera, shows chip-to-chip coupling near 1550 nm by focusing through the back of the glass top chip. A plot showing the raw measured wavelength response from 1480-1640 nm for one of the best aligned chip-to-chip channels alongside the lowest loss Si straight through channel is shown in Figure 4(b). The plot in Figure 4(c) shows the evanescent coupling loss across the 1480-1640 nm wavelength

regime for one of the best aligned channels (see Section 4.A of Supplemental 1 for details on how chip-to-chip coupling was extracted). The average coupling loss across the 1480-1640 nm wavelength window for this channel was 0.73 dB, with 95% of the data falling within ± 0.92 dB (± 2σ) of this value. Likewise, the coupling loss at 1550 nm was calculated to be 0.39 ± 1.06 dB. Finally, the 1-dB bandwidth was determined to be 160 nm based on the fact that over 90% of the coupling loss data fell within ± 1 dB of the loss at 1550 nm, and the fact that 100% of the data fell within ± 1 dB of the average coupling loss across the 1480-1640 nm wavelength spectrum.

Analysis was also done to determine the 1-dB and 3-dB lateral alignment tolerances, beginning with the normalization of each chip-to-chip channel to the best aligned chip-to-chip channel, determined to be the 11th chip-to-chip channel from the bottom of the mask (see Section 4.B of Supplemental 1 for full alignment tolerance analysis). This indicated the passive pick-and-place accuracy for this set of chips was approximately 0.4 μm in the lateral direction. A plot showing the excess channel loss as a function of the lateral misalignment at 1550 nm wavelength, alongside 3D Eigenmode Expansion Method (EME) simulation data, can be found on the right side of Figure 4(d). The 1-dB and 3-dB lateral alignment tolerances for 1480-1640 nm are shown in the plot on the left side of Figure 4(d). The average 1-dB alignment tolerance across the 1480-1640 nm wavelength regime was ± 1.38 μm, with 95% of the measured data falling within a ± 0.24 μm span (± 2σ) of this value. Likewise, the average 3-dB alignment tolerance was ± 2.29 μm with a 2σ span of ± 0.34 μm. Finally, the maximum 1-dB alignment tolerance was 1.60 ± 0.23 μm and the maximum 3-dB alignment tolerance was 2.52 ± 0.26 μm, with both occurring at 1545 nm wavelength.

The same analysis described above was performed on the data obtained at the three different temperatures: 23°C, 40°C, and 60°C. The results for coupler loss can be found in Figure 5(a) and the results for lateral alignment tolerance can be found in 5(b), alongside 3D EME simulation data for 600 nm thick NOA61 epoxy (which was run using room temperature conditions). The average coupling loss from 1480-1640 nm with uncertainty (i.e. one standard deviation) was 1.73 ± 0.46 dB, 1.62 ± 0.55 dB, and 2.08 ± 0.56 dB for 23°C, 40°C, and 60°C, respectively. The average 1-dB alignment tolerance from 1480-1640 nm with uncertainty was 1.32 ± 0.13 μm, 1.30 ± 0.21 μm, and 1.28 ± 0.19 μm for 23°C, 40°C, and 60°C, respectively. The plots of coupling loss and alignment tolerance for the four different packaged die can be found in Figure 5(c) and 5(d), respectively. The average coupling loss from 1480-1640 nm with uncertainty was 2.00 ± 0.66 dB, 0.72 ± 0.46 dB, 0.51 ± 0.68 dB, and 1.88 ± 1.04 dB for Package 1, Package 2, Package 3, and Package 4, respectively. The average 1-dB alignment tolerance from 1480-1640 nm with uncertainty was 0.24 ± 0.16 μm, 1.38 ± 0.24 μm, 0.71 ± 0.42 μm, and 1.05 ± 0.40 μm for Package 1, Package 2, Package 3, and Package 4, respectively. Note that Package 2 was the package used for Figures 4, 5(a), and 5(b).

4. Discussion

Based on the results presented in Section 3, there are several important trends to note, beginning with the wavelength dependencies for the plots in Figure 4. The coupling loss, as well as the 1-dB and 3-dB lateral misalignment tolerances, show little wavelength dependence between 1480-1640 nm, as indicated by the fact that 95% of the data from Figure 4(d) falls within ± 0.24 μm of the mean and 90% of the data from Figure 4(c) is within ± 0.5 dB of the mean. A second point to discuss about Figure 4 is how the measured data correlated with the 3D-EME simulations. From Figure 4(d), the difference between the simulated data and the fit line of the measured data at 1550 nm was less than 0.1 dB for misalignments of 1.5 μm or less and was less than 0.75 dB for misalignments of 2 μm or less. The divergence by more than 0.75 dB for misalignments of 2 μm or more can be explained by the absorption in the PECVD SiO_2 cladding and any absorption within the NOA61 epoxy (see Section 5.A of Supplemental 1 for details related to propagation losses and PECVD absorption). As the tapers were increasingly misaligned, the expanded mode

Table 1. Summary of silicon based waveguide-to-waveguide evanescent couplers designed for chip-to-chip connections in chronological order of publication date. The rows shaded blue indicate only simulation results were reported.

Package	CL_{1550} (dB)	1-dB Tolerance (μm)		1-dB BW (nm)	LxW (μm)	Ref.
		Lateral	Vertical			
SOI to polymer	0.4 (TE)	± 3	/	± 100 (1550)	200x5	[29]
SOI to polymer	0.4 (TE/TM)	2	1.5	100 (1470-1570)	1750x5.915	[11, 15]
Si_3N_4 to Si_3N_4	3.1	< ± 1	< 1	/ (1550)	500x3	[30]
Si_3N_4 to Si_3N_4	0.76	± 2	< 1	/ (1550)	500x3	[31]
SOI to polymer	1.25/0.5 (TE/TM) < 0.5 (TE/TM)	± 2 /	/	± 60 (1310) ± 70 (1550)	1500x6.5	[32–34]
SOI to polymer	0.2	> ± 5 ± 1.5° (yaw)	0.5	± 100 (1550)	200x15.3	[35]
SOI to IOX	< 1 (TE/TM)	± 4	3	± 30 (1550)	1500x12	[18]
Si_3N_4 to IOX	0.7	> ± 4	< 2	75 (1515-1590)	2000x11	[21]
Si_3N_4 to Si_3N_4	0.54	< ± 2	< 0.8	400 (1200-1600)	1000x3	[26]
SOI to Si_3N_4	**0.39 (TE)**	**± 1.56**	**> 1.1**	**160 (1480-1640)**	**520x1**	**this work**

CL_{1550} = coupling loss at 1550 nm wavelength
BW = bandwidth
/ = not reported

traveling through the taper interacted with the SiO_2 cladding and epoxy significantly more than when the opposing high index taper was situated directly above it.

Furthermore, from Figure 5(a), the average coupling loss from 1480-1640 nm varied by less than ± 0.35 dB from 23°C to 60°C. Considering a single standard deviation about the mean for room temperature coupling is ± 0.46 dB, the data indicates the evanescent coupling is very weakly dependent on temperature. Similarly, the data from Figure 5(b) shows that the 1-dB lateral alignment tolerance varied by less than ± 30 nm from 23°C to 60°C. The low impact of temperature can be explained by treating the glass-epoxy-silicon package similar to the linear thermal expansion of a composite material system (see Section 5.B of Supplemental 1 for detailed thermal analysis). In this simplified system, a film with a high coefficient of thermal expansion (CTE) is connected to two separate low CTE films, one above and one below. When using this model with a $\Delta T = 40°C$, the calculated lateral misalignment was 0.12-0.55 μm with a calculated vertical misalignment of less than 10 nm. Based on the results shown in Figure 5(b) and 4(d), the 0.12-0.55 μm lateral misalignment due to thermal expansion should weakly impact coupling efficiency - a hypothesis confirmed by the data in 5(a).

Additionally, from Figure 5(c) it can be seen that the average coupling loss from 1480-1640 nm varies by less than 1.5 dB from the minimum of 0.51 dB (Package 3) to a maximum of 2.00 dB (Package 1). The average coupling loss when combining the data from all four packages across all measured wavelengths (1480-1640 nm) was 1.28 dB with a standard deviation of ± 0.98 dB, while the average coupling loss at 1550 nm was 1.36 dB with a standard deviation of ± 1.09 dB. The average coupling loss at 1550 nm is substantially increased by the 3.02 ± 1.56 dB coupling loss at 1550 nm for Package 4. For Packages 1-3, the average coupling loss at 1550 nm was 0.81 dB with a standard deviation of ± 0.61 dB. Similarly, Packages 2-4 show a tightly bound 1-dB lateral alignment tolerance with the average calculated after combining the data from these three packages being ± 1.05 μm with a standard deviation of ± 0.35. The lower alignment tolerance of Package 1, shown in black in Figure 5(d), can be explained by a larger epoxy thickness compared to the other packages. Based on how the 3D-EME simulation data correlates with the measured data in the callout of Figure 5(d), the epoxy thickness for Package 1 is 0.7-0.9 μm larger than for Packages 2-4, meaning the total taper separation is approximately 2-2.25 μm compared to 1.1-1.8 μm for the other packages. As a result, the average alignment tolerance is only ± 0.24 μm.

Despite the larger thickness, the coupler still performed well as evidenced by the 2.00 ± 0.66 dB average coupling loss and 1.67 ± 1.90 dB coupling loss at 1550 nm as shown in Figure 5(c).

Lastly, we can compare the performance of this evanescent chip-to-chip coupler to other inter-chip evanescent couplers by analyzing the data in Table 1. The evanescent coupler presented in this work is the first demonstration of direct inter-chip coupling between SOI waveguides and other Si based waveguides. This coupler demonstrated a coupling loss of 0.39 dB at 1550 nm, the lowest reported for an evanescent inter-chip coupler between Si based waveguides. This was made possible through the strategic use of relatively thick films with high refractive indices to minimize scattering losses from abrupt refractive index changes occurring near the waveguide cladding, such as at the edge of the top chip or epoxy bond line. For the 1-dB lateral alignment tolerances, the coupler presented in this work demonstrated an average of ± 1.38 μm from 1480-1640 nm with a maximum of ± 1.60 μm at 1545 nm. This lateral alignment tolerance is large enough to enable passive assembly using automated pick-and-place tools designed for high volume manufacturing [28, 36]. In addition, this coupler was roughly a third of the typical length, and 10%-20% of the typical width, versus comparable designs. This was done while maintaining a vertical taper-to-taper distance greater than 1.1 μm which aids in making the design compatible with typical BEOL layer thicknesses. The combination of these advantages demonstrate the usefulness of this coupler for scaling to Pbps I/O in integrated photonic systems.

5. Conclusion

A vertical chip-to-chip evanescent coupler between Si_3N_4 and SOI was experimentally demonstrated for the first time with a coupling loss of 0.39 ± 1.06 dB at 1550 nm wavelength and an average coupling loss of 0.72 ± 0.46 dB across the C-band, S-band, and L-band (1480-1640 nm). The coupler had an average 1-dB lateral alignment tolerance of 1.38 ± 0.12 μm for the 1480-1640 nm wavelength range, making it possible to assemble passively using automated pick-and-place technology. In addition, thermal stability was explored and variation of less than ± 0.35 dB and ± 30 nm for coupling loss and alignment tolerance was observed for operation from 20-60°C. Finally, repeatability of the observed results was highlighted by showing similar performance across four sets of separately packaged die.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Supplemental document. See Supplemental 1 for supporting content.

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