Polymeric Semiconductor in Field-Effect Transistors Utilizing Flexible and High-Surface Area Expanded Poly(tetrafluoroethylene) (ePTFE) Membrane Gate Dielectrics

Christopher R. Bond[1], Howard E. Katz*[1], Daniel J. Frydrych[2], David B. G. Rose[2], Daniel Miranda[2]

[1] Department of Materials Science and Engineering, Johns Hopkins University, Baltimore, MD 21218 USA

[2] W.L. Gore and Associates, Elkton, MD 21922 USA

*corresponding author; email hekatz@jhu.edu

Abstract

Organic field-effect transistors (OFETs) were fabricated using three high-surface area and flexible expanded-poly(tetrafluoroethylene) (ePTFE) membranes in gate dielectrics, along with the semiconducting polymer poly[2,5-bis(2-octyldodecyl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione-3,6-diyl)-alt-(2,2';5',2'';5'',2'''-quaterthiophen-5,5'''-diyl)] (PDPP4T). The transistor behavior of these devices was investigated following annealing at 50°C, 100°C, 150°C, and 200°C, all sustained for 1 hour. For annealing temperatures above 50°C, the OFETs displayed improved transistor behavior and a significant increase in output current while maintaining similar magnitudes of V_{th} shifts when subject to static voltage, compared to those kept at ambient temperature. We also tested response to NO_2 gas as further characterization and for possible applications. The ePTFE-PDPP4T interface of each membrane was characterized via scanning electron microscopy (SEM) for all four annealing temperatures to derive a model for the hole mobility of the ePTFE-PDPP4T OFETs that accounts for the microporous structure of the ePTFE and consequently adjusts the channel width of the OFET. Using this model, a maximum hole mobility of 1.8±1.0 $cm^2/V{\cdot}s$ was calculated for the polymer in an ePTFE-PDPP4T OFET annealed at 200°C whereas a PDPP4T OFET using only the native silicon wafer oxide as a gate dielectric exhibited a hole mobility of just 0.09±0.03 $cm^2/V{\cdot}s$ at the same annealing condition. This work demonstrates that responsive semiconducting polymer films can be deposited on nominally nonwetting and extremely bendable membranes, and the charge carrier mobility can be significantly increased compared to their as-prepared state by using thermally durable polymer membranes with unique microstructures as gate dielectrics.

Keywords: polymer transistor, expanded poly(tetrafluoroethylene), PDPP4T, thermal stability, charge retention, vapor response

Introduction

Organic electronic devices based on flexible materials are promising candidates for a wide variety of applications such as chemical and biological sensors[1,2,3,4], flexible displays[5,6], and wearable electronics that can be made conformable to the human body[7,8]. Organic field-effect transistors (OFETs) are a type of electronic device commonly studied to investigate the threshold voltage, charge storage behavior, and charge carrier mobility associated with organic dielectrics

in combination with organic semiconductors to help determine their most appropriate applications. Organic dielectrics and semiconductors are commonly either solution or thermally processible, making them easy to modify and process for the fabrication of low-cost electronic devices. While the low cost, flexibility, and ease of processibility are key benefits of organic electronic devices, they lack the same magnitude of charge carrier mobility exhibited by traditional inorganic devices, despite the frequent emphasis on the design and synthesis of various novel semiconducting polymers[9,10,11], and manipulating the microstructure of the gate dielectric for this purpose[13,14]. Hole mobilities of the best solution-processed organic semiconductors used in OFETs are commonly on the order of just 1 to 10 $cm^2/V \cdot s$[15,16] and are orders of magnitude smaller than the hole mobility of silicon at 480 $cm^2/V \cdot s$[17]. Silicon also exhibits an electron mobility several times higher than its hole mobility at 1350 $cm^2/V \cdot s$[17], making it a preferred choice for traditional high-performance electronic devices.

Poly[2,5-bis(2-octyldodecyl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione-3,6-diyl)-alt-(2,2';5',2'';5'',2'''-quaterthiophen-5,5'''-diyl)] (PDPP4T) is a well-studied semiconducting polymer that exhibits a relatively high hole mobility,[43] with OFET mobilities of PDPP4T derivatives as large as 9.1 $cm^2/V \cdot s$ reported by Yang et al[18] as well as Ma et al[41] under certain conditions. PDPP4T is a desirable OFET semiconductor due to its ease of processing, high thermal stability, and high hole mobility. The polymer is solution processible in many organic solvents such as chloroform and 1,2-dichlorobenzene, making it highly compatible with a wide variety of substrates and organic gate dielectrics used in the design and fabrication of top-contact bottom-gate OFETs. As will be discussed below, we use the polymer herein to form semiconducting films on an especially flexible, low-polarity, and high-surface area membrane substrate, on which it is particularly challenging to form continuous charge-transport pathways.

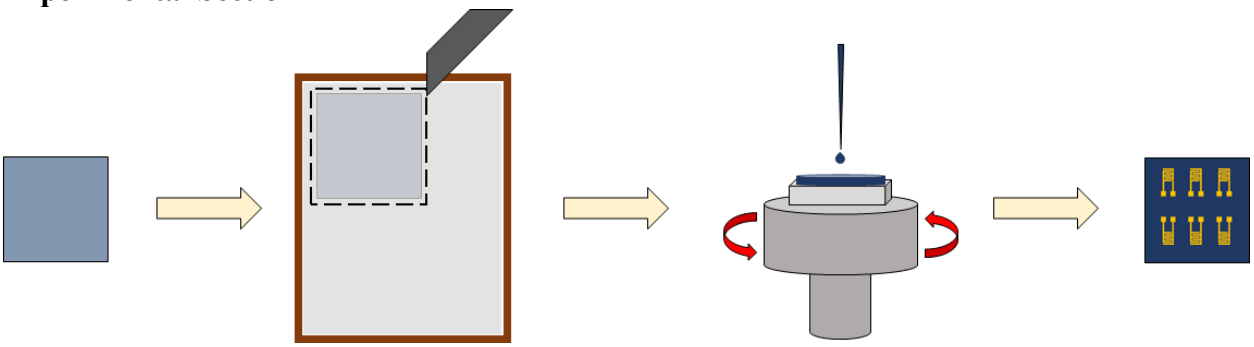
One example of a gate dielectric commonly utilized in OFETs is polystyrene (PS), which exhibits the beneficial characteristics of organic materials previously mentioned. PS is soluble in many different organic solvents and has been well studied as a gate dielectric in OFETs due to its thermal stability[19,42]. In addition to PS, fluorinated polymer dielectrics such as poly(perfluorobutenylvinylether) (CYTOP)[20,21,42] and Teflon® AF[22,43,44] have been investigated in OFETs due to their insensitivity to water and advantageous thermal stability. CYTOP or Teflon® AF gate dielectrics have been used in solution- or thermally processed OFETs, microporous expanded- poly(tetrafluoroethylene) (ePTFE) membranes have never been investigated as gate dielectrics in OFETs.

In contrast with PTFE, ePTFE is an air-permeable and microporous membrane that has been processed to generate a unique microstructure that is desirable for various applications. Many studies utilizing ePTFE in biomedical devices have been conducted due to its biocompatibility and high strength-to-weight ratio, making it an attractive material in the medical field. Examples of the use of ePTFE in biomedical devices include tissue regeneration membranes and vascular grafts[23,24,25], ePTFE-coated stents[26,27], and prostheses[28,29]. In addition to its widespread use in biomedical devices, ePTFE has also been studied in composite membranes for use in durable and high-temperature stable fuel cells[30,31]. Based on the many attractive properties of ePTFE membranes and the existing use of Teflon® AF and CYTOP as gate dielectrics in OFETs, it is surprising that the use of ePTFE membranes in OFET gate dielectrics has never been investigated. The flexibility and hydrophobicity of the membranes along with the ability to tune properties such

as their dielectric constant, surface energy, molecular absorptivity, charge retention, and stiffness through their unique microstructure provides enticing possibilities for the development of free-standing, flexible, high-performance, biocompatible electronic devices.

In this work, ePTFE membranes with three different microstructures are used in gate dielectrics in top-contact bottom-gate PDPP4T-based OFET devices. Their output and transfer characteristics are measured immediately after device fabrication, and threshold voltage (V_{th}) shifts are measured after applying a –70 V bias to the source and drain electrodes for five minutes. The devices are then exposed to NO_2 gas in a chamber at concentrations of 1, 2, 5, and 10 ppm for 3 minutes each and measured between exposures to each concentration to determine the sensitivity and signal-to-drift ratio at each concentration, as a further indication of thermal stability and possible applicability, taking advantage of the high surface area. Upon the completion of these tests, the OFETs are then annealed at either 100°C, 150°C, or 200°C in a ceramic oven for 1 hour and all previously mentioned tests are repeated under the same conditions to measure the thermal stability and any performance changes. The transfer behavior of the OFETs along with SEM micrographs of the ePTFE-PDPP4T surface are used to develop a model for the hole mobility that accounts for the pores on this surface being unable to contribute to the charge transport. This model indicates that the hole mobility of a continuous polymer strand is enhanced by as much as 2000% for the semiconducting polymer in the ePTFE OFETs relative to OFETs utilizing the nonporous native silicon wafer oxide as a gate dielectric. The ePTFE OFETs exhibit exceptional thermal stability, and annealing-based performance increases with slight variations among membranes arising from their unique microstructures.

Experimental Section



Scheme 1. Fabrication Process Schematic of an ePTFE-PDPP4T OFET. A membrane is cut to match the dimensions of a silicon wafer to which it is physically attached. Semiconducting polymer PDPP4T is spin-coated and shadow-mask-defined gold electrodes are vapor-deposited.

Substrate Preparation and ePTFE Membrane Attachment. Silicon wafers with 300 nm thermally deposited silicon oxide were cut into 24 mm squares (Scheme 1) and etched in a 3:1 H_2SO_4:30% H_2O_2 piranha solution for at least 4 hours. The wafers were then submerged and sonicated in solutions of deionized water, acetone, and isopropyl alcohol for 15 minutes each. Immediately following the sonication, the wafers were individually dried under nitrogen gas flow and ePTFE membranes (W. L. Gore & Associates) were laminated onto the wafers. To attach the ePTFE membrane, the dried wafer was placed oxide-side-up on a sheet of aluminum foil and a 9-inch by 11-inch frame of ePTFE membrane was placed directly on top of the wafer. A square of ePTFE membrane slightly larger than 24 mm was cut out using a razor blade and the excess membrane

was gently wrapped around the edges of the wafer using tweezers to prevent detachment during subsequent processing, with extra care taken not to stretch or deform the membrane during attachment.

Deposition of PDPP4T Semiconductor. A solution of 10 mg/mL PDPP4T (Ossila) dissolved in chloroform (Sigma-Aldrich) was prepared in a small glass vial, sonicated for 90 minutes in a 50 °C heated water bath, and filtered into a new glass vial using a 0.45 µm hydrophobic PTFE syringe filter. Enough solution was deposited on the surface of the membranes to cover it, and the membranes were subsequently spun at a speed of 2000 rpm with a spin acceleration of 1000 rpm/s for 60 seconds. Immediately after spin-coating, all coated membranes were placed in a vacuum oven set to 50°C at a pressure of approximately 50 cm Hg for 1 hour.

Deposition of Gold Electrodes. 50 nm of gold was thermally evaporated at a rate of 0.4 Å/s through shadow masks to produce six pairs of source-drain electrodes on all OFET samples with a channel length of 200 µm and a channel width of 11 mm.

SEM Imaging. The PDPP4T-coated membranes from each ePTFE OFET were carefully removed from their silicon wafer and mounted to SEM stubs using double-sided conductive tape. Cross-sections of each coated membrane were prepared using a Gatan Illion2 broad beam ion mill. The samples were then coated with a thin layer of platinum using a Cressington 208HR sputter coater. SEM images were then obtained using a Hitachi SU8230 FESEM.

X-Ray Diffraction. GIXRD patterns of PDPP4T, ePTFE membrane 1, and PDPP4T-coated ePTFE membrane 1 on silicon wafers were obtained using a Rigaku SmartLab diffractometer using Cu k_α radiation. The instrument was operated in a grazing incidence geometry at a 0.2º incident angle. Operating in this geometry greatly enhances the scattering intensity of the coated membrane by increasing the irradiated volume of the membrane relative to the substrate. Scans were measured from 3-40° 2θ at a 0.02° increment and a rate of 0.5° per minute using a HyPix 3000 detector in 0D mode.

Electrical Measurements. The output and transfer characteristics of four top-contact bottom-gate OFETs were analyzed using four different gate dielectrics. The gate dielectrics consisted of either ePTFE membrane 1 of nominal thickness 12.8 µm, ePTFE membrane 2 of nominal thickness 18 µm, ePTFE membrane 3 of nominal thickness 16 µm, or the native thermal oxide on the silicon wafer of nominal thickness 300 nm. The three ePTFE membranes were supplied by W. L. Gore & Associates and were fabricated according to the methodology outlined in U.S. patents.[55,56] The silicon oxide gate dielectric OFET served as a control device to analyze the influence of the three different ePTFE membranes being used in gate dielectrics.

To determine the output characteristics of the four OFETs, the drain current (I_{ds}) was measured as a function of the drain voltage (V_{ds}) from 0 V to -90 V while modulating the gate voltage (V_g) from 0 V to -70 V in steps of -10 V, producing a total of eight output curves corresponding to eight different values of V_g for each OFET. To determine the transfer characteristics of the four OFETs, I_{ds} was measured as a function of V_g from 0 V to -90 V while keeping V_{ds} constant at -90 V. In addition to these measurements, each OFET was charged for five minutes by applying a constant bias of -70 V to the source and drain electrodes while the gate

electrode remained unbiased at 0 V. Immediately after applying this bias to the source and drain electrodes, the transfer characteristics were re-measured using the exact same measurement conditions described above to analyze the threshold voltage shift (ΔV_{th}) in each OFET after charging.

Once the output and transfer characteristics of the four OFETs were measured, the OFETs were then annealed in a ceramic oven for 1 hour at either 100°C, 150°C, or 200°C. The same batch of four OFETs were never annealed at more than one of these temperatures for any duration longer than an hour – three different batches of four OFETs were fabricated such that one batch was annealed at 100°C for 1 hour, a second batch was annealed at 150°C for 1 hour, and a third batch was annealed at 200°C for 1 hour with all annealing taking place after initial testing. After annealing the OFETs in the ceramic oven, the output and transfer characteristics were re-measured using identical measurement conditions followed by the same -70 V charging for 5 minutes and additional transfer characteristic measurement.

The capacitance of each OFET was measured using an Agilent 4284A LCR meter operated at 1 kHz by connecting one test fixture probe to the gate electrode and the second test fixture probe to either the source electrode or drain electrode. Polarization-Field (P-E) loops were obtained by applying voltage to the gate electrode and measuring the polarization of each device.

Results

The output characteristics of OFETs using ePTFE membrane 1 and silicon oxide in gate dielectrics at annealing temperatures of 50°C and 150°C are shown in Figure 1. The transfer characteristics (sqrt drain current vs gate voltage) of OFETs using ePTFE membrane 1 and silicon oxide in gate dielectrics at annealing temperatures of 50°C and 150°C are shown in Figure 2.

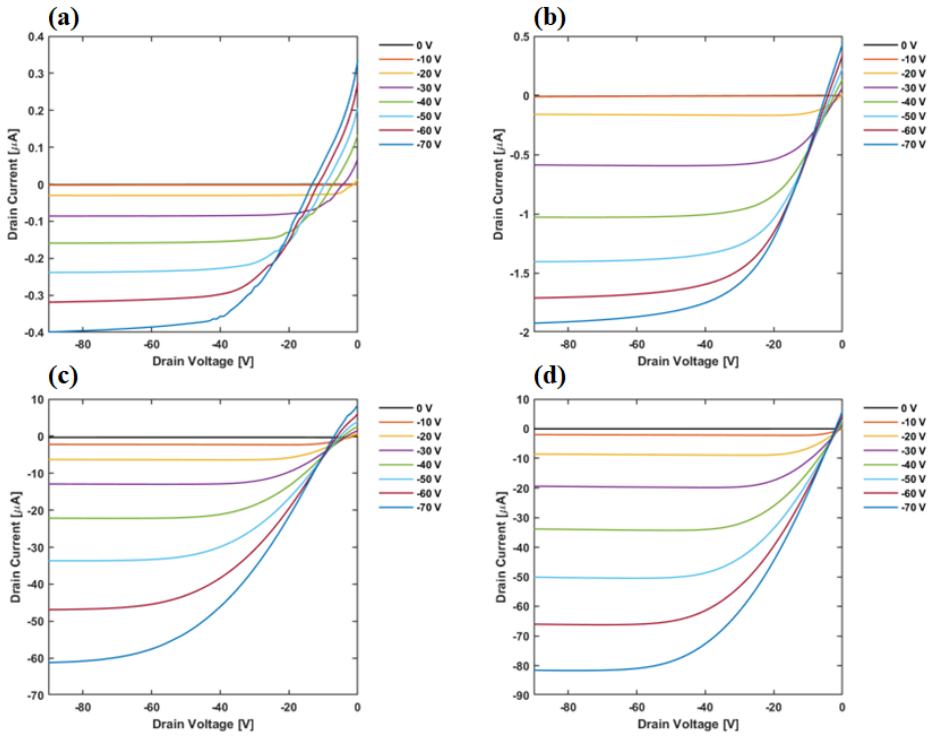


Figure 1. Output Characteristics of a) ePTFE Membrane 1 OFET Annealed at 50°C for 1 Hour, b) ePTFE Membrane 1 OFET Annealed at 150°C for 1 Hour, c) Silicon Oxide OFET Annealed at 50°C for 1 Hour, and d) Silicon Oxide OFET Annealed at 150°C for 1 Hour.

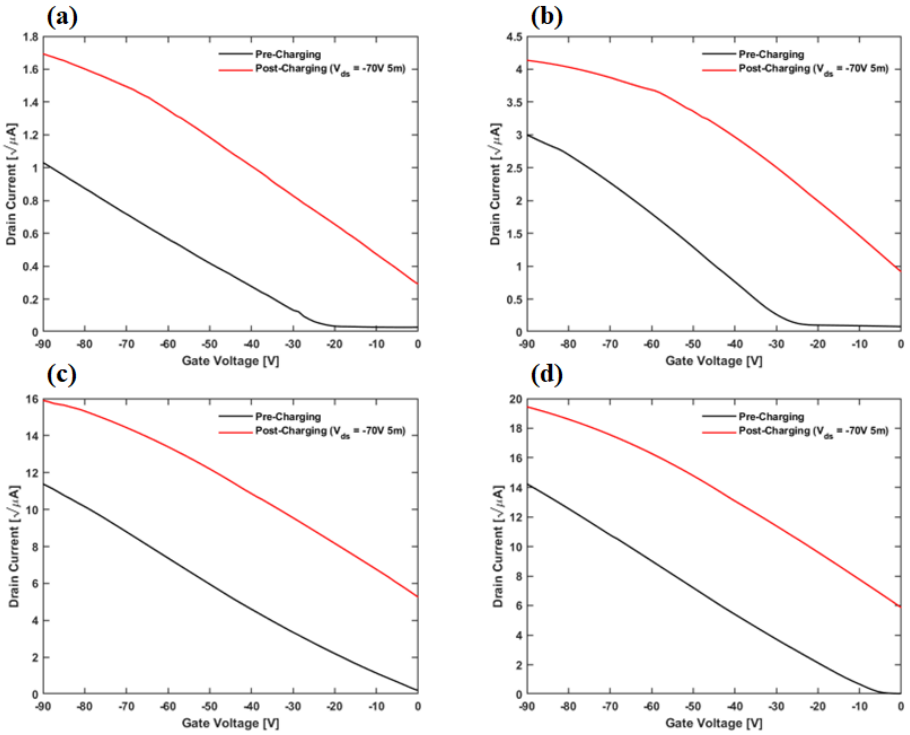


Figure 2. Square Root Transfer Characteristics (SQRT Drain Current vs Gate Voltage) Before and After Applying a -70 V Bias for 5 Minutes to Source and Drain Electrodes of a) ePTFE Membrane 1 OFET Annealed at 50°C for 1 Hour, b) ePTFE Membrane 1 OFET Annealed at 150°C for 1 Hour, c) Silicon Oxide OFET Annealed at 50°C for 1 Hour, and d) Silicon Oxide OFET Annealed at 150°C for 1 Hour. The Drain Voltage Was Held at -90 V During the Transfer Curve Acquisition.

Additional output and transfer characteristics, including on log scales, for all four annealing temperatures and all four gate dielectric materials are shown in Figures S1-S12 of the Supporting Information. For membrane 2, irregularities in the output curves are resolved on annealing at 100°C, but are more persistent with membrane 3. Hysteresis in the transfer behavior of devices on the better-performing membranes 1 and 2 is shown in Figure S13 of the Supporting Information. The curves indicate modest bias stress[57,58] for all the devices, except for an additional contribution from discharging of static polarization after charging membrane 1. The linear regions of the saturation regime in the sqrt transfer curves shown in Figure 2 (which show only modest gate voltage dependence of the slopes except at the highest gate voltages in some cases) can be used to extract the hole mobility of each device using the equation $I_{ds} = \frac{W}{2L}\mu C\left(V_g - V_{th}\right)^2$, in which W is the channel width of the device, L is the channel length of the device, C is the measured capacitance

per unit area of the device, and μ is the charge carrier mobility of the device, or in this case the hole mobility of the device.[37,45] By measuring the capacitance of each device and dividing it by the area of the electrode on which the measurement was performed, the above equation can be used for direct calculation of the hole mobility of each device.

OFET capacitances were measured in the presence of PDPP4T, as measuring the capacitances of uncoated ePTFE membranes with a silicon bottom contact and gold top contact produced extremely small capacitances resulting in calculated dielectric constants much smaller than 1. The PDPP4T did not add to the area of the capacitance measurement, which was ultimately determined by the total area of either the source electrode or drain electrode depending on which electrode the measurement was performed. It is possible, however, that the PDPP4T may have locally penetrated the ePTFE membrane under source and drain electrodes where the capacitance was measured, acting to decrease the effective dielectric thickness and resulting in slightly increased capacitances.

Polarization-field (P-E) loops for all devices at all four annealing temperatures and two different frequencies are provided for reference in Figures S14-S17 of the Supporting Information to show relationships between capacitance, voltage, and frequency. Figures S14-S15 show devices comprised of both membrane 1 and membrane 2 acting in depletion for positive gate voltages and accumulation for negative gate voltages. This behavior holds well up to an annealing temperature of 200˚C sustained for 1 hour and is consistent with capacitance-voltage characteristics of p-type OFETs.[59-61] The hysteresis in the accumulation regime of Figures S14-S15 shows that injected charge is not reversible during the measurement timescale at either frequency, while in the depletion regime the injected charge is almost completely reversible aside from devices annealed at 200˚C for 1 hour which show a very slight breakdown in dielectric behavior. Depletion-mode capacitances at 100 Hz and 1 kHz were comparable. Figure S16 illustrates devices comprised of membrane 3 showing far less ideal behavior than devices shown in Figures S14-S15, with devices annealed at 200˚C for 1 hour showing signs of dielectric breakdown and an absence of accumulation charge. The oxide control OFETs shown in Figure S17 also display non-ideal behavior with devices not properly operating in depletion for positive gate voltages at 1 kHz, however the devices do operate in accumulation for negative gate voltages which holds well at all four annealing temperatures. Similar to devices comprised of membranes 1 and 2, the control OFETs show accumulated charge is not immediately reversible at either measurement frequency, indicating that the accumulation of charges is not gate voltage dependent in these devices.

While the previously outlined approach for calculating the hole mobility of OFETs is suitable for most devices with continuous semiconducting films, we sought to quantify the mobility of the PDPP4T itself on the ePTFE. To do this, adjustments were required because of the porous ePTFE microstructure and lack of a continuous surface through which charge carriers can drift. This may be seen in the scanning electron microscopy (SEM) image of the top surface of ePTFE membrane 1 shown in Figure 3. SEM images of each ePTFE membrane at the four different annealing temperatures (shown in Figures S18-S21 of the Supporting Information) were obtained and edited in ImageJ by tracing and color-coding all areas of each image that were not the PDPP4T-coated top layer of the membrane. Only the top layer of the ePTFE membranes was considered to contribute to the charge carrier mobility. Due to the hydrophobic nature of the ePTFE membranes, it is unlikely that the PDPP4T solution would penetrate deeper than the top layer of

each membrane and form continuous transport paths there. The surface tension of chloroform at room temperature is 27.1 mN/m and while the surface tension of PTFE can vary, the room temperature value commonly given is 20.2 mN/m.[38,39] Studies of the wetting kinetics of PTFE show that for solutions with comparable surface tension to PTFE, wetting contact angles of less than 90° take up to approximately 10 seconds to be observed, far longer than the 1 to 2 seconds the solution contacts the membrane during spin coating.[40] In addition to the PDPP4T likely not penetrating into the membrane pores, the thermally evaporated gold electrodes do not penetrate deeply into the membrane pores as evidenced by cross-sectional SEM images of the PDPP4T-coated ePTFE membranes. An example is shown in Figure 3 for the case of ePTFE membrane 1, with cross-sections of each type of device shown in Figures S22-S25 of the Supporting Information. The edited SEM surface images (shown in Figures S26-S28 of the Supporting Information) were subsequently analyzed in Python by subtracting the color-coded regions of the images to calculate an adjusted channel width for each ePTFE OFET at all four annealing temperatures. After calculating the adjusted channel width for each ePTFE-PDPP4T OFET, the linear portion of the saturation regime of the transfer characteristic of each OFET was used to calculate the hole mobility. The results of the mobility calculations among other characteristic values determined from the OFETs transfer curves are displayed in Table 1.

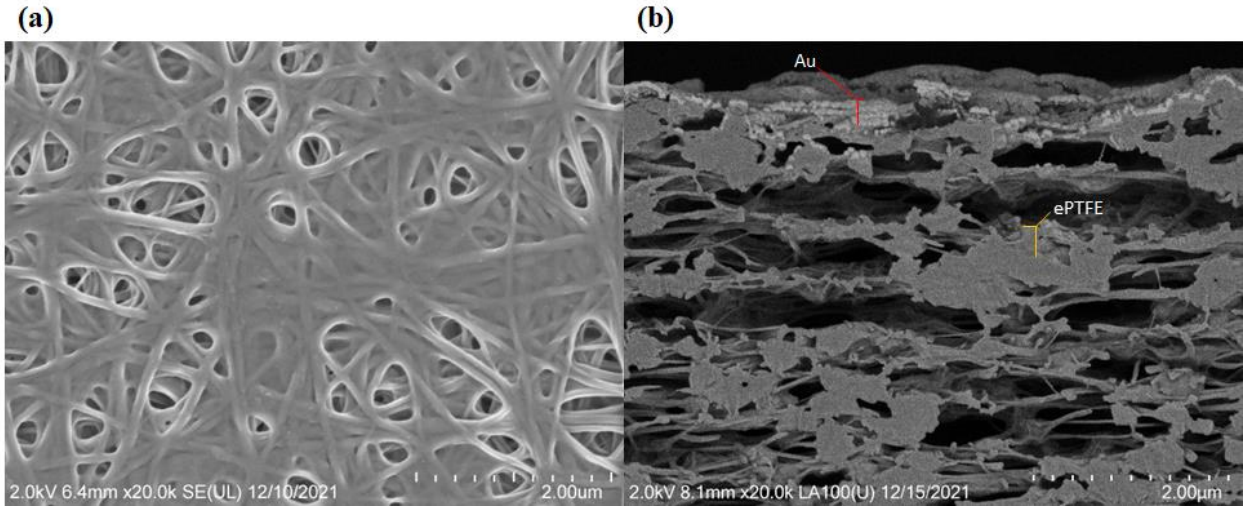


Figure 3. Scanning Electron Microscopy (SEM) Images of a) the Microstructure of the PDPP4T-ePTFE Surface of an ePTFE Membrane 1 OFET Annealed at 50°C for 1 Hour and b) the Cross-Section of the Same Device at the Location of a Pair of Source-Drain Electrodes Produced by Backscaterred Electrons.

Table 1. Mobilities, Threshold Voltages and Their Shifts, and on/off Ratios of OFETs Utilizing Four Different Gate Dielectrics After Annealing for 1 Hour at 50°C, 100°C, 150°C, and 200°C.

Dielectric	T_{anneal} [°C]	μ [$cm^2/V \cdot s$]	V_{th} [V]	ΔV_{th} [V]	I_{ON}/I_{OFF}
ePTFE 1	50	0.01±0.00	-21.8±1.6	38.56±0.64	10^3
	100	0.05±0.01	-24.0±1.1	40.88±0.79	10^2
	150	0.13±0.05	-26.0±3.7	42.7±1.6	10^3
	200	0.27±0.14	2.8±6.7	30.8±4.7	10^1
ePTFE 2	50	0.01±0.00	-21.5±1.8	30.4±1.4	10^3
	100	0.11±0.04	-34.0±4.3	33.8±2.8	10^2
	150	0.42±0.31	-25±11	38.8±4.8	10^1
	200	1.8±1.0	8.0±5.1	36.2±2.4	10^1
ePTFE 3	50	0.01±0.00	-15.9±4.0	11.5±1.2	10^1
	100	0.03±0.01	-39.1±3.7	9.4±2.5	10^2
	150	0.14±0.07	-26.1±4.0	14.4±3.0	10^1
	200	x	31.1±3.2	30.4±5.3	10^1
Silicon Oxide	50	0.09±0.02	-7.5±1.9	45.8±1.5	10^3
	100	0.15±0.04	-4.3±4.6	39.7±3.3	10^3
	150	0.13±0.01	-10.1±0.7	41.8±1.4	10^4
	200	0.09±0.03	-6.9±1.4	38.2±2.0	10^4

The sensitivity of the OFETs to NO_2 was determined by exposing the devices to concentrations of 1, 2, 5, and 10 ppm of NO_2 gas in a closed chamber for three minutes for each exposure and measuring the output and transfer characteristics of the devices between each exposure. The output characteristic was measured with V_g set to only –40 V while keeping the other previously discussed conditions the same, while the transfer characteristic was measured with no modifications from the previously discussed conditions. Using the transfer curves from each concentration of NO_2, the sensitivity was calculated as $S = \frac{I_{ds,NO2} - I_{ds,air}}{I_{ds,air}} \cdot 100\%$ at a V_g of -40 V for all OFETs. This V_g was chosen as it is larger than the V_{th} of all devices while minimizing non-ideal effects, such as contact resistance[48], that clearly manifest at V_g much higher than -40 V in the transfer curves. The transfer curve with corresponding I_{ds} at Vg = -40 V before any NO_2 gas exposure occurred, or 0 ppm, was used as the baseline ($I_{ds,air}$) for all sensitivity calculations. The sensitivities to NO_2 gas of the OFETs using ePTFE membrane 1 and the native silicon wafer oxide as gate dielectrics are shown in Figure 4. The responses of all devices at all four annealing temperatures after exposure to NO_2 gas are shown in Figures S29-S40 of the Supporting Information.

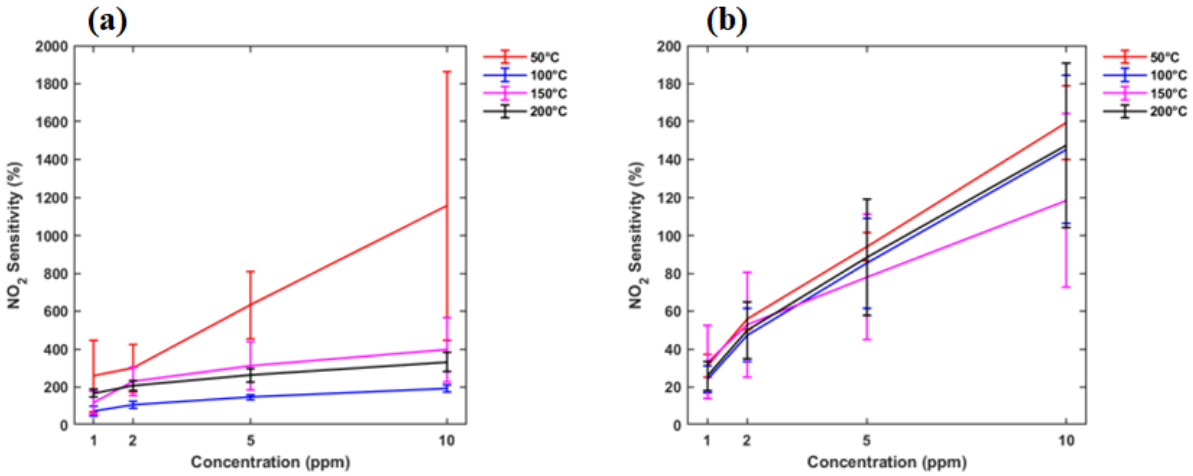


Figure 4. The Sensitivity of OFETs Utilizing a) ePTFE Membrane 1 and b) Silicon Oxide as Gate Dielectrics for Four Different Annealing Temperatures When Exposed to NO_2 in Concentrations of 1, 2, 5, and 10 ppm for 3 Minutes Each.

The drift of current of the OFETs in air was also determined before exposure to any NO_2 gas by measuring 25 transfer curves at a rate of –10 V/s while devices were exposed to air at ambient conditions. The drift in air of OFETs utilizing ePTFE membrane 1 and the native silicon wafer oxide are shown in Figure 5, with drifts of all devices at all four annealing temperatures provided in Figures S41-S44 and current vs. time data provided in Figures S45-S48 of the Supporting Information. The ratio of the drain current from the last transfer curve and the drain current from the first transfer curve at a gate voltage of -40 V was calculated to be the drift of each device, similar to how the sensitivity was calculated. After calculating the drift of the OFETs in air and the sensitivity of the OFETs to NO_2 gas, signal-to-drift ratios of the devices were calculated as $D = \frac{S}{\left(\frac{\Delta I_{ds}}{I_{ds}}\right)_{air}}$.[36] The drift and signal-to-drift ratios at concentrations of 1 and 10 ppm NO_2 for

all OFETs at each of the four annealing temperatures are summarized in Table 2. Note that drifts are actually current decreases while response signals are current increases, so the net sensitivity over time is even larger than tabulated here. Also, such drifts can be minimized with compensating circuitry.[50-54]

Table 2. Drift in Air and Signal-to-Drift Ratios For 3 Minute Exposure to NO_2 at 1 ppm and 10 ppm of OFETs Utilizing Four Different Gate Dielectrics After Annealing for 1 Hour at 50°C, 100°C, 150°C, and 200°C.

Dielectric	T_{anneal} [°C]	Drift [%]	$D_{1\ ppm}$	$D_{10\ ppm}$
ePTFE 1	50	-53±25	4.9±3.6	22±13
	100	-76.3±5.2	0.96±0.32	2.51±0.25
	150	-94.0±1.7	1.26±0.63	4.2±1.8
	200	-82.3±7.0	2.04±0.25	4.03±0.63
ePTFE 2	50	-72±17	1.20±0.96	19.3±5.1
	100	-81.4±7.2	2.9±1.3	10.4±4.6
	150	-68.9±8.0	3.9±3.2	9.7±5.7
	200	-80.4±6.4	4.34±0.89	9.4±1.6
ePTFE 3	50	-70±18	6.0±3.5	85±45
	100	-82.7±3.0	2.41±0.73	24±13
	150	-66.4±4.5	3.6±1.7	8.9±4.5
	200	-50±10	3.6±1.7	8.8±4.7
Silicon Oxide	50	14±11	2.23±0.43	11.3±1.4
	100	11.0±4.1	2.20±0.65	13.2±3.5
	150	8±11	4.3±2.5	15.5±6.0
	200	13±11	2.02±0.61	11.6±3.4

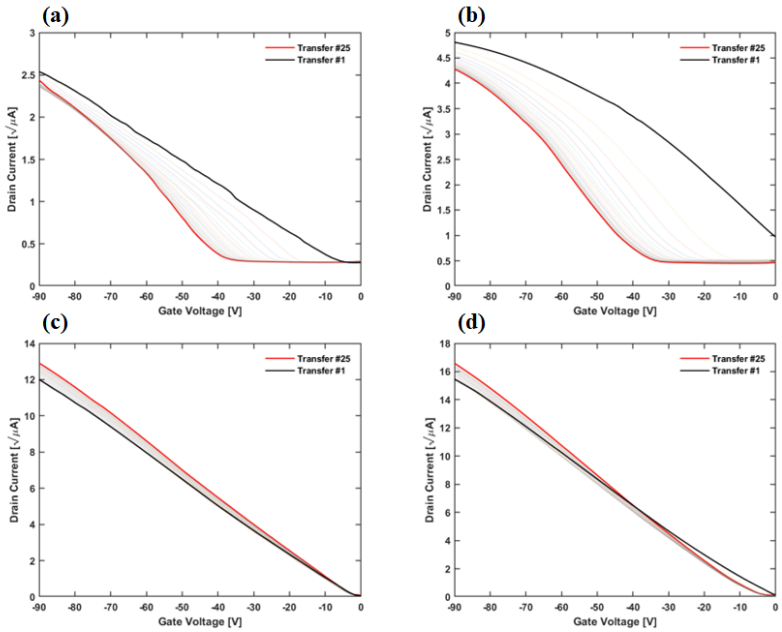


Figure 5. The 25 SQRT Transfer Curves Obtained at a Rate of -10 V/s While OFETs Were Exposed to Air and Ambient Conditions for Determination of Drift Current in a) ePTFE Membrane 1 OFET Annealed at 50°C for 1 Hour, b) ePTFE Membrane 1 OFET Annealed at 150°C for 1 Hour, c) Silicon Oxide OFET Annealed at 50°C for 1 Hour, and d) Silicon Oxide OFET Annealed at 150°C for 1 Hour.

Grazing incidence X-ray diffraction (GIXRD) patterns of PDPP4T, ePTFE membrane 1, and PDPP4T-coated ePTFE membrane 1 on silicon wafers are shown in Figure 6. A shoulder indicating the PDPP4T principal diffraction peak is observed from the coating on ePTFE, identified by the red dashed line intersecting the blue trace.

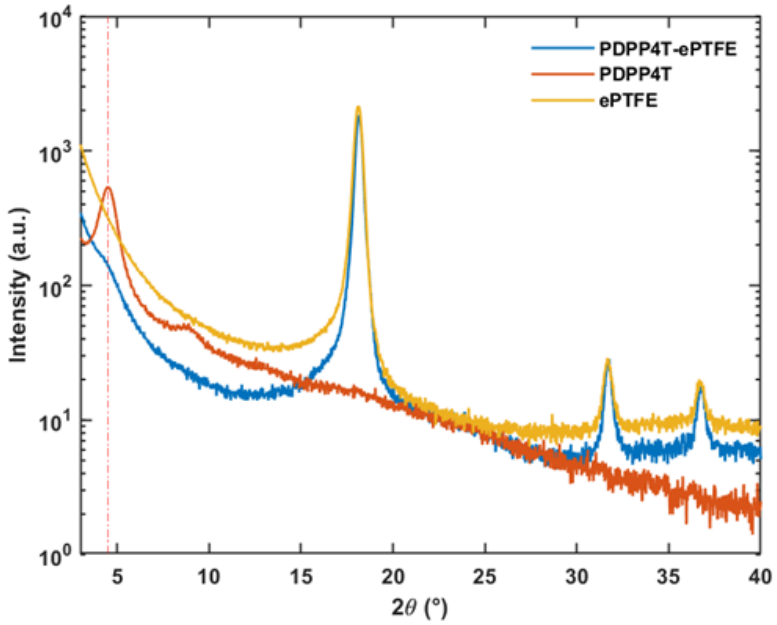


Figure 6. Grazing Incidence X-Ray Diffraction (GIXRD) Patterns of ePTFE Membrane 1 on a Cleaned Silicon Wafer, a PDPP4T Thin Film on a Cleaned Silicon Wafer Produced From a 10 mg/mL PDPP4T in Chloroform Solution, and ePTFE Membrane 1 Coated With a 10 mg/mL PDPP4T in Chloroform Solution on a Cleaned Silicon Wafer.

Discussion and Analysis

The output characteristics shown in Figure 1 and Figures S1-S4 of the OFETs tested in this study display clear behavioral contrasts between the use of ePTFE membranes and the native silicon wafer oxide alone in gate dielectrics. The output characteristics of all ePTFE membrane OFETs show clear deviations from ideal OFET behavior at the base annealing temperature of 50°C. While membrane 1 appears to show significant leakage current[46] as well as pronounced effects of contact resistance[47], this non-ideal behavior becomes even more noticeable with ePTFE membranes 2 and 3 at 50°C. However, as annealing temperature increases to 100°C and above, the output behavior of the ePTFE membrane OFETs improves and even becomes comparable to the silicon oxide OFET. Meanwhile, the silicon oxide OFET displays relatively ideal OFET behavior at all annealing temperatures apart from slight effects of contact resistance observed at low drain voltages, serving as a strong control device with which to compare results of the ePTFE OFETs.

As annealing temperature increases, the leakage current and contact resistance both lessen in the ePTFE OFETs while I_{ds} increases significantly. For example, OFETs using ePTFE membrane 2 exhibited a maximum I_{ds} of just -202 nA at a V_g of -70 V when annealed at 50°C for 1 hour, while the same device annealed at 200°C for 1 hour exhibits a maximum I_{ds} of -7.19 µA at a V_g of -70 V. In Figure 1, there is a 480% increase in the maximum I_{ds} of the ePTFE membrane 1 OFET as a result of annealing at 150°C for 1 hour, while only a 130% increase in the maximum I_{ds} is observed in the control OFET for the same annealing process. While the output behavior improves and I_{ds} increases dramatically in ePTFE OFETs annealed above the base 50°C annealing temperature, slight conductive behavior begins to develop due to the increased annealing

temperature. This is especially apparent in OFETs utilizing ePTFE membrane 3, as annealing temperatures of 150°C and 200°C sustained for 1 hour create clear effects of partially conductive behavior as evidenced by the output characteristics of these devices. The control device also appears to show very slight development of partially conductive behavior with increasing annealing temperature as current saturation is not completely achieved at higher gate voltages, however the effects are much less pronounced compared to the ePTFE OFETs.

In addition to the output characteristic improvements exhibited by the ePTFE OFETs as a result of annealing, significant changes in the transfer characteristics also arise from static charging as shown in Figure 2 and Figures S5-S12. The transfer characteristics of both the ePTFE OFETs and the control OFET exhibit relatively ideal behavior at all four annealing temperatures, with clear linear and saturation regimes present in each transfer curve. Once again, current increases are observed as a result of increasing the annealing temperature with more prominent increases occurring in the ePTFE OFETs. When comparing the V_{th} of the OFETs in Table 1, the control OFET requires much less voltage to turn on than the ePTFE OFETs. At an annealing temperature of 50°C, V_{th} of the control OFET is just -7.5 V while the ePTFE OFETs exhibit a V_{th} of -21.8V, -21.5 V, and -15.9 V for membranes 1, 2, and 3, respectively. As annealing temperature is increased, V_{th} remains relatively constant for the control OFET, ranging from -4.3 V at 100°C to -10.1 V at 150°C. For the ePTFE OFETs, V_{th} tends to slightly increase at both 100°C and 150°C, then substantially decreases and becomes positive at 200°C for all three membranes, probably due to the beginning of oxidative decomposition that created doping sites and conductive behavior even at gate voltage of zero. The positive V_{th} observed in all three ePTFE OFETs annealed at 200°C is likely a result of doping that arises due to slight decomposition of the membrane at such a high annealing temperature, evidenced by surface and cross-sectional SEM images of the membrane OFETs provided in Figures S18-S24. While V_{th} changes significantly when the ePTFE OFETs are annealed at 200°C, ΔV_{th} of all four OFETs remains similar in magnitude at every annealing temperature, apart from the ePTFE membrane 3 OFET showing a significant increase in ΔV_{th} after annealing at 200°C. The observed ΔV_{th} in all devices is consistent with the mechanism of bias stress[57,58] and holds at all annealing temperatures. This indicates that charge storage behavior is not compromised by the annealing process, signifying the integrity of the OFETs is maintained and their performance increases are sustainable at the annealing conditions used in this study due to their thermal and mechanical durability. However, we did not observe stability in the charge storage behavior, meaning that the conditions under which we applied static charge did not drive this charge into deep enough states (energetically or positionally) to prevent dissipation. The equilibration of the trap energy level to lower gate voltages (less negative V_{th}) would be the result of holes injected from the dielectric into traps during static charging, thus filling them and allowing a less negative onset voltage for holes to be mobile.

The largest difference among the OFETs that is observed in the transfer characteristic is the hole mobility of the devices. The control OFET exhibits a hole mobility ranging from 0.09 to 0.15 $cm^2/V \cdot s$, with the maximum mobility occurring after annealing the device at 100°C for 1 hour. When comparing these values to the mobilities of the ePTFE OFETs in the temperature range of 150°C to 200°C, the ePTFE OFETs exhibit mobilities as much as 20 times larger than the control OFET. Additionally, the mobilities of the ePTFE OFETs at 200°C are anywhere from 27 to 180 times greater than their mobilities at 50°C. The peak mobilities for OFETs utilizing membranes 1,

2 and 3 are 0.27, 1.8, and 0.14 $cm^2/V \cdot s$, respectively, occurring at an annealing temperature of 150°C for membrane 3 and 200˚C for membranes 1 and 2. While it is possible that an OFET utilizing ePTFE membrane 3 may also exhibit higher mobility at 200˚C than 150˚C, the calculated mobility value for this device was omitted due to being unreasonably high, likely caused by a breakdown in the insulating behavior of the dielectric membrane. To understand why the mobilities of the ePTFE OFETs are so much greater than the control OFET and why the mobilities increase substantially with increased annealing temperature, it is important to discuss the mobility model on which these calculations are based and the underlying mechanisms of the annealing-induced performance enhancements.

As previously mentioned, the channel width of the ePTFE OFETs was adjusted to account for the microporous structure of the membranes. It is logical that charge carriers are unable to be transported through a medium in which both the dielectric membrane material and the semiconducting polymer are not present, therefore this must be accounted for when calculating the mobility of the ePTFE OFETs. When analyzing the SEM micrographs of the ePTFE-PDPP4T surface (Figures S18-S20), it appears that the PDPP4T coats the fibers of the top surface layer of the ePTFE membrane. Cross-sectional SEM images of the ePTFE OFETs (Figures S22-S24) show lack of penetration of thermally evaporated gold electrodes beneath the top surface layer of the ePTFE. It is also likely that the low surface tension of the ePTFE membranes combined with their hydrophobic characteristics is sufficient to prevent the PDPP4T in chloroform solution from penetrating into the micropores of the membranes.[38,39,40] Assuming that PDPP4T-coated ePTFE fibers exist only on the top surface layer of the ePTFE membrane and that charge carriers cannot be transported in areas where these coated fibers are not present, then any surface pores or uncoated ePTFE fibers underneath the top surface layer of the membranes shown in the SEM micrographs can be considered not to contribute to the hole mobility of the OFET. By establishing these assumptions, the areas of the SEM micrographs that do not contribute to the mobility of the OFET can be traced and colored with a specific RGB color code not originally present in the micrographs for subsequent image analysis to calculate the adjusted channel width of the OFET.

To calculate the adjusted channel width of the ePTFE OFETs, first all areas of the SEM micrograph not containing top surface ePTFE fibers are traced and saved as an overlay in the image analysis software ImageJ. Using the overlay and ImageJ, the entire area of all traced non-contributing areas is colored with the RGB color code (255, 0, 0). This specific RGB color code is chosen as it is not present anywhere in the original unedited SEM micrograph, while choosing a color code with only a single non-zero value simplifies further steps of the image analysis. After color-coding the non-contributing areas, the image is analyzed in Python to calculate the number of colored pixels with RGB value (255, 0, 0) that occur in every row of 1-pixel width. The fraction of pixels in each row that are colored are then subtracted from 100% to determine the fraction of pixels in each row that represent the PDPP4T-coated ePTFE fibers on the top surface of the membrane. The fraction of remaining unedited ePTFE fibers is then multiplied by the original channel width of 11 mm to yield the adjusted channel width of the ePTFE OFET. This model is generated for all ePTFE membranes at all annealing temperatures, yielding a total of 12 unique models producing adjusted OFET channel widths to use for calculations of hole mobility in the ePTFE OFETs. Adjusted channel widths and capacitances, among other characteristic values, used to calculate the mobility of each device are shown in Tables S1-S4 of the Supporting Information.

The channel length of these OFETs remains unadjusted despite the corrections made to the channel width due to the geometry of the source and drain electrodes. This is a conservative decision, as some charge transport pathways are more convoluted than a linear distance between source and drain.

When looking at the SEM micrographs (Figures S18-S21), the nearest electrodes would be parallel to the top and bottom of the images with a total length of 200 μm between them, while the larger channel width of 11 mm runs horizontally across the micrograph and snakes back and forth throughout the rest of the device channel. Modifying both dimensions would not properly account for the membrane microstructure while modifying the channel length and keeping the channel width constant would be inaccurate, as this would result in mobilities that are an order of magnitude smaller than what is actually observed and many orders of magnitude smaller than the adjusted width mobilities. Neither the channel width nor channel length of the control OFETs require adjustment as both the silicon oxide dielectric layer and the PDPP4T semiconductor layer are continuous throughout the entire channel. The calculation of an adjusted channel width is necessary for the ePTFE OFETs, as employing a constant channel width of 11 mm at each annealing temperature would underestimate the fixed mobility of the device that results from the porous microstructure and its response to each annealing procedure.

The maximum mobility values that arise from this approach are exceptionally higher than those of the silicon oxide control OFETs, especially the maximum mobility of 1.8 $cm^2/V \cdot s$ observed in the OFET utilizing ePTFE membrane 2. In the extreme case that an adjusted channel width based on the porous membrane microstructure is not considered at all, maximum mobility values of OFETs utilizing membranes 1, 2 and 3 would be 0.16, 0.84, and 0.06 $cm^2/V \cdot s$, respectively, again occurring at an annealing temperature of 150°C for membrane 3 and 200˚C for membranes 1 and 2. Even in the complete absence of the adjusted channel width model, the maximum mobility of 0.84 $cm^2/V \cdot s$ in the ePTFE membrane 2 OFET is still quite impressive and far larger than the maximum mobility of the control OFET. While the OFETs utilizing ePTFE membranes show significant mobility enhancements when compared to the silicon oxide control OFET, the mobilities of these OFETs are considerably smaller, sometimes by as much as two orders of magnitude, compared to reported mobility values for PDPP4T OFETs in the literature. This is attributed to a lack of optimization in the device fabrication process, such as using a spinning solution of room temperature chloroform rather than hot 1,2-dichlorobenzene and not using any surface treatment on the silicon wafers aside from the piranha etch and solvent cleaning process.[18,32,41,42]

Many of the improvements of the OFETs in this study that result from increased annealing temperatures can be attributed to increases in crystallization of both the PDPP4T and the ePTFE membranes. A study on PDPP5T, whose structure is very similar to PDPP4T, showed that annealing OFETs up to 200°C resulted in increased mobility and device current[32]. It has also been demonstrated that oriented PTFE films can promote epitaxial growth of additional layers, leading to high degrees of alignment in films deposited on PTFE[33,34,35].Considering that the PDPP4T likely does not penetrate into the pores of the membranes during spin coating based on the surface tensions of PTFE and chloroform,[38,39,40] it is likely that the PDPP4T has a preferred orientation with the ePTFE and forms a highly ordered coating on the membrane surface. The membranes themselves have crystalline characteristics as shown in the GIXRD data in Figure 6, which can

further support the idea that the PDPP4T has a preferred orientation with respect to the surface of the ePTFE membrane during the coating process. Subsequent annealing at higher temperatures allows for the development of higher ordering in the PDPP4T, increasing the crystallinity as well as the π-π stacking of the polymer chains leading to increased current in the output characteristics and contributing to the increased mobility of all OFETs in this study. The peaks in Figure 6 localized near 4.5° and 9.1° are representative of the high crystallinity observed in the PDPP4T thin film, while peaks near 18.1°, 31.7°, and 36.7° show the crystallinity of ePTFE membrane 1. A shoulder peak is observed near 4.5° in the PDPP4T-coated ePTFE membrane 1 sample, possibly due to lower quantity of crystalline PDPP4T exposed to the x-ray beam relative to ePTFE.

The annealing process also causes observable changes in the ePTFE microstructure, as shown in Figures S18-S25, which likely contribute to the improved output behavior. High annealing temperatures above the glass transition temperature (T_g) and closer to the melting temperature (T_m) of PTFE, combined with the microporous structure of ePTFE, can result in the dielectric layer thickness of the ePTFE OFETs decreasing with sustained annealing times, as mentioned more generally in the "results" section. This is also clearly visible in Figures S22-S24, in which ePTFE membranes 1 and 2 undergo significant shrinkage from 50˚C to 200˚C while surprisingly, ePTFE membrane 3 maintains a relatively constant thickness. The reduced thickness of the dielectric layer can lead to increased electric fields in the device which would allow for greater charge carrier induction observed as increased current in the device, associated with higher capacitance that was indeed incorporated into the mobility calculations. Due to the unorthodox nature in which the dielectric membrane is attached to the substrate to preserve the unique membrane microstructures and fabricate the ePTFE OFETs in this study, it is likely the bonding between the dielectric layer and the gate is much lower than if a traditional processing method such as spin coating were used. This could be a major source of non-ideal output behavior in the ePTFE OFETs at low annealing temperatures and it is possible the thickness reduction of the ePTFE membrane during the annealing process allowed for better contact to be made between the dielectric layer and the gate, resulting in drastic improvements in the quality of the output characteristics of the ePTFE OFETs.

Variations in each ePTFE membrane microstructure shown in Figures S18-S24, such as pore diameter and total porosity, will also lead to characteristic differences in OFET device behavior which can be found in maximum current, mobility, and gas sensitivity. Figures S18-S19 show that as annealing temperatures increase from 50˚C to 150˚C in ePTFE membranes 1 and 2, pore size appears to decrease due to fibrils becoming longer and thinner. A further annealing temperature increase to 200˚C causes opposite effects on the pore size and appearance of the fibrils due to the previously mentioned shrinkage of these two membranes that occurs at this annealing temperature. Figure S20 shows less variance in microstructure as a function of annealing temperature for ePTFE membrane 3, which is due to the absence of significant shrinkage in this membrane as shown in Figure S24, where very little shrinkage is observable. These observations are also consistent with trends in the adjusted channel width of each ePTFE membrane OFET listed in Tables S1-S3, as devices comprised of membranes 1 and 2 show reduction in adjusted channel width from 50˚C to 150˚C before moderate increases are observed at 200˚C, while the ePTFE membrane 3 OFET maintains a relatively consistent adjusted channel width across all four annealing temperatures with a slight increase observed at 200˚C. The observed differences in how

annealing temperature affects the microstructure and adjusted channel width of the three different ePTFE membranes can be explained by differences in porosity, thickness, and surface area of each membrane as well as higher crystallinity of ePTFE membrane 3, which is likely responsible for the previously mentioned breakdown in insulating behavior of this membrane at an annealing temperature of 200˚C.

In addition to the performance increases resulting from the annealing process, responses of the OFETs to NO_2 gas were monitored as shown in Figure 4. The responses of the control OFET to NO_2 gas were highest at an annealing temperature of 50°C, with maximum sensitivities of 31 %, 56%, 94%, and 159% when exposed for 3 minutes at concentrations of 1, 2, 5 and 10 ppm, respectively. The responses were approximately 5-25% smaller at all concentrations at increased annealing temperatures, with the smallest responses occurring at an annealing temperature of 100°C for 1 and 2 ppm and 150°C for 5 and 10 ppm. For membrane 1, maximum responses to NO_2 were also observed to occur at an annealing temperature of 50°C, with maximum sensitivities of 260%, 300%, 630%, and 1200% when exposed for 3 minutes at concentrations of 1, 2, 5 and 10 ppm, respectively. The smallest responses for the ePTFE membrane 1 OFET all occurred at an annealing temperature of 100°C, with responses as much as 83% smaller than the maximum response occurring at a concentration of 10 ppm. Membrane 2 shows slightly higher maximum sensitivities to NO_2 than membrane 1, with maximum responses of 350%, 420%, 780%, and 1390% when exposed for 3 minutes at concentrations of 1, 2, 5, and 10 ppm, respectively. These maximum sensitivities occur at annealing temperatures of 200°C for 1 and 2 ppm of NO_2 and 50°C for 5 and 10 ppm of NO_2. Membrane 3 shows a strong trend of decreasing sensitivity with increased annealing temperature at all concentrations, with responses as high as 3100% occurring at a concentration of 10 ppm NO_2 and a 50°C annealing temperature.

The drift in air, shown in Figure 5 as well as Figures S41-S44 for all devices, is comparable for all three membranes at all four annealing temperatures. Drifts were measured to be between 50% and 94% in the direction of decreasing current for the ePTFE OFETs. For the control OFET, drifts ranged from 8% at 150°C to 14% at 50°C in the direction of increasing current. The response to NO_2 of all devices is in the direction of increasing current. Previous work where polymers similar in structure to PDPP4T were exposed to NO_2 gas indicate similar signal-to-drift ratios for the control OFET[36], with the control OFET annealed at 150°C for 1 hour showing the largest and most competitive signal-to-drift ratios despite a 2-minute shorter exposure to NO_2. Exposure of the OFETs to NO_2 gas results in increased current as the NO_2 is an oxidizing agent, creating higher charge density in the PDPP4T and enhancing the current of the OFET.[48,49] The sensitivities of the ePTFE OFETs to NO_2 are much larger than the control likely due to the much larger surface area provided by the porous membrane microstructure, providing far more numerous active sites at which the NO_2 can interact with the PDPP4T. Likewise, the drift of the ePTFE OFETs is much larger than the control due to the increased surface area and may also be caused by the previously mentioned lack of bonding between the membrane and the gate. Maximum signal-to-drift ratios appear to occur at annealing temperatures of 150°C for silicon oxide, while membranes 1, 2, and 3 all peak at 50°C, with the exception of membrane 2 having the highest signal-to-drift for 1 ppm at an annealing temperature of 200°C. The signal-to-drift ratio at 150°C and 1 ppm NO_2 exposure in the control OFET is comparable to the maximum signal-to-drift ratio at 1 ppm NO_2 exposure in the ePTFE OFETs, while at 10 ppm NO_2 exposure the signal-to-drift ratios of the ePTFE OFETs

are considerably higher than the control OFET. Overall, the unique microstructure of the ePTFE membranes serves to enhance the sensitivity of the OFET when exposed to NO_2 at a wide variety of concentrations, with large variances observed in all devices due to the drift current.

Utilization of ePTFE membranes as novel dielectric materials in OFETs serves to enhance the mobility of the semiconducting polymer and sensitivity of the devices while providing a flexible, thermally and mechanically durable hydrophobic substrate upon which devices with a wide variety of applications can be fabricated. Annealing the OFETs serves to improve their transistor behavior in the output and transfer characteristics by substantially increasing their current, mobility, and possibly improving the bonding at the gate-dielectric interface. Annealing temperatures up to 200°C sustained for up to 1 hour do not appear to damage the integrity of the device, as the charge storage behavior of the devices and the magnitude of ΔV_{th} are maintained. Many future experiments can be conducted using ePTFE membranes in gate dielectrics, such as fundamental studies of the crystallinity and orientation of semiconducting polymers with which the membranes are coated, or measuring device responses to a variety of gases and analytes other than NO_2. Making a freestanding device by using ePTFE membranes as both the substrate and the dielectric layer could help alleviate sources of error, as a lack of bonding at the gate-dielectric interface would likely not be a prominent issue in a successfully operable freestanding device. The results of this study, including the significant hole mobility enhancements, could be transferrable to other non-PTFE polymer membrane dielectrics, providing a unique approach towards the fabrication of high-performance, low-cost, flexible electronics.

Conclusion

In this study, OFETs utilizing ePTFE membranes as a novel gate dielectric exhibited pronounced increases in device performance as a result of a 1-hour annealing process up to temperatures of 200°C. Annealing the devices dramatically improved their transistor behavior and resulted in material mobilities as large as 1.8 $cm^2/V \cdot s$, compared to a maximum mobility of just 0.15 $cm^2/V \cdot s$ observed when utilizing the native silicon wafer oxide as a gate dielectric. Devices utilizing ePTFE membranes also showed enhanced sensitivity to NO_2 gas, with larger signal-to-drift ratios than devices utilizing silicon oxide. These results present a unique approach for improving the performance of organic electronic devices, where the combination of a microporous dielectric membrane and high-temperature annealing produce marked increases in device mobility and current while preserving their charge storage behavior. Further development of this work provides the opportunity for the fabrication of flexible, biocompatible, thermally and mechanically durable electronics that are low in cost and high in performance.

Supporting Information. Electronic characteristics of transistors, polarization data, electron microscopy, vapor responses, thermal stability, capacitance data, and data for mobility correction.

Conflict of Interest Statement. A patent application was filed on this technology.

Acknowledgements

This research was supported by W. L. Gore & Associates and the National Science Foundation Partnerships for Innovation program, Grant number 2234261. We thank Klaus Seibert for consulting on the use of ePTFE membranes, and Cornelia Rosu for consulting on the X-ray diffraction experiments. We acknowledge initial tests of the fabrication method by Qingyang Zhang and Evan Plunkett. The Radiant Technologies P-E apparatus and its initial testing was supported by the Office of Naval Research, Grant number N00014-23-1-2273.

References

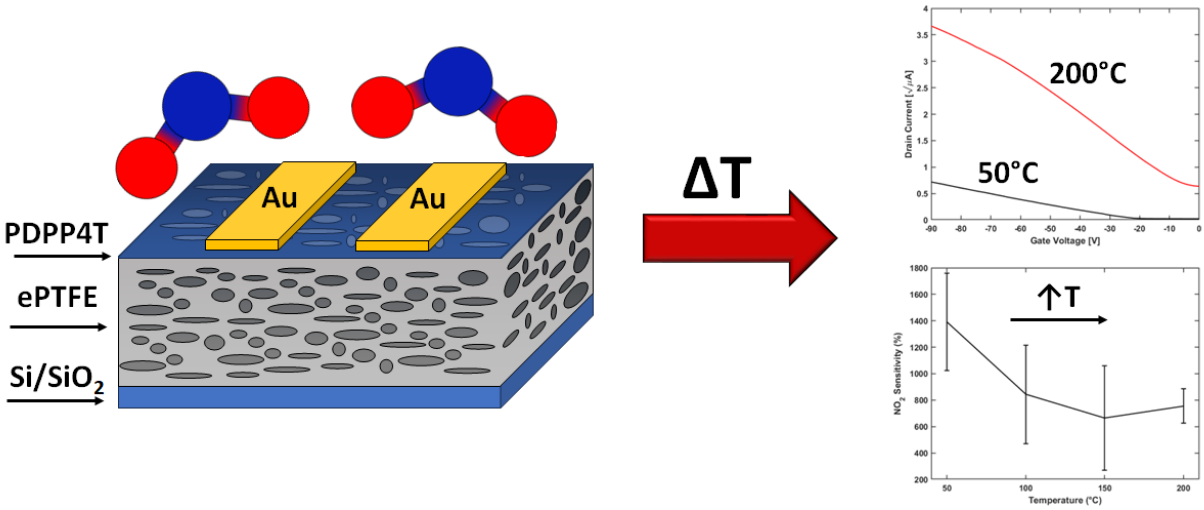
1. Zhang, F., Qu, G., Mohammadi, E., Mei, J., Diao, Y., Zhang, F., Qu, G., Mohammadi, E., Diao, Y., Mei, J. Solution-Processed Nanoporous Organic Semiconductor Thin Films: Toward Health and Environmental Monitoring of Volatile Markers. *Advanced Functional Materials* **2017,** *27(23)*, 1701117, DOI: 10.1002/ADFM.201701117
2. Yu, J., Yu, X., Zhang, L., Zeng, H. Ammonia Gas Sensor Based on Pentacene Organic Field-Effect Transistor. *Sensors and Actuators B: Chemical* **2012**, *173*, 133-138, DOI: 10.1016/J.SNB.2012.06.060
3. Lee, M. Y., Lee, H. R., Park, C. H., Han, S. G., Oh, J. H. Organic Transistor-Based Chemical Sensors for Wearable Bioelectronics. *Accounts of Chemical Research* **2018**, *51(11)*, 2829-2838, DOI: 10.1021/acs.accounts.8b00465
4. Han, S., Yang, Z., Li, Z., Zhuang, X., Akinwande, D., Yu, J. Improved Room Temperature NO2 Sensing Performance of Organic Field-Effect Transistor by Directly Blending a Hole-Transporting/Electron-Blocking Polymer into the Active Layer. *ACS Applied Materials & Interfaces* **2018**, *10(44)*, 38280-38286, DOI: 10.1021/acsami.8b07838
5. Soldano, C., D'Alpaos, R., Generali, G. Highly Efficient Red Organic Light-Emitting Transistors (OLETs) on High-k Dielectric. *ACS Photonics* **2017**, *4(4)*, 800-805, DOI: 10.1021/acsphotonics.7b00201
6. Yagi, I., Hirai, N., Miyamoto, Y., Noda, M., Imaoka, A., Yoneya, N., Nomoto, K., Kasahara, J., Yumoto, A., Urabe, T. A Flexible Full-Color AMOLED Display Driven by OTFTs. *Journal of the Society for Information Display* **2008**, *16(1)*, 15-20, DOI: 10.1889/1.2835023
7. Wang, X., Gu, Y., Xiong, Z., Cui, Z., Zhang, T. Silk-Molded Flexible, Ultrasensitive, and Highly Stable Electronic Skin for Monitoring Human Physiological Signals. *Advanced Materials* **2014**, *26(9)*, 1336-1342, DOI: 10.1002/ADMA.201304248
8. Kang, J., Son, D., Wang, G., Liu, Y., Lopez, J., Kim, Y., Oh, J., Katsumata, T., Mun, J., Lee, Y., Jin, L., Tok, J., Bao, Z. Tough and Water-Insensitive Self-Healing Elastomer for Robust Electronic Skin. *Advanced Materials* **2018**, *30(13)*, 1706846, DOI: 10.1002/ADMA.201706846
9. Torrent, M., Rovira, C. Novel Small Molecules for Organic Field-Effect Transistors: Towards Processability and High Performance. *Chemical Society Reviews* **2008**, *37(4)*, 827-838, DOI: 10.1039/B614393H
10. Quinn, J., Zhu, J., Li, X., Wang, J., Li, Y. Recent Progress in the Development of N-Type Organic Semiconductors for Organic Field Effect Transistors. *Journal of Materials Chemistry C* **2017**, *5(34)*, 8654-8681, DOI: 10.1039/C7TC01680H

11. Shi, L., Guo, Y., Hu, W., Liu, Y. Design and Effective Synthesis Methods for High-Performance Polymer Semiconductors in Organic Field-Effect Transistors. *Materials Chemistry Frontiers* **2017**, *1(12)*, 2423-2456, DOI: 10.1039/C7QM00169J
12. Liu, Z., Yin, Z., Chen, S., Dai, S., Huang, J., Zheng, Q. Binary Polymer Composite Dielectrics for Flexible Low-Voltage Organic Field-Effect Transistors. *Organic Electronics* **2018**, *53*, 205-212, DOI: 10.1016/J.ORGEL.2017.11.039
13. Aziz, F., Anuar, A., Ahmad, Z., Roslan, N., Makinudin, A., Bawazeer, T., Alsenany, N., Alsoufi, M., Supangat, A. Enhancing the Electrical Properties of Vertical OFETs Using a P(VDF-TrFE) Dielectric Layer. *Journal of Electronic Materials* **2020**, *49(2)*, 1362-1371, DOI: 10.1007/S11664-019-07805-3
14. Kang, B., Jang, M., Chung, Y., Kim, H., Kwak, S., Oh, J., Cho, K. Enhancing 2D Growth of Organic Semiconductor Thin Films with Macroporous Structures via a Small-Molecule Heterointerface. *Nature Communications* **2014**, *5(1)*, 1-7, DOI: 10.1038/ncomms5752
15. Ha, J. S, Kim, K. H., Choi, D. H. 2,5-Bis(2-octyldodecyl)pyrrolo[3,4-c]pyrrole-1,4-(2H,5H)-dione-Based Donor-Acceptor Alternating Copolymer Bearing 5,5'-Di(thiophen-2-yl)-2,2'-biselenophene Exhibiting 1.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$ Hole Mobility in Thin-Film Transistors. *Journal of the American Chemical Society* **2011**, *133(27)*, 10364-10367, DOI: 10.1021/ja203189h
16. Liu, X., Guo, Y., Ma, Y., Chen, H., Mao, Z., Wang, H., Yu, G., Liu, Y. Flexible, Low-Voltage and High-Performance Polymer Thin-Film Transistors and Their Application in Photo/Thermal Detectors. *Advanced Materials* **2014**, *26(22)*, 3631-3636, DOI: 10.1002/ADMA.201306084
17. Ludwig, G., Watters, R. Drift and Conductivity Mobility in Silicon. *Physical Review* **1956**, *101(6)*, 1699, DOI: 10.1103/PhysRev.101.1699
18. Yang, Y., Liu, Z., Chen, L., Yao, J., Lin, G., Zhang, X., Zhang, G., Zhang, D. Conjugated Semiconducting Polymer with Thymine Groups in the Side Chains: Charge Mobility Enhancement and Application for Selective Field-Effect Transistor Sensors toward CO and H_2S. *Chemistry of Materials* **2019,** *31(5)*, 1800-1807, DOI: 10.1021/acs.chemmater.9b00106
19. Lin, Z., Guo, X., Zhou, L., Zhang, C., Chang, J., Wu, J., Zhang, J. Solution-Processed High Performance Organic Thin Film Transistors Enabled by Roll-to-Roll Slot Die Coating Technique. *Organic Electronics* **2018**, *54*, 80-88, DOI: 10.1016/J.ORGEL.2017.12.030
20. Cheng, X., Caironi, M., Noh, Y., Wang, J., Newman, C., Yan, H., Facchetti, A., Sirringhaus, H. Air Stable Cross-Linked Cytop Ultrathin Gate Dielectric for High Yield Low-Voltage Top-Gate Organic Field-Effect Transistors. *Chemistry of Materials* **2010**, *22(4)*, 1559-1566, DOI: 10.1021/cm902929b
21. Hwang, D., Fuentes-Hernandez, C., Kim, J., Potscavage, W., Kippelen, B. Flexible and Stable Solution-Processed Organic Field-Effect Transistors. *Organic Electronics* **2011**, *12(7)*, 1108-1113, DOI: 10.1016/J.ORGEL.2011.04.002
22. Baeg, K., Noh, Y., Kim, D. Charge Transfer and Trapping Properties in Polymer Gate Dielectrics for Non-Volatile Organic Field-Effect Transistor Memory Applications. *Solid-State Electronics* **2009**, *53(11)*, 1165-1168, DOI: 10.1016/J.SSE.2009.07.003
23. Cheng, C., Lee, Y., Chi, L., Chen, Y., Hung, S., Ling, L. Bacterial Penetration Through Antibiotic-Loaded Guided Tissue Regeneration Membranes. *Journal of Periodontology* **2009**, *80(9)*, 1471-1478, DOI: 10.1902/JOP.2009.090044

24. Sacar, M., Goksin, I., Baltalarli, A., Turgut, H., Sacar, S., Onem, G., Ozcan, V., Adali, F. The Prophylactic Efficacy of Rifampicin-Soaked Graft in Combination with Systemic Vancomycin in the Prevention of Prosthetic Vascular Graft Infection: An Experimental Study. *Journal of Surgical Research* **2005**, *129(2)*, 329-334, DOI: 10.1016/J.JSS.2005.05.017
25. Al Meslmani, B., Mahmoud, G., Bakowsky, U. Development of Expanded Polytetrafluoroethylene Cardiovascular Graft Platform Based on Immobilization of Poly lactic-co-Glycolic Acid Nanoparticles Using a Wet Chemical Modification Technique. *International Journal of Pharmaceutics* **2017**, *529(1-2)*, 238-244, DOI: 10.1016/J.IJPHARM.2017.06.091
26. Turco, M., Buchbinder, M., Popma, J., Weissman, N., Mann, T., Douceet, S., Johnson, W., Greenberg, J., Leadley, K., Russell, M. Pivotal, Randomized U.S. Study of the Symbiot^{TM} Covered Stent System in Patients with Saphenous Vein Graft Disease: Eight-Month Angiographic and Clinical Results from the Symbiot III Trial. *Catheterization and Cardiovascular Interventions* **2006**, *68(3)*, 379-388, DOI: 10.1002/CCD.20873
27. Briguori, C., Sarais, C., Sivieri, G., Takagi, T., Di Mario, C., Colombo, A. Polytetrafluoroethylene-Covered Stent and Coronary Artery Aneurysms. *Catheterization and Cardiovascular Interventions* **2002**, *55(3)*, 326-330, DOI: 10.1002/CCD.10063
28. Formichi, M., Guidoin, R., Jausseran, J., Awad, J., Johnston, K., King, M., Courbier, R., Marois, M., Rouleau, C., Batt, M., Girard, J., Gosselin, C. Expanded PTFE Prostheses as Arterial Substitutes in Humans: Late Pathological Findings in 73 Excised Grafts. *Annals of Vascular Surgery* **1988**, *2(1)*, 14-27, DOI: 10.1007/BF03187341
29. Chevallier, P., Janvier, R., Mantovani, D., Laroche, G. In Vitro Biological Performances of Phosphorylcholine-Grafted ePTFE Prostheses Through RFGD Plasma Techniques. *Macromolecular Bioscience* **2005**, *5(9)*, 829-839, DOI: 10.1002/MABI.200500088
30. Xiao, P., Li, J., Tang, H., Wang, Z., Pan, M. Physically Stable and High Performance Aquivion/ePTFE Composite Membrane for High Temperature Fuel Cell Application. *Journal of Membrane Science* **2013**, *442*, 65-71, DOI: 10.1016/J.MEMSCI.2013.04.014
31. Jie, Z., Haolin, T., Mu, P. Fabrication and Characterization of Self-Assembled Nafion-SiO2-ePTFE Composite Membrane of PEM Fuel Cell. *Journal of Membrane Science* **2008**, *312(1-2)*, 41-47, DOI: 10.1016/J.MEMSCI.2007.12.025
32. Yi, Z., Sun, X., Zhao, Y., Guo, Y., Chen, X., Qin, J., Yu, G., Liu, Y. Diketopyrrolopyrrole-Based π-Conjugated Copolymer Containing β-Unsubstituted Quintetthiophene Unit: A Promising Material Exhibiting High Hole-Mobility for Organic Thin-Film Transistors. *Chemistry of Materials* **2012**, *24(22)*, 4350-4356, DOI: 10.1021/cm302341m
33. Xia, W., Peter, C., Weng, J., Zhang, J., Kliem, H., Jiang, Y., Zhu, G. Epitaxy of Ferroelectric P(VDF-TrFE) Films via Removable PTFE Templates and Its Application in Semiconducting/Ferroelectric Blend Resistive Memory. *ACS Applied Materials & Interfaces* **2017**, *9(13)*, 12130-12137, DOI: 10.1021/acsami.7b01571
34. Wittmann, J., Lotz, B., Smith, P. Formation of Highly Oriented Films by Epitaxial Crystallization on Polymeric Substrates. *Progress in Colloid & Polymer Science* **1993**, *92*, 32-38, DOI: 10.1007/BFB0115446
35. Wittmann, J., Smith, P. Highly Oriented Thin Films of Poly(tetrafluoroethylene) as a Substrate for Oriented Growth of Materials. *Nature* **1991**, *352(6334)*, 414-417, DOI: 10.1038/352414a0

36. Mukhopadhyaya, T., Wagner, J. S., Fan, H., Katz, H. E. Design and Synthesis of Air-Stable p-Channel-Conjugated Polymers for High Signal-to-Drift Nitrogen Dioxide and Ammonia Sensing. *ACS Applied Materials & Interfaces* **2020**, *12(19)*, 21974-21984, DOI: 10.1021/acsami.0c04810
37. Horowitz, G., Hajlaoui, R., Bouchriha, H., Bourguiga, R., Hajlaoui, M. The Concept of "Threshold Voltage" in Organic Field-Effect Transistors. *Advanced Materials* **1998**, *10(12)*, 923-927, DOI: 10.1002/(SICI)1521-4095(199808)10:12<923::AID-ADMA923>3.0.CO;2-W
38. Fanelli, R. The Surface Tension of Chloroform. *Journal of the American Chemical Society* **1948**, *70(2)*, 1792-1793.
39. Zdziennicka, A., Krawczyk, J., Szymczyk, K., Jańczuk, B. Components and Parameters of Liquids and Some Polymers Surface Tension at Different Temperature. *Colloids and Surfaces A: Physiochemical and Engineering Aspects* **2017**, *529*, 864-875, DOI: 10.1016/J.COLSURFA.2017.07.002
40. Zosel, A. Studies of the Wetting Kinetics of Liquid Drops on Solid Surfaces. *Colloid & Polymer Science* **1993**, *271(7)*, 680-687, DOI: 10.1007/BF00652830
41. Ma, J., Liu, Z., Wang, Z., Yang, Y., Zhang, G., Zhang, X., Zhang, D. Charge Mobility Enhancement for Diketopyrrolopyrrole-Based Conjugated Polymers by Partial Replacement of Branching Alkyl Chains with Linear Ones. *Materials Chemistry Frontiers* **2017**, *1*, 2547-2553, DOI: 10.1039/C7QM00307B
42. Kwon, H.-J., Gao, C. Y., Tang, X., Hong, J., Park, C. E., Kong, H., Kim, S. H., Yang, H. Comparison of Semiconductor Growth and Charge Transport on Hydrophobic Polymer Dielectrics of Organic Field-Effect Transistors: Cytop vs. Polystyrene. *Organic Electronics* **2020**, *77*, 105485, DOI: 10.1016/j.orgel.2019.105485
43. Hirschberg, R., Scharnberg, M., Schröder, S., Rehders, S., Strunskus, T., Faupel, F. Electret Films with Extremely High Charge Stability Prepared by Thermal Evaporation of Teflon AF. *Organic Electronics* **2018**, *57*, 146-150, DOI: 10.1016/j.orgel.2018.02.040
44. Scharnberg, M., Rehders, S., Adiyaman, Ö., Schröder, S., Strunskus, T., Faupel, F. Evaporated Electret Films with Superior Charge Stability Based on Teflon AF 2400. *Organic Electronics* **2019**, *70*, 167-171, DOI: 10.1016/j.orgel.2019.04.016
45. Horowitz, G., Delannoy, P. An Analytical Model for Organic-Based Thin-Film Transistors. *Journal of Applied Physics* **1991**, *70*, 469-475, DOI: 10.1063/1.350250
46. de Boer, R. W. I., Iosad, N. N., Stassen, A. F., Klapwijk, T. M., Morpurgo, A. F. Influence of the Gate Leakage Current on the Stability of Organic Single-Crystal Field-Effect Transistors. *Applied Physics Letters* **2005**, *86*, 032103, DOI: 10.1063/1.1852089
47. Shi, Y., Liu, J., Hu, Y., Hu, W., Jiang, L. Effect of Contact Resistance in Organic Field-Effect Transistors. *Nano Select* **2021**, *2(9)*, 1661-1681, DOI: 10.1002/nano.202000059
48. Wagner, J., Jang, H.-J., Han, J., Katz, H. E. Enhanced and Unconventional Responses in Chemiresistive Sensing Devices for Nitrogen Dioxide and Ammonia From Carboxylated Alkylthiophene Polymers. *Materials Horizons* **2020**, *7*, 1358-1371, DOI: 10.1039/D0MH00049C
49. Li, H., Dailey, J., Kale, T., Besar, K., Koehler, K., Katz, H. E. Sensitive and Selective NO_2 Sensing Based on Alkyl- and Alklythio-Thiophene Polymer Conductance and Conductance

Ratio Changes from Differential Chemical Doping. *ACS Applied Materials & Interfaces* **2017**, *9(24)*, 20501-20507, DOI: 10.1021/acsami.7b02721
50. Mukhopadhyaya, T., McKeever, N., Katz, H. E., Wondmagegn, W. Polymer Thin Film Transistor Vapor Sensor Analysis, Drift Suppression, and Response Optimization via Circuit Level Strategy. *Journal of Computational Electronics* **2022**, *21*, 1048-1059, DOI: 10.1007/s10825-022-01893-x
51. Katz, H. E. Stabilization and Specification in Polymer Field-Effect Transistor Semiconductors. *ACS Applied Materials and Interfaces* **2022**, *14(14)*, 15861-15870, DOI: 10.1021/acsami.2c00649
52. Wondmagegn, W., Chu, Y., Li, H., Katz, H. E., Huang, J. Simulation of Two-Transistor Parallel and Series Circuits for Gas Sensing Validated by Experimental Data. *Journal of Computational Electronics* **2021**, *20*, 626-634, DOI: 10.1007/s10825-020-01591-6
53. Fan, H., Li, H., Han, J., McKeever, N., Yu, J., Katz, H. E. A Humid-Air-Operable, NO_2-Responsive Polymer Transistor Series Circuit with Improved Signal-to-Drift Ratio Based on Polymer Semiconductor Oxidation. *ACS Sensors* **2019**, *4(12)*, 3240-3247, DOI: 10.1021/acssensors.9b01751
54. Chu, Y., Li, H., Huang, J., Katz, H. E. High Signal-to-Noise Chemical Sensors Based on Compensated Organic Transistor Circuits. *Advanced Materials Technologies* **2019**, *4(10)*, 1900410, DOI: 10.1002/admt.201900410
55. Gore, R. W. Process for Producing Porous Products. US3953566A, **1976**.
56. Bacino, J. E., Hobson, A. R., Strid, J. J. Porous PTFE Materials and Articles Produced Therefrom. US7306729B2, **2007**.
57. Sirringhaus, H. Reliability of Organic Field-Effect Transistors. *Advanced Materials* **2009**, *21(38-39)*, 3859-3873, DOI: 10.1002/adma.200901136
58. Chen, Y., Podzorov, V. Bias Stress Effect in "Air-Gap" Organic Field-Effect Transistors. *Advanced Materials* **2012**, *24(20)*, 2679-2684, DOI: 10.1002/adma.201200455
59. Guo, T-F., Tsai, Z-J., Chen, S-Y., Wen, T-C., Chung, C-T. Influence of Polymer Gate Dielectrics on *N*-Channel Conduction of Pentacene-Based Organic Field-Effect Transistors. *Journal of Applied Physics* **2007**, *101(12)*, 124505, DOI: 10.1063/1.2748869
60. Dagar, J., Yadav, V., Tyagi, P., Singh, R. K., Suman, C. K., Srivastava, R. Effect of Reduction of Trap Charge Carrier Density in Organic Field Effect Transistors by Surface Treatment of Dielectric Layer. *Journal of Applied Physics* **2013**, *114(22)*, 224504, DOI: 10.1063/1.4842856
61. Wang, A., Kymissis, I., Bulovic, V., Akinwande, A. I. Engineering Density of Semiconductor-Dielectric Interface States to Modulate Threshold Voltage in OFETs. *IEEE Transactions on Electron Devices* **2006**, *53(1)*, 9-13, DOI: 10.1109/TED.2005.860633



For Table of Contents Only