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Research Article

# High Mobility Transistors and Flexible Optical Synapses Enabled by Wafer-Scale Chemical Transformation of Pt-Based 2D Layers

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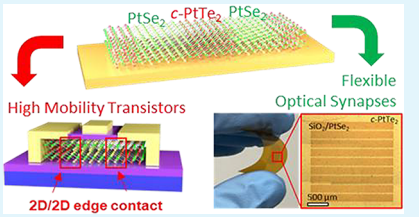
**ABSTRACT:** Electronic devices employing two-dimensional (2D) van der Waals (vdW) transition-metal dichalcogenide (TMD) layers as semiconducting channels often exhibit limited performance (e.g., low carrier mobility), in part, due to their high contact resistances caused by interfacing non-vdW three-dimensional (3D) metal electrodes. Herein, we report that this intrinsic contact issue can be efficiently mitigated by forming the 2D/2D in-plane junctions of 2D semiconductor channels seamlessly interfaced with 2D metal electrodes. For this, we demonstrated the selectively patterned conversion of semiconducting 2D $PtSe_2$ (channels) to metallic 2D $PtTe_2$ (electrodes) layers by employing a wafer-scale low-temperature chemical vapor deposition (CVD) process. We investigated a variety of field-effect transistors (FETs) employing wafer-scale CVD-2D $PtSe_2$/2D $PtTe_2$ heterolayers and identified that silicon dioxide ($SiO_2$) top-gated FETs exhibited an extremely high hole mobility of ~120 $cm^2\ V^{-1}\ s^{-1}$ at room temperature, significantly surpassing performances with previous wafer-scale 2D $PtSe_2$-based FETs. The low-temperature nature of the CVD method further allowed for the direct fabrication of wafer-scale arrays of 2D $PtSe_2$/2D $PtTe_2$ heterolayers on polyamide (PI) substrates, which intrinsically displayed optical pulse-induced artificial synaptic behaviors. This study is believed to vastly broaden the applicability of 2D TMD layers for next-generation, high-performance electronic devices with unconventional functionalities.




**KEYWORDS:** *2D TMD, $PtSe_2$, $PtTe_2$, FET, optical synapse, edge contact, anion exchange, high mobility*



## INTRODUCTION

Two-dimensional (2D) semiconducting transition-metal dichalcogenides (TMDs) have garnered widespread attention due to their exceptional properties, suited to building blocks for next-generation electronic and/or optoelectronic applications such as field-effect transistors (FETs)[1−4] and optosynaptic devices.[5−7] However, despite their promising attributes, the practical application of 2D TMDs in device applications faces a number of technological bottlenecks, e.g., contact[3,4,8] or interface[4,9−14]-related property degradation, scalability and uniformity demanded in material preparation,[15,16] as well as 2D layer interlayer coupling,[17,18] and/or bandgap engineering.[19] Among them, directly interfacing semiconducting 2D TMD layers with three-dimensional (3D) metal electrodes imposes inevitable challenges due to the intrinsic nature of the van der Waals (vdW) molecular bonding inherent to 2D TMD layers. This challenge leads to a variety of issues impeding the performances of 2D TMD layer-based devices such as uncontrollable Schottky barriers,[4,9,10] Fermi pinning,[11−14] and high contact resistance[3,4,8] which should be resolved toward improving and optimizing their device performances, i.e., high carrier mobility, large "on" current,[20] as well as enhanced photoresponsiveness.[21,22] Extensive efforts have been made to overcome such issues, mainly focusing on modifying the interfacial nature of vdW 2D layers/non-vdW metal electrodes through chemical and physical methods.[3,8,23−28] Specifically, seamlessly interfacing semiconducting vdW 2D layers with other metallic vdW 2D layers in place of conventional non-vdW metal electrodes is highly promising in reducing the device contact resistance. This approach of forming "2D/2D edge contacts" by connecting the edges of semiconducting 2D layers (channels) and metallic 2D layers (electrodes) can not only eliminate the tunnel barrier at the channel/electrode interfaces but also is compatible with the chemical vapor deposition (CVD)-based manufacturing process.[20,29−33] However, implementing this idea toward wafer-scale, all 2D layer-based electronic devices has not been rigorously pursued mainly due to a lack of reliable CVD processes to fabricate a large number of 2D/2D edge contact arrays.[30] Accordingly, high-performance all-2D devices benefiting the true potential of the edge contact approach have not been reported, and their projected performance enhancements are largely unknown.

In this work, we investigate a CVD reaction process that can transform semiconducting 2D layers to metallic 2D layers and

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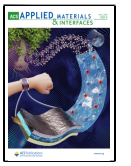

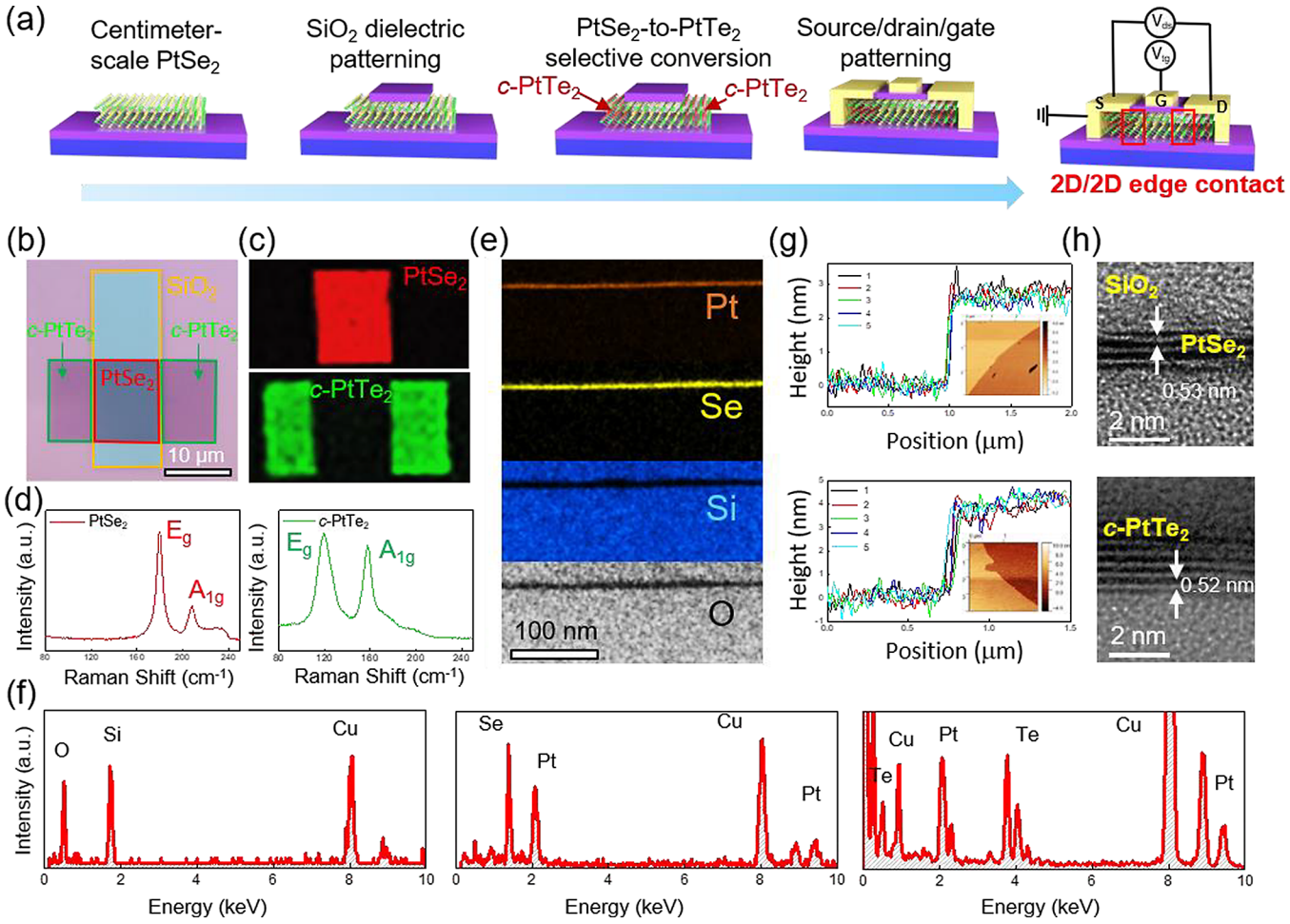


**Figure 1.** (a) Schematics for fabrication of top-gated FETs with 2D/2D edge contacts by selective transformation of semiconducting 2D $PtSe_2$ layers (channels) to metallic 2D *c*-$PtTe_2$ layers (source/drain electrodes). (b) Optical microscope image of $SiO_2$ top-gated 2D $PtSe_2$ FET contacted with 2D *c*-$PtTe_2$ layers. (c) Raman mapping images of 2D $PtSe_2$ (top) and 2D *c*-$PtTe_2$ (bottom) layers obtained from the red and green boxed regions of (b), respectively. (d) Raman spectra of 2D $PtSe_2$ (left) and 2D *c*-$PtTe_2$ (right) layers obtained from the red and green boxed regions of (b), respectively. (e) Cross-sectional EDS mapping images obtained from 2D $PtSe_2$ layers underneath $SiO_2$. (f) EDS spectra obtained from the top $SiO_2$ layers (left), 2D $PtSe_2$ layers underneath $SiO_2$ (middle), and 2D *c*-$PtTe_2$ layers outside $SiO_2$ (right). (g) AFM height profiles obtained from 2D $PtSe_2$ layers (top) and 2D *c*-$PtTe_2$ layers (bottom). The insets are AFM topography images of the corresponding samples. (h) Cross-sectional HR-TEM images of 2D $PtSe_2$ layers (top) and 2D *c*-$PtTe_2$ layers (bottom).

employ this method in realizing a wafer-scale array of semiconducting 2D/metallic 2D edge contacts. Specifically, we demonstrate a low-temperature, one-step CVD conversion of semiconducting 2D platinum diselenide ($PtSe_2$) layers to metallic 2D platinum ditelluride ($PtTe_2$) layers in a spatially controllable and dimensionally scalable manner. This chemical transformation method enables the fabrication of wafer-scale FETs containing an array of 2D $PtSe_2$ layer semiconductor channels seamlessly interfaced with 2D $PtTe_2$ layer metal electrodes in a 2D/2D edge contact manner. We identify that top-gated FETs employing 2D $PtSe_2$/2D $PtTe_2$ edge contacts exhibit an excellent combination of high mobility and high on/off ratios, significantly outperforming previous studies. The low temperature nature of the CVD process further enables the direct integration of all-2D $PtSe_2$/$PtTe_2$ arrays on polymeric substrates, which yield optoelectronic synaptic characteristics essential for artificial neuromorphic devices with mechanical flexibility.

## RESULTS AND DISCUSSION

Figure 1a illustrates the fabrication procedures of 2D $PtSe_2$ layers (channel)-based FETs interfaced with metallic 2D $PtTe_2$ layers (source/drain). Initially, wafer-scale semiconducting 2D $PtSe_2$ layers are directly grown on wafers—i.e., silicon dioxide/silicon ($SiO_2$/Si) or sapphire via a CVD method—or are mechanically integrated onto $SiO_2$/Si wafers following their CVD growth. Subsequently, $SiO_2$ is selectively deposited onto the 2D $PtSe_2$ layers on $SiO_2$/Si, wherein it functions as a dielectric medium for top-gated FETs as well as protecting the 2D $PtSe_2$ layers underneath it. After the $SiO_2$ deposition, the sample undergoes a CVD tellurization reaction as reported in our previous study,[20] which selectively transforms the exposed 2D $PtSe_2$ layers to metallic 2D converted-$PtTe_2$ (*c*-$PtTe_2$) layers, and then gold (Au) is deposited on the edges of the 2D *c*-$PtTe_2$ layers for source/drain patterning as well as on top of the $SiO_2$ protection layer for gate patterning. The last schematic in Figure 1a illustrates the final FET structure, clarifying that semiconducting 2D $PtSe_2$ layer channels are seamlessly "edge-contacted" with metallic 2D *c*-$PtTe_2$ layer electrodes for top-gating measurements. Details about the


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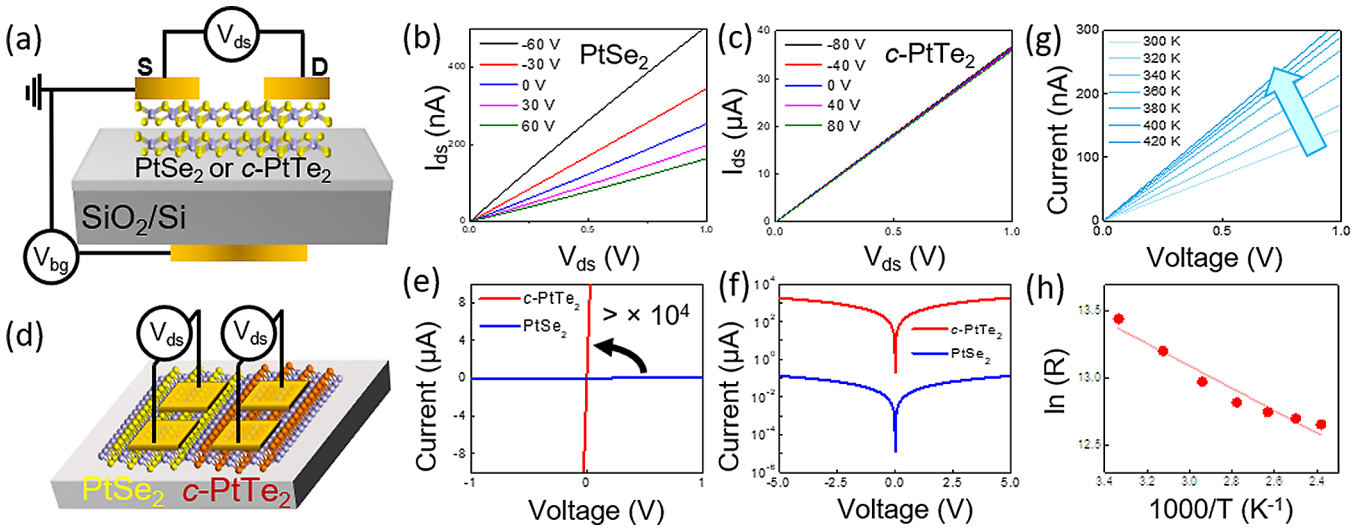


**Figure 2.** (a) Schematic of back-gated FET employing 2D $PtSe_2$ or 2D *c*-$PtTe_2$ layers as channels. (b, c) $I_{ds}$−$V_{ds}$ transfer curves obtained from FET with channels of (b) 2D $PtSe_2$ and (c) 2D *c*-$PtTe_2$ layers, respectively. (d) Schematic of two-terminal measurement for 2D $PtSe_2$ (left) and 2D *c*-$PtTe_2$ (right) layers with seamless lateral interfaces. (e, f): *I*-*V* curves corresponding to (d) obtained from 2D $PtSe_2$ (blue) and 2D *c*-$PtTe_2$ (red) layers in (e) linear and (f) log scales, respectively. (g) Temperature variant $I_{ds}$-$V_{ds}$ characteristics of 2D $PtSe_2$ layers under $V_g$ = 0 V revealing their semiconductor nature. (h) Arrhenius plot corresponding to (g).

CVD growth and conversion procedures are described in the Experimental Section. Figure 1b shows an optical microscope image of a 2D−2D edge-contacted *c*-$PtTe_2$/$PtSe_2$/*c*-$PtTe_2$ heterostructure array with a $SiO_2$ protection layer (orange box) prepared by the procedures described in Figure 1a. Figure 1c presents Raman spectroscopy mapping images of the sample in Figure 1b, confirming a highly localized distribution of 2D $PtSe_2$ (red, top) and 2D *c*-$PtTe_2$ (green, bottom) layers formed only on the locations where they are intended. Figure 1d presents Raman spectra corresponding to Figure 1c, obtained from the 2D $PtSe_2$ (left) and 2D *c*-$PtTe_2$ (right) layers, respectively. Raman peaks assigned to in-plane ($E_g$) and out-of-plane ($A_{1g}$) vibration modes are observed at specific positions, i.e., $E_g$ at ∼175 $cm^{-1}$ and $A_{1g}$ at ∼207 $cm^{-1}$ for 2D $PtSe_2$ layers while $E_g$ at ∼116 $cm^{-1}$ and $A_{1g}$ at ∼157 $cm^{-1}$ for 2D *c*-$PtTe_2$ layers, which are fully consistent with previous studies.[34−37] All of these Raman characterizations strongly evidence that the 2D $PtSe_2$ layers initially outside the $SiO_2$ protection layer become completely transformed to 2D *c*-$PtTe_2$ layers as manifested by the appearance of their Raman characteristics (i.e., green in the Raman mapping/spectra). Meanwhile, the 2D $PtSe_2$ layers underneath the $SiO_2$ layer remain intact against the CVD tellurization reaction (i.e., red in the Raman mapping/spectra). To further clarify the efficacy of the $SiO_2$ layer in protecting 2D $PtSe_2$ layers, we performed cross-sectional transmission electron microscopy (TEM) characterizations. Figure 1e presents cross-sectional energy dispersive X-ray spectrometry (EDS) TEM mapping images obtained from the same 2D $PtSe_2$ layers underneath $SiO_2$ in Figure 1b, revealing the highly homogeneous elemental distribution of Pt, Se, Si, and O. Furthermore, cross-sectional EDS mapping images of 2D *c*-$PtTe_2$ layers obtained after the CVD tellurization are presented in the Supporting Information, Figure S1. Figure 1f displays EDS spectra acquired from the $SiO_2$ protection layer (left), 2D $PtSe_2$ layers underneath $SiO_2$ (middle), and 2D *c*-$PtTe_2$ layers (right), affirming the stoichiometric ratios of ∼1:2 for each 2D material. Figure 1g presents atomic force microscopy (AFM) thickness profiles for 2D $PtSe_2$ (top) and 2D *c*-$PtTe_2$ (bottom) layers, respectively. Figure 1h shows high-resolution (HR) cross-sectional TEM images of the corresponding 2D $PtSe_2$ (top) and 2D *c*-$PtTe_2$ (bottom) layers, consistent with the AFM characterizations. Furthermore, the observation of the horizontally aligned individual 2D basal planes with well-preserved vdW gap spacings of ∼0.52−0.53 nm well agrees with the (001) lattice fringe characteristics of the materials.[34−37]

Before evaluating the performances of FETs employing *c*-$PtTe_2$/$PtSe_2$/*c*-$PtTe_2$ heterostructures, we first focused on characterizing the electrical properties of their individual components, i.e., 2D $PtSe_2$ and 2D *c*-$PtTe_2$ layers, by inspecting FET gate responses. Figure 2a illustrates a schematic of the FET back-gating measurement configuration where 2D $PtSe_2$ and 2D *c*-$PtTe_2$ layers are separately employed as channels. Figure 2b,c presents the FET gate responses of 2D $PtSe_2$ and 2D *c*-$PtTe_2$ layers, respectively, revealing their intrinsic carrier transport types. Highly distinct FET transfer output curves are observed, manifested by $I_{ds}$−$V_{ds}$ characteristics with varying $V_g$, i.e., an increase of $I_{ds}$ with decreasing $V_g$ is observed for 2D $PtSe_2$ layers, indicating their p-type semiconducting transport (Figure 2b), consistent with previous studies.[20,34,35,38] Meanwhile, a complete overlap of $I_{ds}$ irrespective of $V_g$ is observed for 2D *c*-$PtTe_2$ layers, indicating their metallic transport (Figure 2c). This observation strongly confirms that the transformation of 2D $PtSe_2$-to-2D *c*-$PtTe_2$ layers by the CVD tellurization drives the transition of semiconducting-to-metallic transport, accompanying a significant increase in $I_{ds}$. To further clarify the distinct transport characteristics of the materials before/after their transformation, we prepared for 2D $PtSe_2$/2D *c*-$PtTe_2$ heterostructures with in-plane/lateral junctions by selectively transforming 2D $PtSe_2$ layers to 2D *c*-$PtTe_2$ layers. Figure 2d illustrates a schematic of the prepared sample, where individual 2D layers are separately inspected via two-terminal measurements. Figure 2e shows the two-terminal characteristics (i.e., *I*−*V* curves) of semiconducting 2D $PtSe_2$ (blue) and metallic 2D *c*-$PtTe_2$ (red) layers, wherein they are seamlessly interfaced with each other. It is noted that the electrical conductivity of the sample significantly increases by the CVD tellurization-


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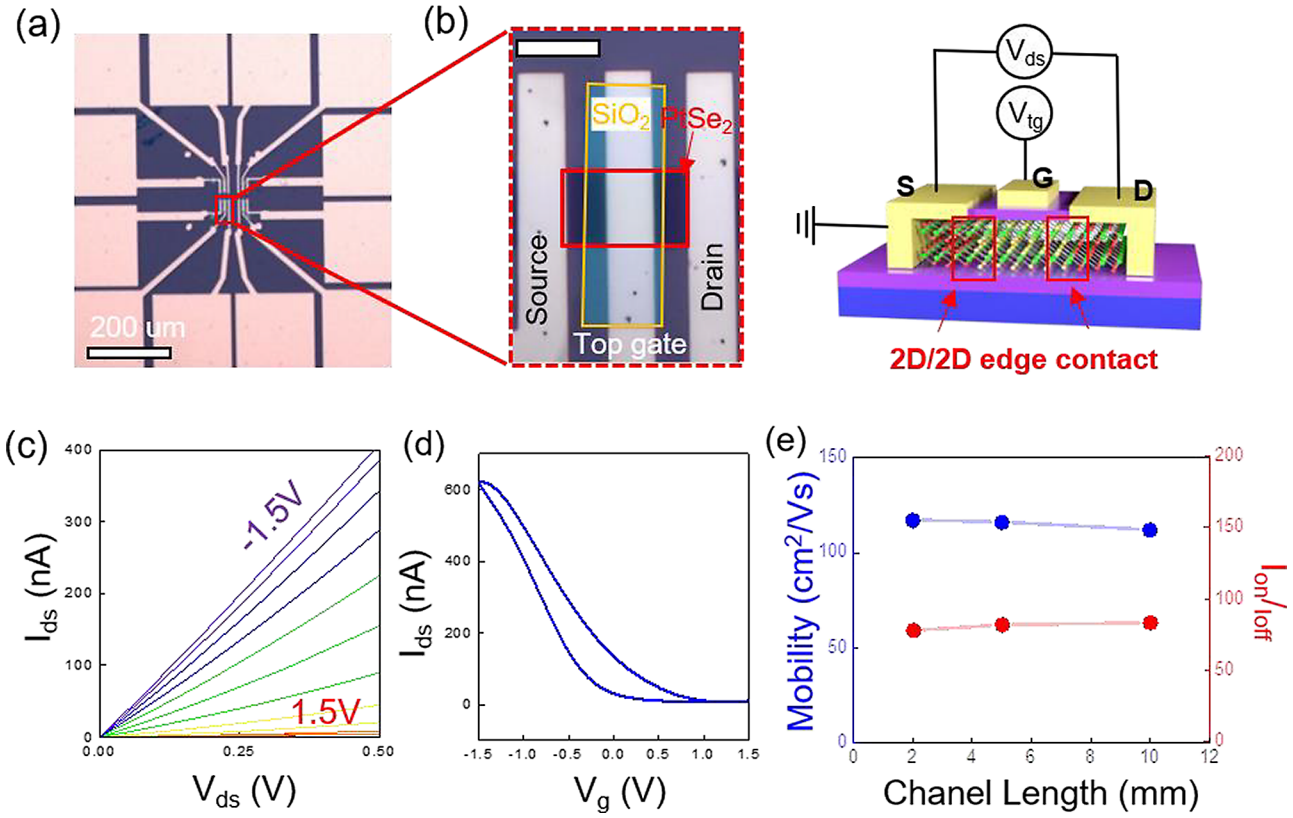


**Figure 3.** (a) Optical microscope image of top-gated 2D $PtSe_2$ FET arrays edge-contacted with 2D *c*-$PtTe_2$ layers. (b) Zoom-in view of single FETs (left) and their corresponding schematic (right) to elucidate structural details of the FETs. Scale is 10 $\mu$m. (c, d) Performances of edge-contacted top-gated FET manifested by (c) $I_{ds}-V_{ds}$ *characteristics under varying top-gate voltages and (d)* $I_{ds}-V_g$ *characteristics at* $V_{ds}$ *= 1 V with 10 μm channel length. (e) Channel length-independent FET mobility and* $I_{on}/I_{off}$ *ratio.*

driven transformation, i.e., >$10^4$ higher conductivity of metallic 2D *c*-$PtTe_2$ layers compared to semiconducting 2D $PtSe_2$ layers. The conductivity values extracted from the two-terminal $I-V$ curves of the metallic *c*-$PtTe_2$ layers and semiconducting 2D $PtSe_2$ layers are $1.0 \times 10^5$ and 7.0 S/m, respectively. Figure 2f presents the log-scale plot of Figure 2e, further highlighting the significant conductivity contrast achieved within the materials maintaining 2D/2D in-plane heterointerfaces. After identifying the intrinsic transport characteristics of the 2D $PtSe_2$ layers and 2D *c*-$PtTe_2$ layers individually, we extended our observations to the heterostructures of *c*-$PtTe_2$/$PtSe_2$/*c*-$PtTe_2$. For this, we specifically focused on the semiconducting transport of 2D $PtSe_2$ layers interfaced with metallic 2D *c*-$PtTe_2$ layers by employing temperature-variant $I-V$ measurements. Figure 2g presents $I-V$ characteristics of 2D $PtSe_2$ layers with metallic 2D *c*-$PtTe_2$ layers employed as electrodes in a varying temperature range of 300−420 K. A significant current increase (~2.2 times) is observed with the increase of temperature by 120 K, which reflects the thermally generated carrier transport within the semiconducting 2D $PtSe_2$ layers, similar to previous observations with other 2D materials.[39−41] From such temperature-dependent conductance variations, the thermal activation energy ($E_a$) for majority carrier transports within semiconductors can be determined at a given temperature, $T$, from the below Arrhenius equation[39,41]

$$\sigma(T) = \sigma_0 \exp\left(-\frac{E_a}{kT}\right)$$

where $\sigma_0$ is the electrical conductivity at $T$ = 0 K and $k$ is Boltzmann's constant. Figure 2h exhibits the Arrhenius plot for the semiconducting 2D $PtSe_2$ layers, yielding an $E_a$ of 72 meV derived from the tangential slope of the linear fitting (red line). An optical microscope image of the actual sample employed for the temperature-dependent measurements as well as its corresponding cross-sectional schematic illustration are presented in the Supporting Information, Figure S2.

Based on the electrical characterizations, we explored performances of FETs employing *c*-$PtTe_2$/$PtSe_2$/*c*-$PtTe_2$, where semiconducting 2D $PtSe_2$ layer channels are top-gated and edge-contacted with metallic 2D *c*-$PtTe_2$ layers. Figure 3a presents a low-magnification optical microscope image of a representative sample, revealing an array of edge-contacted and top-gated FETs. Figure 3b shows a zoomed-in view (left) of a FET with a 10 $\mu$m channel length of semiconducting 2D $PtSe_2$ layers in Figure 3a and its corresponding cross-sectional schematic illustration (right), highlighting the presence of $PtSe_2$/*c*-$PtTe_2$ edge contacts. For this device, the 2D $PtSe_2$ layer channels are embedded underneath a 70 nm thick $SiO_2$ layer which functions as a dielectric medium for top-gating as well as protecting the 2D $PtSe_2$ layers against the subsequent transformation to 2D *c*-$PtTe_2$ layers. Completing the device's architecture, Au contacts are meticulously deposited atop the 2D *c*-$PtTe_2$ layer electrodes and the $SiO_2$ layer gate dielectric assuming the roles of source/drain and top-gating, respectively. The edge-contacted FET arrays were fabricated using electron beam lithography (EBL), whose process details are described in the Experimental Section. Figure 3c presents the output $I_{ds}-V_{ds}$ transfer curve of the FETs in Figure 3b as a function of the


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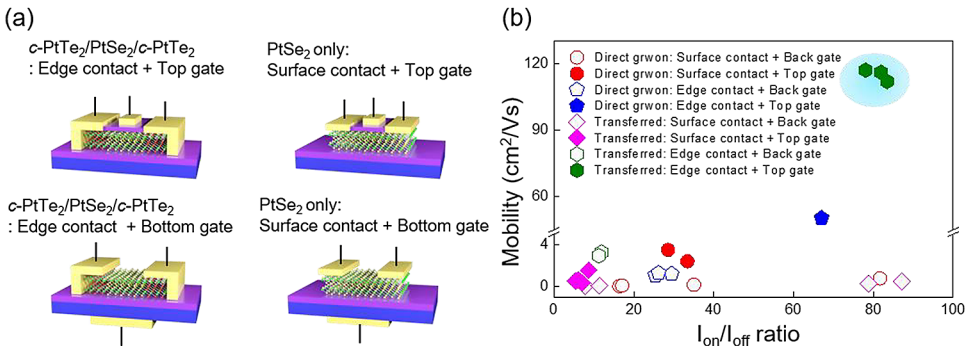


**Figure 4.** (a) Schematic of various bottom- and top-gated FETs employing 2D $PtSe_2$ layer channels with Au surface contacts and 2D *c*-$PtTe_2$ layer edge contacts. (b) Summary of hole mobility and $I_{on}/I_{off}$ obtained from various 2D $PtSe_2$ FETs investigated in this work.

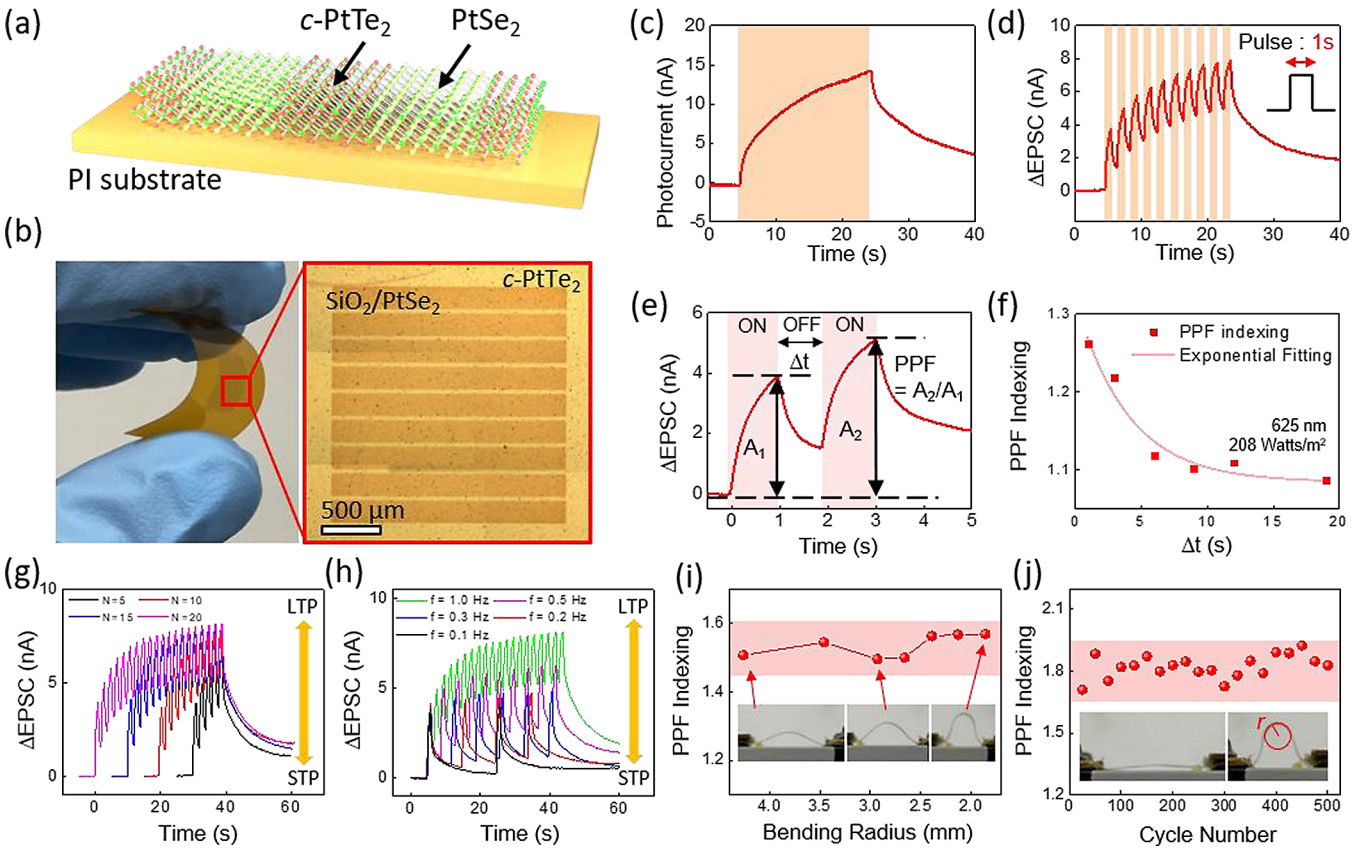


**Figure 5.** (a) Schematic representation of the *c*-$PtTe_2$/$PtSe_2$ array fabricated on a flexible PI substrate. (b) Photographic image of the flexible *c*-$PtTe_2$/$PtSe_2$ array on a PI substrate (left) and its enlarged view (right). (c) Temporal photocurrent response from flexible *c*-$PtTe_2$/$PtSe_2$ device under 625 nm LED illumination for 20 s. (d) Temporal photocurrent response obtained with pulsed optical illumination. (e, f) Optically stimulated synaptic behaviors of flexible *c*-$PtTe_2$/$PtSe_2$ device characterized by (e) PPF index determined from $\Delta E_{PSC}$ responses under two consecutive pulse stimuli, and (f) pulse interval ($\Delta t$)-dependent PPF, (g, h) STP-to-LTP transition obtained by (g) increasing pulse number, and (h) increasing pulse frequency. (i, j) Mechanical robustness of flexible *c*-$PtTe_2$/$PtSe_2$ device manifested by (i) bending strain-invariant PPF indexing, and (j) endurance of PPF indexing across 500 bending cycles.

top-gating voltage ($V_{tg}$), affirming its outstanding p-type characteristics. Additionally, Figure 3d displays the corresponding output curve of the $I_{ds}$–$V_{tg}$ characteristics, providing further evidence of its notable p-type characteristics. The FET hole mobility extracted from the tangential linear slope of the $I_{ds}$–$V_{tg}$ curve[42] is approximately 112 $cm^2\ V^{-1}\ s^{-1}$, accompanied by a current on/off ratio ($I_{on}/I_{off}$) of ~83. We also inspected a large number of FETs with varying channel lengths and identified their influences on FETs' performance parameters. Figure 3e exhibits plots of hole mobility and $I_{on}/I_{off}$ vs channel length values for the edge-contacted top-gated FETs. Remarkably, high hole mobility values exceeding 110 $cm^2\ V^{-1}\ s^{-1}$ are consistently observed irrespective of channel length variations, accompanying channel length-independent $I_{on}/I_{off}$ well. For comparison, these mobility values markedly surpass those from previous studies on CVD-grown 2D $PtSe_2$ FETs,[20,38,43,44] which is particularly encouraging given that our CVD 2D $PtSe_2$ layers are on a lateral dimension of a full wafer scale (>$cm^2$). This significant enhancement of FET mobility values is attributed to the efficient reduction of the contact resistances rising at the interfaces of channels and


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source/drain electrodes, facilitated by the seamless formation of 2D/2D edge contacts as previously validated.[20]

For an in-depth investigation into the performances of CVD-grown 2D $PtSe_2$-based FETs, we fabricated a number of FET arrays in various configurations on identical $SiO_2$/Si wafers (300 nm thickness of $SiO_2$). These include edge-contacted top- or bottom-gated FETs composed of *c*-$PtTe_2$/$PtSe_2$/*c*-$PtTe_2$ as well as Au surface-contacted top- or bottom-gate FETs without 2D *c*-$PtTe_2$ layer edge contacts. Figure 4a illustrates the schematic representations of all fabricated and tested FETs where two types of centimeter-scale 2D $PtSe_2$ layers were employed, i.e., directly grown on $SiO_2$/Si wafers or manually transferred onto $SiO_2$/Si wafers after their CVD growth on sapphire wafers. Details for the growth and transfer procedures are described in the Experimental Section. Figure 4b provides a summary of hole mobility and $I_{on}/I_{off}$ values for all 2D $PtSe_2$-based FETs analyzed in our study, with detailed data available in the Supporting Information, Table S1. This overview demonstrates that edge-contacted and top-gated *c*-$PtTe_2$/$PtSe_2$/*c*-$PtTe_2$ FETs employing transferred CVD-2D $PtSe_2$ layers (lateral dimension > $cm^2$) exhibit superior performances accompanying an excellent combination of high mobility and high $I_{on}/I_{off}$. We also evaluated performances of FETs employing directly grown or mechanically transferred CVD-2D $PtSe_2$ layers with various channel lengths, i.e., 1, 2, 3, 5, and 10 $\mu$m (Supporting Information, Figure S3). All values of hole carrier mobility and $I_{on}/I_{off}$ were calculated from the measured $I_{ds}-V_g$ and $I_{ds}-V_{ds}$ transfer curves.[42] These excellent performances are attributed to various factors associated with multiple process advantages in our FET fabrications. For example, (1) significant reduction of channel/electrode contact resistances enabled by the edge-contact geometry.[20] (2) high-quality growth of 2D $PtSe_2$ layers on single-crystalline sapphire wafers and their water-assisted clean transfer to $SiO_2$/Si wafers without employing wafer etchants.[45−47] (3) enhanced gate controllability and reduced short-channel effects inherent to top-gating operation.[48−50] Further studies will delve deeper into these aspects to better elucidate the underlying mechanisms exclusively contributing to the enhanced FET performances.

Lastly, we further expanded the opportunities of the chemical transformation-driven 2D/2D edge contact approach in realizing unconventional all-2D devices beyond the exploration of FETs. Specifically, we demonstrated artificial optical synapse devices containing a wafer-scale array of *c*-$PtTe_2$/$PtSe_2$ with 2D/2D edge contacts accompanying mechanical flexibility. For this, we noted the low-temperature (i.e., 400 °C) nature of the CVD transformation reaction and leveraged it in directly growing 2D $PtSe_2$ layers on plastic (e.g., polyamide (PI)) substrates and transforming them to *c*-$PtTe_2$ layers without employing layer transfer approaches. Figure 5a illustrates a schematic of *c*-$PtTe_2$/$PtSe_2$ patterns where the 2D $PtSe_2$ layers directly grown on a PI substrate are subsequently transformed to *c*-$PtTe_2$ layers with an aid of the $SiO_2$ protection layer atop the spatially localized pregrown 2D $PtSe_2$ layers. Figure 5b displays a photographic image (left) and its corresponding zoom-in view (right) of an array of *c*-$PtTe_2$/$PtSe_2$ on a PI substrate employed for optical synapses demonstrations as well as demonstrating its mechanical flexibility. Figure 5c presents the time-dependent photocurrent response of the flexible device under continuous optical illumination by a light-emitting diode (LED) with a wavelength of 625 nm. It exhibits a gradual increase in the photocurrent followed by its slow decay upon removing the illumination source, i.e., a typical persistent photoconductivity (PPC) behavior which is an essential feature for facilitating optically controlled learning and forgetting in synaptic devices.[51] In simulating the presynaptic spike stimuli mimicking the biological synaptic inputs, we illuminated the device with a pulsed LED and explored its suitability for artificial synapses by inspecting its excitatory behaviors manifested by the pulse-induced photoresponsiveness. Figure 5d illustrates the time-dependent excitatory postsynaptic current (EPSC) curve recorded in response to the pulsed presynaptic stimuli, which exhibits a continuous increase of the photocurrent, i.e., optical potentiation of the device mimicking synaptic responses in biological systems.[52] Figure 5e displays an EPSC plot showing the photoresponsiveness obtained under two consecutive pulse illuminations, each with a duration and an interval time of one second. It is noted that the EPSC value generated by the second pulse ($A_2$) is larger than that by the first one ($A_1$). This observation indicates that the device intrinsically exhibits synaptic plasticity, termed as paired pulse facilitation (PPF), another essential feature for artificial synaptic devices, which is defined as PPF index = $A_2/A_1 \times 100$.[53,54] Figure 5f displays a trend of PPF indexing with varying interval ($\Delta t$) values defined by two consecutive pulses. The observation of its exponential decay confirms the successful simulation of synaptic learning and memory processes.[55] The temporal decay of PPF over $\Delta t$ typically follows a double exponential decay function[53−55]

$$\text{PPF decay} = 1 + c_1 \times \exp\left(\frac{\Delta t}{\tau_1}\right) + c_2 \times \exp\left(\frac{\Delta t}{\tau_2}\right)$$

where $\tau_1$ and $\tau_2$ represent the characteristic relaxation times of the phases, and $c_1$ and $c_2$ denote the initial magnitudes of the rapid and slow phases, respectively. Beyond the demonstration of the intrinsic synaptic plasticity, we further expanded it to realize the transition between short-term potentiation (STP) and long-term potentiation (LTP) toward fulfilling the learning/memory capability of the *c*-$PtTe_2$/$PtSe_2$ device demanded in artificial synapses.[53−55] For this, we modulated the device conductivity (i.e., synaptic weight) by controlling the number and frequency of the 625 nm LED light pulses. Figure 5g,h presents the time-dependent STP-to-LTP transition obtained from the same device with varying pulse number (Figure 5g) and frequency (Figure 5h), respectively, measured under an illumination intensity of 208 $W/m^2$. The STP-to-LTP transition was manifested by the stronger potentiation of the synaptic weight (i.e., increase in $\Delta E_{PSC}$), enabled by increasing the pulse number (5−20) and frequency (0.1−1 Hz). In both cases, a longer decay time was observed for LTP compared to that for STP, as further supported in the Supporting Information, Figure S4. This extended decay time of LTP is indicative of its role in forming long-term memories, allowing the brain to retain learned information over prolonged periods. In contrast, the shorter decay time of STP suggests its utility in short-term memory and rapid information processing, which is essential for the immediate integration of and response to new information.[55−57] Furthermore, optical pulses of different intensities, i.e., 85 and 140 $W/m^2$, were applied to the device to demonstrate its illumination intensity-variant STP-to-LTP transition characteristics (Supporting Information, Figure S5). In fact, the device exhibits consistent STP-to-LTP transitions at both intensities


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accompanying decreasing EPSC values with decreasing intensities, reflecting its intensity-dependent reduction of photoexcited electron−hole pairs. These results further confirm that the STP-to-LTP transition is an intrinsic feature of our devices, justifying their suitability for optical-stimuli-responsive artificial synapses. Having confirmed the comprehensive synaptic characteristics, we then focused on unveiling the ability of the flexible *c*-$PtTe_2$/$PtSe_2$ device to retain the essential PPF characteristics under severe mechanical deformation. Figure 5i presents the PPF index values of the device mechanically bent with bending radii in a range of 4.3−1.9 mm, revealing its bending strain-invariant characteristics. Additionally, we tested the mechanical robustness of the device subject to a periodic application/release of bending for >500 cycles with a fixed bending radius of 1.9 mm. Figure 5j shows that the device maintained a nearly constant PPF index of 1.7−1.9 throughout the prolonged cyclic endurance test. Both the pulse duration and interval times were set to be 1 s for all synaptic placidity, bending, and endurance tests. These comprehensive studies on the optical synapses of *c*-$PtTe_2$/$PtSe_2$ devices further verify the versatility of our chemical transformation approach in creating a wafer-scale array of atomically thin heterostructures with seamlessly integrated 2D/2D interfaces.

## CONCLUSIONS

In conclusion, we demonstrated the chemical transformation of semiconducting 2D $PtSe_2$ layers to metallic 2D $PtTe_2$ layers and leveraged its opportunities in exploring a variety of all-2D devices. The wafer-scale manufacturability of the approach was confirmed by the spatially patternable $PtSe_2$-to-$PtTe_2$ transformation, which led to fabricating an array of *c*-$PtTe_2$/$PtSe_2$/*c*-$PtTe_2$ heterostructure with 2D/2D edge contacts. CVD 2D $PtSe_2$ layer-based FETs in various configurations were systematically inspected, and the top-gated FETs benefiting from the edge-contacted heterostructures were identified to exhibit remarkable performances, i.e., hole mobility up ∼120 $cm^2/(V\ s)$ at room temperature, which significantly outperformed previous developments. This controlled chemical transformation method was further extended to develop all-2D artificial synapses that are responsive to optical stimuli. The devices directly integrated on PI substrates employing 2*D*/2D edge-contacted heterostructures displayed all essential characteristics demanded in neuromorphic applications, i.e., optically modulated synaptic plasticity and weight coupled with excellent mechanical deformability. Accordingly, this study highlights new methodological aspects of congruently achieving performance enhancements and exotic functionalities in electronic and optoelectronic devices of extreme thinness and practically relevant dimensions.

## EXPERIMENTAL SECTION

**Growth of 2D $PtSe_2$ Layers and Their Conversion to 2D $PtTe_2$ Layers.** We employed CVD selenization for the growth of 2D $PtSe_2$ layers and CVD tellurization for their conversion to 2D $PtTe_2$ layers. Thickness-controlled Pt films were deposited on growth substrates including $SiO_2$/Si (300 nm of $SiO_2$ thickness), sapphire wafers, and PI substrates by using an electron beam evaporator (Thermionics VE-100) at a fixed evaporation rate of 0.05 Å/s. For the CVD selenization and tellurization processes, the Pt-deposited substrates were placed in the central heating zone of a horizontal quartz tube furnace (Lindberg/Blue M Mini-Mite). Subsequently, alumina boats filled with precursor powders (i.e., selenium: 99.9% and tellurium: 99%, Millipore Sigma) were placed inside the quartz tube at the upstream side of the furnace (temperature ∼200 °C) for selenization and tellurization reactions, respectively. The quartz tube was pumped down to a base pressure of ∼25 mTorr, followed by 10 min of purging with argon (Ar) gas to remove any residual organic and oxygen in the tube. The furnace was subsequently heated to 400 °C in 5 °C/min and maintained at that temperature for another 50 min under a continuous supply of Ar gas at a flow rate of 150 standard cubic centimeters per minute (sccm). After the reaction, the quartz tube was naturally cooled to room temperature. For the selective tellurization employed for the fabrication of edge-contacted FETs, a 70 nm $SiO_2$ layer was deposited on top of as-grown 2D $PtSe_2$ layers using the electron beam evaporator.

**Transfer Process of 2D $PtSe_2$ Layers.** 2D $PtSe_2$ layers grown on sapphire wafers were manually transferred onto desired substrates using a layer transfer technique involving poly(methyl methacrylate) (PMMA, Millipore Sigma) and water. Initially, the 2D $PtSe_2$ layer-on-sapphire wafers were coated with a thin layer of PMMA using a spin coater and were left at room temperature overnight. Subsequently, the PMMA-coated 2D $PtSe_2$ layer/sapphire samples were immersed in a potassium hydroxide solution (KOH, Carolina Biological Supply, 4 mol in DI water) on a hot plate at 80 °C for 20 min to dissolve the edge side of the sapphire wafers. The samples were then slowly immersed in deionized (DI) water, which resulted in the delamination of PMMA/2D $PtSe_2$ layers and their floating on the water surface. The floating PMMA/2D $PtSe_2$ layers were transferred to another DI water bath and allowed to be soaked for 20 min. This water rinsing process was repeated three times to eliminate any residual KOH solution. Subsequently, the PMMA/2D $PtSe_2$ layers were integrated onto target substrates (e.g., $SiO_2$/Si wafer, PI substrate) and dried for 15 min. The PMMA/2D $PtSe_2$ layer-integrated substrates were then heated on a hot plate at 220 °C for 5 min, and the PMMA layer was dissolved in acetone (99.9%, Millipore Sigma) for 3 h. Following this step, the 2D $PtSe_2$ layers attached to the target substrates were rinsed with acetone and isopropyl alcohol (IPA). Finally, any residual IPA on the substrates was eliminated using a blast of nitrogen gas.

**Structural and Chemical Characterizations.** Cross-sectional EDS analysis was performed with an FEI Talos F200X TEM. JEOL ARM 200F Cs-corrected TEM was employed for the cross-sectional HR-TEM analysis. For the TEM cross-sectional sample preparation, standard lift-out techniques were employed using a dual-beam focused ion beam (FIB) with a 30 kV gallium (Ga) ion beam system. Raman characterizations were performed with a Horiba LaRAM HR Evolution Nano system using a laser source of 532 nm wavelength.

**FET Device Fabrication and Measurements.** Surface- and edge-contacted 2D $PtSe_2$ FETs were fabricated by the EBL technique using a Zeiss NVision 40 for the precise patterning of 2D layers, $SiO_2$ protection layers, and gold contacts. We first fabricated 2D $PtSe_2$ layers on prepatterned areas of thickness-controlled Pt thin films on top of $SiO_2$/Si wafers using the CVD selenization process. Following this growth step, $SiO_2$ protection layers (70 nm thickness) were patterned and deposited onto the pregrown 2D $PtSe_2$ layers using the e-beam evaporator (Thermionics VE-100). Subsequently, an additional CVD tellurization process was conducted for the selective conversion of 2D $PtSe_2$ layers to 2D $PtTe_2$ layers, yielding a patterned array of edge-contacted *c*-$PtTe_2$/$PtSe_2$/*c*-$PtTe_2$ heterostructures. This additional CVD tellurization process was skipped for the fabrication of surface-contacted FETs. Metal contacts of Ti (3 nm)/Au (50 nm) were deposited on top of 2D $PtSe_2$ layers, 2D *c*-$PtTe_2$ layers, and $SiO_2$ layers using the e-beam evaporator, respectively, for the patterning of the source, drain, and top-gating electrodes. All FET measurements were performed at room temperature in the air using a home-built micromanipulator probe station and a semiconductor parameter analyzer (HP 4156A).

## ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.4c06540.



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Cross-sectional EDS mapping images of $c$-$PtTe_2$ layers; cross-sectional schematic illustration and top-view optical microscope image of an edge-contacted FET; plots of hole mobility and on/off ratio; performance summary of various $Ptse_2$-based FETs; decay curves of $\Delta EPSC$; and STP-to-LTP transition behaviors under varying light intensities (PDF)

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### Author Contributions

Y.J. initiated and led the project. S.S.H. prepared all samples and characterized their properties as well as conducting all device fabrication and measurements. J.-C.S. assisted in the device fabrication and analysis under the supervision of G.-H.L., and Y.J. A.G. contributed to writing the manuscript. J.-H.L., S.-G.L., H.-S.C., and J.H.K. performed TEM characterizations. S.S.H. and Y.J. wrote the manuscript with inputs from all authors.

### Notes

The authors declare no competing financial interest.

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