High-Voltage Phased Array Electronics for Ultrasound Neuromodulation

Ardavan Javid
School of Electrical Engineering and Computer Science
The Pennsylvania State University
University Park, PA, USA
ardavan.javid@psu.edu

Rudra Biswas
School of Electrical Engineering and Computer Science
The Pennsylvania State University
University Park, PA, USA
rfb5659@psu.edu

Sheikh Jawad Ilham
School of Electrical Engineering and Computer Science
The Pennsylvania State University
University Park, PA, USA
sjl6090@psu.edu

Mehdi Kiani
School of Electrical Engineering and Computer Science
The Pennsylvania State University
University Park, PA, USA
mkiani@psu.edu

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***Abstract*—An ultrasound (US) phased array with electronic steering and focusing capability can enable high-resolution, large-scale US neuromodulation in basic research and clinical experiments. For such applications in different subjects (animals and humans), phased array electronics should provide flexibility in generating waveforms with different patterns (stimulation parameters), fine delay resolution between channels, and high voltage across US transducers (generating high US pressure output) over an extended duration. This paper presents 16-channel high-voltage phased array electronics for neuromodulation, capable of driving US transducers with up to 150 V pulses and 5 ns delay resolution while providing a wide range of sonication waveforms. The electronics has been integrated with a custom-made 2 MHz, 16-element US transducer array (4.3×11.7×0.7 mm^3). In measurements, the phased array system achieved up to 6 MPa peak-to-peak US pressure output at a focal depth of 10 mm with a lateral/axial resolution of 0.6/4.67 mm. The beam focusing/steering capability of the system in measurements and the theoretical analysis of the power consumption of the high-voltage driver (along with measured results) have also been provided.**

Keywords— Phased array, high-voltage driver, ultrasound focusing, beamformer, ultrasound transducer, neuromodulation

I. Introduction

Ultrasound (US) has been proven as a promising modality for both exciting and inhibiting neural activities in animals and humans, while exhibiting millimeter-scale spatial resolution [1]. To achieve US stimulation at various targets, conventional systems mechanically move a single element transducer, suffering from mechanical wearing, and limited spatial coverage and beam repositioning speed [2]. However, a phased array system, realized using an array of US transducers and multiple channels of driving electronics (as shown in Fig. 1), can provide electronically controlled steering and focusing of the generated US beam at different locations by modifying the excitation timing of each individual array element, enabling large-scale, high-resolution US neuromodulation [3].

Although several hardware implementations of US phased array electronics exist, they suffer from shortcomings [4]-[8]. The inaccuracy of the delay profile due to the delay profile quantization can degrade the spatial resolution, reduce the US peak pressure output, and cause undesired sidelobes [9]. Additionally, there is a lack of flexibility in providing a wide range of stimulation parameters (Fig. 2), such as US pressure output, sonication frequency (f_S), tone-burst duration (*TBD*), pulse-repetitive frequency (*PRF*), sonication duration (*SD*), inter-stimulus interval (*ISI*), and total stimulation time (*TT*) [1]. This limitation hinders their application in different animal and human subjects in various research and clinical experiments.

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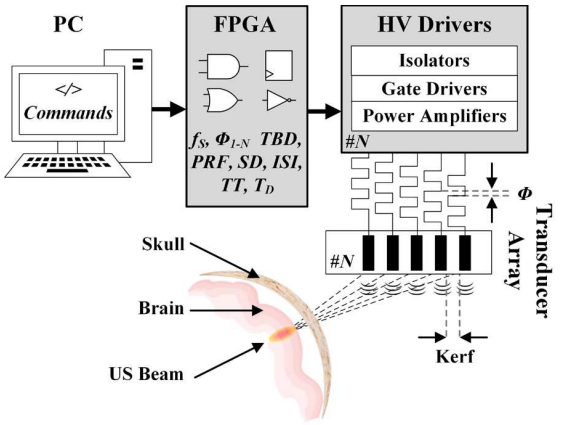

Fig. 1. Simplified schematic of the proposed programmable 16-channel phased array system for ultrasound neuromodulation applications.

The US stimulation application often requires generating sonication waveforms with a large *SD* (e.g., 100s of ms) at a high US pressure output (considering large attenuation of US waves in the skull). Thus, unlike imaging applications, US transducers should be driven with high voltage pulses for extended periods in the US neuromodulation. Consequently, this imposes drastic constraints on the power consumption and thermal dissipation in the driving electronics, particularly when implemented through the application-specific integrated circuit (ASIC) technology. For instance, the low-voltage 8.4 MHz CMOS ASIC in [5] has achieved a low peak-peak US pressure output (USP_{pp}) of < 100 kPa at *SD* of < 1 ms, while utilizing a delay-locked-loop with a phase interpolator with 1.6 ns delay resolution. The high-voltage CMOS ASIC in [6] has achieved USP_{pp} of 1.15 MPa at 2 MHz with *SD* < 300 ms and delay resolution of 31.5 ns (incorporating high clock frequency and digital counters).

Implementing the phased array electronics using discrete components (e.g., [8] with USP_{pp} = 2.2 MPa; *SD* = 13 ms; 5 MHz) can provide more flexibility in generating waveforms

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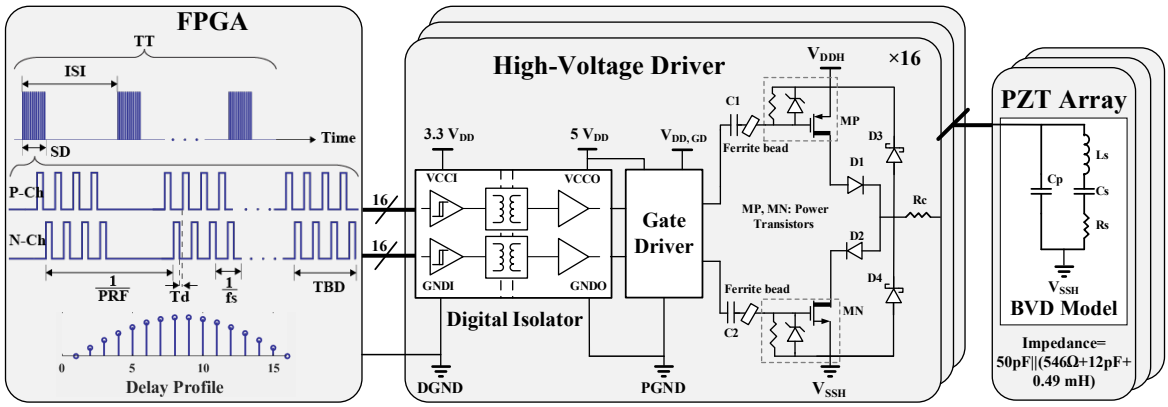

Fig. 2. Detailed block diagram of the implemented 16-channel phased array electronics (in a modular fashion) that can easily be extended to more channels.

with different patterns, fine delay resolution between channels, and high voltage across US transducers (generating high US pressure output) over an extended duration. This paper presents the design, implementation, and testing of a 16-channel high-voltage phased array electronics using discrete components with high degree of flexibility. As shown in Fig. 1, the phased array system consists of a PC for dynamic control of stimulation parameters/target, a field programmable gate array (FPGA) for creating any sonication waveform for each channel with fine delay resolution (5 ns), multi-channel high-voltage (HV) drivers generating up to 150 V pulses, and a US transducer array.

To focus and steer the desired US beam generated by an *N*-element US transducer array (linear array in this work for simplicity) at the target focal depth (F) and azimuthal angle (θ_s), the PC computes the optimal delay profile (Δt_n) for each element (n: 1 to N) based on the US propagation velocity in the medium (c) and the US transducers' interelement spacing (d) [3].

$$\Delta t_n = (F/c)(1 - \sqrt{[1 + (nd/F)^2 - 2nd \times sin(\theta_s)/F]}) \quad (1)$$

The optimal delay profile along with the desired stimulation parameters are sent to the FPGA, generating corresponding signals for the HV drivers.

The paper is organized as follows. Section II describes the system architecture with an emphasis on the HV driver circuit. Section III summarizes the measurement results of the phased array system, followed by the conclusion in Section IV.

II. Phased Array Electronics Design

Fig. 2 depicts the detailed block diagram of the 16-channel phased array electronics (FPGA, HV drivers) for driving a 16-element transducer array. After generating desired waveforms by the FPGA, an isolator level-shifts the signals from the FPGA and provides electrical protection and isolation between FPGA and HV drivers. Gate drivers generate signals to drive power transistors, and switching power amplifiers ultimately drive the transducer arrays. Key design challenges include providing high-power driving capability, minimizing the printed circuit board (PCB) size, effective heat dissipation, and mitigating electromagnetic interference/crosstalk from HV electronics into low-voltage (LV) control circuits.

To drive US transducers at high voltages, a half-bridge class D switching power amplifier structure is chosen as it is more efficient than linear amplifiers (and more compact than other structures). For operation at up to 150 V, several MHz, and 10s of Watts (required for US stimulation), discrete silicon DMOS transistors are utilized for the HV driver design due to the simplicity of their gate driver circuits compared to N-type SiC and GaN transistors. For the 16-channel HV driver, eight Microchip® TC8220 power transistors are used, each containing two pairs of low threshold (V_{th}) vertical N-Ch and P-Ch DMOS transistors (breakdown voltage of 200 V). Each pair is utilized to drive one US element (*MP* and *MN* in Fig. 2). Generated by the FPGA, each *MP* and *MN* pair is driven by nonoverlapping rectangular pulses (at resonance frequency of transducers *fs*, duty cycle of < 50%) with a programmable dead time (T_d), avoiding shorting the HV supply to ground during transitions. The programmability of the dead time can even enable class DE operation [10] with soft switching in the case of driving transducers at a slightly higher frequency than *fs* to improve power efficiency. One should consider that proper operation of class DE is sensitive to transducers' impedance characteristics.

In the HV driver in Fig. 2, Schottky barrier diodes (SBDs) D_3 and D_4 are added to clamp the output to V_{DDH} and ground since the parasitic inductance causes very large ringing on the output node during transitions, which may exceed transistors' breakdown voltage. Due to the Schottky diode's lower forward voltage compared to the minority carrier body-drain diode of the power transistors, $D_{3,4}$ mainly pass the current in this condition, reducing the reverse-recovery current of body diodes. Also, when the body-drain diode of the power transistor is forward biased during the dead time, the abrupt reversed recovery current can activate the parasitic bipolar transistor, leading to the turn-off failure [11]. This is prevented by adding diodes D_1 and D_2 in series with *MN* and *MP* (in addition to Schottky diodes) at the cost of a small power loss ($P_D = V_F \times I_{load,avg}$) across these diodes.

While the dead time prohibits the shoot-through current, the high dV_{DS}/dt and di_D/dt (V_{DS}: drain-source voltage; i_D: drain current) may still turn on the supposedly off power transistor during transition, increasing power dissipation and heat and possibly damaging power transistors. The parasitic gate-drain capacitor (C_{GD}) can transfer the sudden drain voltage jump to the gate if the ratio of C_{GD} and gate-source capacitor (C_{GS}) is not low enough. Also, the parasitic inductances and C_{GD} can cause ringing at the gate. The issue gets even worse at higher driving voltages and frequencies as the radiating electromagnetic field exacerbates interference on the gate driver power line. Although good layout/floor-planning and adding bypass capacitors can help, to effectively mitigate this issue, dV_{out}/dt should be

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decreased by slowing down the power transistors by placing a small resistor (R_C = 56 Ω) in series with each transducer and an optional ferrite bead at the gate, as shown in Fig. 2.

The reverse breakdown and forward voltage of the integrated Zener diode inside the power transistors clamps V_{GS} for protection. The integrated resistor and external C_1 and C_2 capacitors form a fast level shifter to shift gate driver output levels of [0, 5] V to [V_{SSH}, V_{SSH} + 5] V and [V_{DDH} - 5, V_{DDH}] V for *MN* and *MP*, respectively (note that V_{SSH} = 0 in this work). Eight Microchip® MD1822 chips are used for the gate driver. For electrical isolation of HV and LV circuits, eight one-direction transformer-based digital isolators (Analog Device® ADUM3480) are utilized. High data rate (25 Mbps) and high common-mode transient immunity (25 V/ns) of the isolator satisfy the target frequency and high slew rate. The electronics board requires three power supplies: 3.3 V for digital isolators' input side, 5 V for gate drivers and digital isolators' output side, and adjustable V_{DDH} (up to 150 V) for HV drivers. To mitigate heat dissipation in power transistors, passive anodized aluminum heatsinks are mounted on the bottom of the PCB with a soft pad thermal interface material (BERGQUIS® TGP3000). Additionally, the internal ground planes are placed in mid-layers to reduce the interference and act as a heat sink.

The power amplifiers consume the largest amount of power compared to the other blocks. Their power/heat dissipation due to the conduction loss and switching loss is the limiting factor in generating high US pressure output. The power consumption on the HV supply (V_{DDH}) is analyzed here. The switching loss is caused by the parasitic drain-source capacitor (C_{DS}) of the power transistors. During each half cycle, the C_{DS} of the off transistor (either *MN* or *MP*) is charged to V_{DDH} through the V_{DDH} supply. In the subsequent half cycle, C_{DS} is discharged through the on-resistance (R_{DS}) of its own transistor as heat. The consumed power from V_{DDH} is,

$$P_{Switching\ loss} = f_S V_{DDH} Q = f_S V_{DDH} \int_0^{VDDH} C_{DS(V_{DS})} dv_{DS}, \quad (2)$$

as a junction capacitor depends on its reverse voltage,

$$C_{DS(V_{DS})} = \frac{C_{j0}}{\sqrt{1+V_{DS}/V_B}} \approx \frac{C_{j0}}{\sqrt{V_{DS}/V_B}}, \qquad |V_{DS}| \gg |V_B| \quad (3)$$

where C_{j0} is the zero-bias junction capacitance and V_B is the built-in potential. These parameters are not often provided in the datasheet, but C_{DS} can be approximated in any V_{DS} based on an initial given value:

$$C_{DS(V_{DS1})}/C_{DS(V_{DS2})} = \sqrt{V_{DS2}}/\sqrt{V_{DS1}} \quad (4)$$

As for TC8220, the average C_{DS} (equal to C_{OSS} - C_{RSS} from the datasheet) at V_{DS2} = 25 V for *MN* and *MP* is $C_{DS(VDS2=25V)}$ = 12.75 pF. Therefore, the total switching loss from both power transistors can be calculated from,

$$P_{Switching\ loss} \approx 4\sqrt{V_{DS2}} f_S C_{DS(V_{DS2})} \sqrt{V_{DDH}^3}. \quad (5)$$

Since the Schottky diodes $D_{3,4}$ are mostly reversed biased, their large junction capacitances vary with the driving voltage. Similarly, their contributing loss can be estimated from (2).

The conduction loss caused by R_{DS} and R_C depends on the load current. Assuming a high transducer's quality factor, a sinusoidal current, $I_{peak} \sin \omega_s t$, passes through piezoelectric transducer's R_S in Fig. 2 at the first harmonic (fs) of the driving pulses with the duty cycle of $D = 0.5 - Td \times f_S$. For a unipolar square wave (V_{SSH} = 0 in Fig. 2), the amplitude of the fundamental component is $(2V_{DDH} \times sin(\pi D))/\pi$. Thus, the total conduction loss is,

$$P_{Conduction\ loss} = (R_{DS} + R_C) I_{\text{load},rms}^2 = \left(\frac{R_{DS}+R_C}{2}\right)\left(\frac{2V_{DDH}\sin(\pi D)}{\pi(R_S+R_{DS}+R_C)}\right)^2 \quad (6)$$

Fig. 2 shows the Butterworth-Van Dyke (BVD) electrical model of a piezoelectric transducer consisting of two branches, R_S+C_S+L_S and C_P. At the resonant frequency ($f_S = 1/\sqrt{L_S C_S}$), the impedance is reduced to $C_P||R_S$. Only the energy dissipated in R_S contributes to the acoustic power, and the rest is wasted on C_P as heat through charging/discharging via power transistors:

$$P_{dynamic\ loss,PZT} = f_S C_P V_{DDH}^2 \quad (7)$$

$$P_{Accoustic} = R_S I_{Load,rms}^2 = \frac{R_S}{2}\left(\frac{2V_{DDH}\sin(\pi D)}{\pi(R_S+R_{DS}+R_C)}\right)^2 \quad (8)$$

Finally, the total power consumption can be found from,

$$P_{PA,\text{total}} = DC_{PRF} \times (P_{Switching\ loss} + P_{Conduction\ loss} + P_{SBDs} + P_D + P_{dynamic\ loss,PZT} + P_{Accoustic}), \quad (9)$$

where DC_{PRF} is the duty cycle of the *PRF* signal, as shown in Fig. 2.

III. System Integration and Measurement Results

Fig. 3 shows the integrated phased array system and the experimental setup. A 2 MHz, 16-element US array with APC-855 was fabricated following the process in [3]. The array was encapsulated with sylgard-184 and submerged in a deionized water tank. The fabricated array size is 4.3×11.7×0.7 mm^3.

The Xilinx Artix™ 7–XC7A200T FPGA, operating at 200 MHz clock frequency, was programmed to generate a typical US stimulation waveform with *PRF*, *TBD*, *SD*, *ISI*, *TT*, and f_S of 1 kHz, 0.5 ms, 300 ms, 3 s, 18 s, and 2 MHz, respectively (DC_{PRF} = 50%, T_d = 50 ns). Fig. 4a shows the generated FPGA signals for one channel (*N1-P1* driving one *MN-MP* pair in HV driver) out of 32 outputs. Fig. 4b shows the measured waveforms of the HV driver output (V_{DDH} = 100 V) and the received US pressure, which was converted to electrical signal by a calibrated ONDA HGL-0085 hydrophone at F = 10 mm (θ_s = 0º).

The hydrophone was attached to an automated 3-axis motor stage, as described in [3], to scan the lateral-axial plane in front of the array that resulted in 2D beam profiles at different θ_s of -45º, 0º, and 45º, shown in Fig. 5. The measured focal spot at F = 10 mm and θ_s = 0º has a lateral/axial resolution of 0.6/4.67 mm with no significant sidelobes.

Fig. 6a shows the generated US pressure at F = 10 mm (θ_s = 0º) when the array was driven by 10-100 V pulses. The system achieved maximum 6 MPa peak-peak pressure, which is the utmost range for US neuromodulation [1]. Fig. 6a also shows the measured total power consumption of the HV driver with the same stimulation parameters. Table I summarizes the calculated power characteristics of one HV driver channel at V_{DDH} = 80 V and compares it with the measurement result, indicating a good agreement considering the difficulty in accurately modeling piezoelectric transducers. Although the conduction loss is the lowest in Table I, in case of a piezoelectric material with a high electromechanical coupling factor (k_{33}), the conduction loss will be dominant loss, and favorably more electric power will be converted to US power since $C_P\ \alpha\ (1 - k_{33}^2)$ and $R_S\ \alpha\ 1/k_{33}^2$.

Fig. 6b shows the maximum registered temperature of the electronics at the end of TT = 18 s. It was observed that the power

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TABLE I: POWER CONSUMPTION OF THE HV DRIVER

Switching Loss (W)	Cond. Loss (W)	Diodes Loss (W)	PZT Dynamic Loss (W)	US Output Power (W)	Calculated Total Power (W)	Measured Total Power (W)
0.18	0.1	0.84	0.31	0.86	2.31	2.0

At V_{DDH} = 80 V, f_S = 2 MHz, D = 40%, DC_{PRF} = 50%

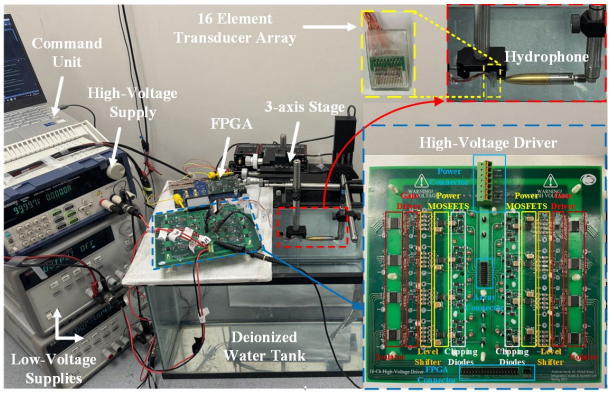


Fig. 3. The integrated phased array system and the experimental setup.

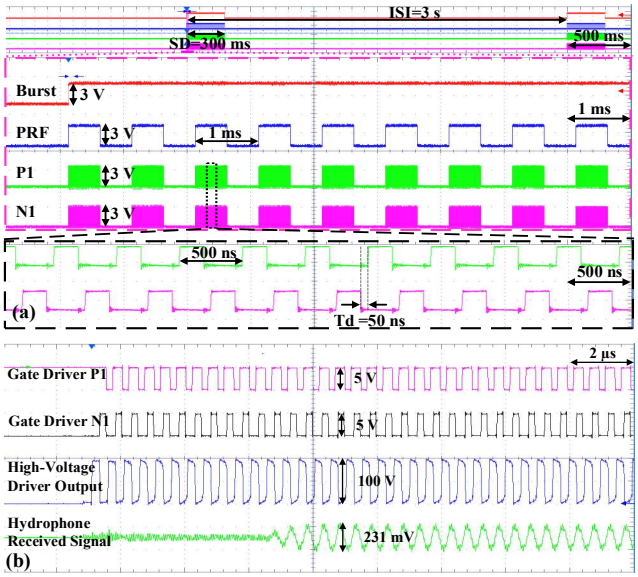


Fig. 4. (a) Measured FPGA signals of one channel: *ISI*, *PRF*, zoomed non-overlapping *MP* and *MN* signals at f_S = 2 MHz. (b) Measured waveforms of the gate diver outputs, 100 V_{PP} driver output, and received US waveforms from a hydrophone at ~10 mm focal depth with 0º steering angle.

transistors were the hottest spot on the board, with only 4.3 ºC temperature increase from the 20.5 °C room temperature.

IV. CONCLUSION

High-voltage 16-channel phased array electronics for US stimulation with high degree of flexibility in waveform and US pressure generation was presented. The system can steer and focus US beams with 5 ns delay resolution and up to 150 V pulses. In measurements, using a 2 MHz piezoelectric transducer array and 100 V pulses, a US beam with 6 MPa pressure output at 10 mm depth was generated with no substantial sidelobes. The functionality of the whole system was demonstrated for different steering angles and driving voltages. Also, the analytical and

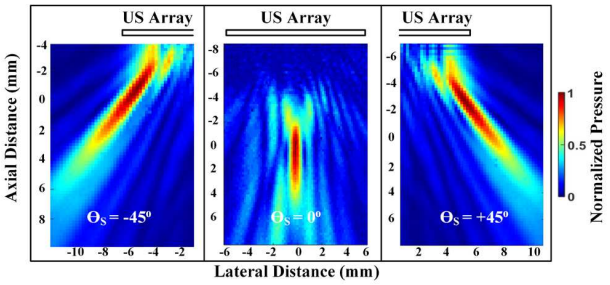
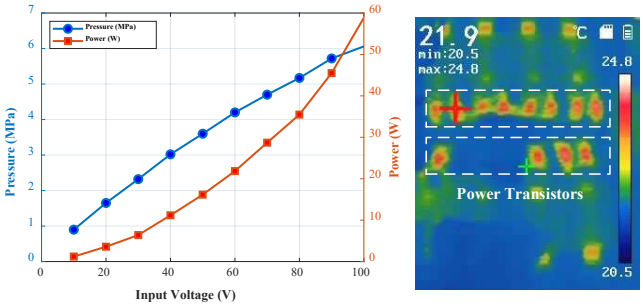


Fig. 5 Measured US beam profiles of the 16-element phased array for beam steering angles of -45º, 0º, and 45º.



(a) (b)

Fig. 6. (a) Measured US pressure output and HV driver power consumption at F = 10 mm. (b)Thermal image of the HV driver at the end of TT = 18 s.

measured power consumption of the HV driver as well as the heat dissipation were evaluated.

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