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A modular 16-channel high-voltage ultrasound phased array system for therapeutic medical applications

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Abstract: An ultrasound (US) phased array with electronic steering and focusing capability can enable high-resolution, large-scale US interventions in various medical research and clinical experiments. For such applications involving different animal subjects and humans, the phased array system must provide flexibility in generating waveforms with different patterns (including experimental parameters), precise delay resolution between channels, and high voltage across US transducers to produce high US pressure output over extended durations. This paper presents a 16-channel high-voltage phased array system designed for therapeutic medical applications, capable of driving US transducers with pulses up to 100 V and a fine delay resolution of 5 ns, while providing a wide range of sonication waveforms. The modular 16-channel electronics are integrated with a custom-built, 2 MHz, 16-element US transducer array with dimensions of 4.3×11.7×0.7 mm^3. In measurements, the phased array system achieved a peak-to-peak US pressure output of up to 6 MPa at a focal depth of 10 mm, with lateral and axial resolution of 0.6 mm and 4.67 mm, respectively. Additionally, the beam focusing and steering capability of the system in measurements and the theoretical analysis of the power consumption of the high-voltage driver (along with measured results) are provided. Finally, the phased array system's ability to steer and focus the ultrasound beam for blood-brain barrier (BBB) opening in different brain regions is successfully demonstrated *in vivo*.

Keywords: ultrasound; phased array; high-voltage driver; beamformer; transducer

1. Introduction

The noninvasive nature of ultrasound (US), combined with its precision when focused, has positioned it as an attractive tool for a range of therapeutic medical applications. Among these applications, focused ultrasound (FUS) has gained significant attention, particularly for its ability to target the nervous system, including the brain [1]. FUS has been successfully employed for various therapeutic purposes such as neuromodulation, temporary blood-brain barrier (BBB) disruption, and thermoablation [2–6]. In neuromodulation applications, FUS has emerged as a promising modality for both stimulating and inhibiting neural activity in various animals and humans, offering millimeter-scale spatial resolution and deep tissue penetration [7–15]. In BBB disruption, FUS has allowed temporary, noninvasive opening of the BBB to facilitate the delivery of therapeutic agents into the brain [3–5].

Achieving precise FUS in different tissue regions presents technical challenges. Traditional systems often rely on a single-element US transducer that is mechanically moved to target different areas [12–19]. While this method has been effective in some cases, it suffers from several limitations, including mechanical wear over time, restricted spatial coverage, and slow beam repositioning speeds [20]. To overcome these limitations, phased array US systems should be developed. A phased array system (as shown in Figure 1) consists of multiple US transducer elements, each driven by separate channels of electronics, allowing for electronically controlled steering and focusing of the US beam. Unlike single-element transducers, phased arrays can achieve beam control by precisely modifying the excitation timing of individual elements, allowing for large-scale, high-resolution US interventions across different regions [21].

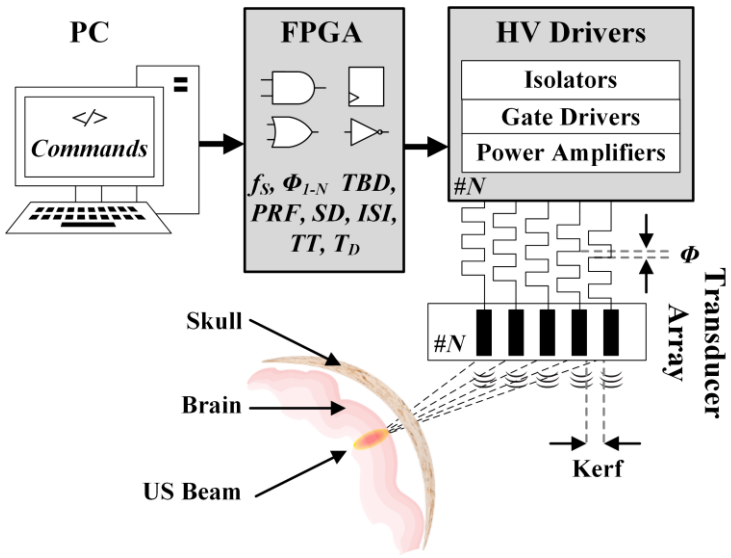


Figure 1. Simplified schematic of the proposed programmable 16-channel US phased array system for therapeutic medical applications.

Although several hardware implementations of US phased array electronics exist, they suffer from shortcomings [22–27]. One issue is the inaccuracy of the delay profile caused by

the delay profile quantization that can degrade the spatial resolution, reduce the US peak pressure output, and cause undesired sidelobes [28]. Accurate delay control is essential for maintaining a sharp focal point and high-intensity US, particularly in applications requiring fine spatial precision such as neuromodulation or BBB disruption. Another significant limitation is the lack of flexibility in providing a wide range of sonication parameters, as described in Figure 2. These include US pressure output, sonication frequency (f_S), tone-burst duration (*TBD*), pulse-repetitive frequency (*PRF*), sonication duration (*SD*), inter-stimulus interval (*ISI*), and total stimulation time (*TT*), which are conventional parameters for US neuromodulation and other FUS applications [1]. These are critical for adapting the system to diverse experimental and clinical needs across different animal and human subjects.

For instance, US stimulation applications often require generating sonication waveforms with a long *SD* (e.g., 100s of ms), while maintaining a high US pressure output to compensate for the significant attenuation of US waves through the skull. Unlike imaging applications, where short pulses are sufficient, some FUS applications such as US neuromodulation and BBB disruption demand that transducers be driven with high-voltage pulses for extended periods. This, in turn, imposes drastic constraints on power consumption and thermal dissipation in the driving electronics, particularly when implemented using application-specific integrated circuit (ASIC) technology. For instance, the low-voltage 8.4 MHz CMOS ASIC in [23] has achieved a low peak-peak US pressure output (USP_{pp}) of < 100 kPa at *SD* of < 1 ms, while utilizing a delay-locked-loop with a phase interpolator with 1.6 ns delay resolution. The high-voltage CMOS ASIC in [24] has achieved USP_{pp} of 1.15 MPa at 2 MHz with *SD* < 300 ms and delay resolution of 31.5 ns (incorporating high clock frequency and digital counters).

Implementing phased array electronics using discrete components, such as in [27] (with USP_{pp} = 2.2 MPa; *SD* = 13 ms; 5 MHz), offers greater flexibility in generating diverse waveforms patterns, achieving fine delay resolution between channels, and maintaining high voltage across US transducers, enabling high US pressure output over extended durations. This paper builds upon our previous work presented in [29], expanding on the design, implementation, and testing of a 16-channel high-voltage phased array system utilizing discrete components, offering a high degree of flexibility in waveform generation and control. As illustrated in Figure 1, the proposed system comprises several key elements: a PC for dynamic control of sonication parameters and target selection, a field-programmable gate array (FPGA) responsible for generating customizable sonication waveforms for each channel with a fine delay resolution of 5 ns, multi-channel high-voltage (HV) drivers capable of delivering pulses up to 100 V, and a US transducer array. This modular architecture allows for precise control and adaptability in a wide range of therapeutic applications, ensuring robust performance across various experimental conditions.

The paper is organized as follows. Section 2 describes the phased array system design, covering the development of the electronics, software, and transducer array. Section 3 summarizes the measurement results of the phased array system. Section 4 provides *in vivo* results, demonstrating the proof of concept for the proposed phased array system in BBB disruption. Finally, Section 5 concludes the paper.

2. Design and development of phased array system

To focus and steer the US beam generated by an *N*-element US transducer array (in this case, a linear array for simplicity) towards the desired focal depth (F) and azimuthal angle (θ_s), a control system (e.g., PC in this work, Figure 1) calculates the optimal delay profile (Δt_n) for each element (n: 1 to N) based on the propagation velocity of the US in the medium (c) and transducers' interelement spacing (d) [21].

$$\Delta t_n = (F/c)(1 - \sqrt{[1 + (nd/F)^2 - 2nd \times sin(\theta_s)/F]}) \quad (1)$$

As shown in Figure 1, the optimal delay profile for accurate beamforming, along with the desired sonication parameters, is sent to the FPGA, generating the corresponding signals for the HV drivers. The multi-channel HV drivers then generate HV pulses across each US transducer element at the sonication frequency (f_S). In this paper, the phased array system operates at f_S = 2 MHz, which is within the range of frequencies for US therapeutic applications [2–6], and can easily be modified in this modular system. This section discusses the design and development of these system components, including the HV drivers, FPGA-based beamformer, and the US transducer array.

2.1. High-voltage driver

Figure 2 illustrates the detailed block diagram of the modular 16-channel phased array electronics (FPGA and HV drivers) designed to drive a 16-element transducer array. After generating desired waveforms by the FPGA, an isolator level-shifts the signals from the FPGA and provides electrical protection and isolation between FPGA and HV drivers. Gate drivers then generate signals to control the power transistors, and the switching power amplifiers ultimately drive the transducer arrays. Key design challenges include providing high-power driving capability, minimizing the printed circuit board (PCB) size, ensuring efficient heat dissipation, and mitigating electromagnetic interference (EMI) and crosstalk from HV electronics into low-voltage (LV) control circuits.

To drive the US transducers at high voltages, a half-bridge class D switching power amplifier structure is chosen as it is more efficient than linear amplifiers (and more compact than other structures). This structure is suitable for operation at voltages up to 100 V, frequencies at several MHz, and power levels of tens of watts, which are required for a wide range of FUS applications. Discrete silicon DMOS transistors are utilized for the HV driver design due to the simplicity of their gate driver circuits compared to N-type SiC and GaN transistors. For the 16-channel HV driver, eight Microchip® TC8220 power transistors are used, each containing two pairs of low threshold (V_{th}) vertical N-Ch and P-Ch DMOS transistors (breakdown voltage of 200 V). Each pair is utilized to drive one US element (*MP* and *MN* in Figure 2). Generated by the FPGA, each *MP* and *MN* pair is driven by nonoverlapping rectangular pulses (at the resonance frequency of the US transducers f_S, duty cycle of < 50%) with a programmable dead time (T_d), avoiding shorting the HV supply to ground during transitions. The programmability of the dead time can even enable class DE

operation [30] with soft switching in the case of driving transducers at a slightly higher frequency than f_S to improve the power efficiency. However, it is important to note that the proper operation of class DE amplifiers is sensitive to the impedance characteristics of the US transducers.

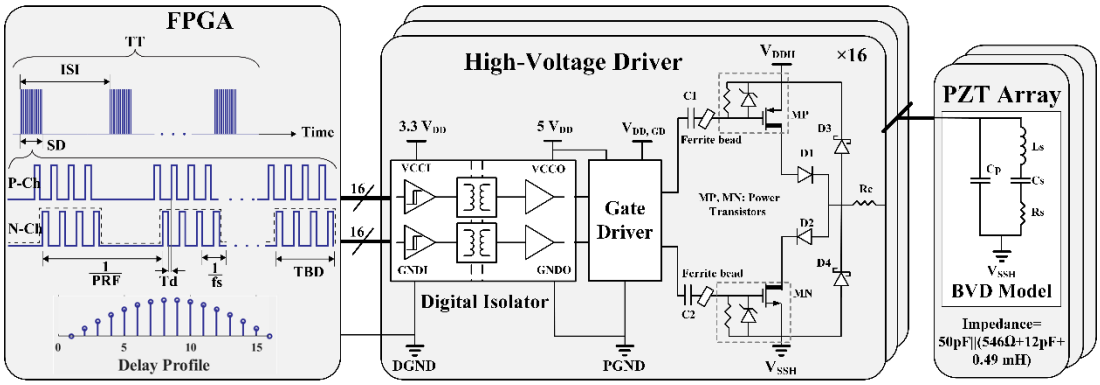


Figure 2. Detailed block diagram of the implemented 16-channel phased array electronics (in a modular fashion) that can easily be extended to more channels.

In the HV driver in Figure 2, Schottky barrier diodes (SBDs) D_3 and D_4 are added to clamp the output to V_{DDH} and ground since the parasitic inductance causes very large ringing on the output node during transitions, which may exceed transistors' breakdown voltage. Due to the Schottky diode's lower forward voltage compared to the minority carrier body-drain diode of the power transistors, $D_{3,4}$ mainly pass the current in this condition, reducing the reverse-recovery current of body diodes. Also, when the body-drain diode of the power transistor is forward biased during the dead time, the abrupt reversed recovery current can activate the parasitic bipolar transistor, leading to the turn-off failure [31]. This is prevented by adding diodes D_1 and D_2 in series with MN and MP (in addition to the Schottky diodes) at the cost of a small power loss ($P_D = V_F \times I_{load,avg}$) across these diodes.

While the dead time prohibits the shoot-through current, the high dV_{DS}/dt and di_D/dt (V_{DS}: drain-source voltage; i_D: drain current) may still turn on the supposedly off power transistor during transition, increasing power dissipation and heat and possibly damaging power transistors. The parasitic gate-drain capacitor (C_{GD}) can transfer the sudden drain voltage jump to the gate if the ratio of C_{GD} and gate-source capacitor (C_{GS}) is not low enough. Also, the parasitic inductances and C_{GD} can cause ringing at the gate. The issue gets even worse at higher driving voltages and frequencies as the radiating electromagnetic field exacerbates interference on the gate driver power line. While good layout and floor-planning design and the use of bypass capacitors can provide some mitigation, a more robust solution is necessary. One approach is to add an extra gate-source capacitor to the MOSFETS to decrease the voltage division between C_{GD} and total C_{GS}, thereby reducing the voltage spikes. However, this increases the power consumption and heat dissipation of the gate drivers. Another option is to utilize a negative voltage instead of ground potential in the gate drivers when turning the MOSFETs off, preventing the voltage spike from reaching the threshold voltage and unintentionally turning the MOSFETs on. However, this solution needs an additional

negative power supply which is not favorable. The third solution involves turning the MOSFET off quickly while slowing down the turning-on time by adding a parallel diode and resistor together series with the gate. A simpler method is to decrease dV_{out}/dt (related to dV_{DS}/dt), where V_{out} is the output voltage across the transducer, by slowing down the power transistors by placing a small resistor (R_C = 56 Ω) in series with each transducer and an optional ferrite bead at the gate, as shown in Figure 2. To remove undesired voltage ringing at the power transistors' gates, a suitable ferrite bead should be selected based on the transducers' operating frequency and the ringing frequency, ensuring that their impedance is high at the ringing frequency and is low at the targeted switching frequency. In this work with the operation at 2 MHz and 100 V, ferrite beads were not required.

The reverse breakdown and forward voltage of the integrated Zener diode inside the power transistors clamps V_{GS} for protection. The integrated resistor and external C_1 and C_2 capacitors form a fast level shifter to shift gate driver output levels of [0, 5] V to [V_{SSH}, V_{SSH} + 5] V and [V_{DDH} - 5, V_{DDH}] V for *MN* and *MP*, respectively (note that V_{SSH} = 0 in this work). Eight Microchip® MD1822 chips are used for the gate driver. For electrical isolation of HV and LV circuits, eight unidirectional transformer-based digital isolators (Analog Device® ADUM3480) are utilized. A high data rate of 25 Mbps and high common-mode transient immunity of 25 V/ns of the isolator satisfy the target frequency and high slew rate. Additionally, the power ground (*PGND*) and digital ground (*DGND*) are separated to prevent ground loops and isolate the noisy ground of HV circuits from the ground of LV circuits, which are highly susceptible to disruption (for unipolar outputs in this paper, V_{SSH} is connected to *PGND*). The electronics board requires three power supplies: 3.3 V for digital isolators' input side, 5 V for gate drivers and digital isolators' output side, and adjustable V_{DDH} of up to 100 V for HV drivers. To mitigate heat dissipation in power transistors, passive anodized aluminum heatsinks are mounted on the bottom of the PCB with a soft pad thermal interface material (BERGQUIS® TGP3000). Additionally, the internal ground planes are placed in mid-layers to reduce the interference and act as a heat sink.

The power amplifiers consume the largest amount of power compared to the other blocks. Their power consumption and heat dissipation due to the conduction loss and switching loss is the limiting factor in generating a high US pressure output. The power consumption on the HV supply (V_{DDH}) is analyzed here. The switching loss is caused by the parasitic drain-source capacitor (C_{DS}) of the power transistors. During each half cycle, the C_{DS} of the off transistor (either *MN* or *MP*) is charged to V_{DDH} through the V_{DDH} supply. In the subsequent half cycle, C_{DS} is discharged through the on-resistance (R_{DS}) of its own transistor as heat. The consumed power from V_{DDH} is,

$$P_{Switching\ loss} = f_S V_{DDH} Q = f_S V_{DDH} \int_0^{VDDH} C_{DS(V_{DS})} dv_{DS} \tag{2}$$

as a junction capacitor depends on its reverse voltage,

$$C_{DS(V_{DS})} = \frac{C_{j0}}{\sqrt{1+V_{DS}/V_B}} \approx \frac{C_{j0}}{\sqrt{V_{DS}/V_B}}, \qquad |V_{DS}| \gg |V_B| \tag{3}$$

where C_{j0} is the zero-bias junction capacitance and V_B is the built-in potential. These parameters are not often provided in the datasheet, but C_{DS} can be approximated in any V_{DS} based on an initial given value:

$$C_{DS(V_{DS1})}/C_{DS(V_{DS2})} = \sqrt{V_{DS2}}/\sqrt{V_{DS1}} \quad (4)$$

As for TC8220, the average C_{DS} (equal to C_{OSS} - C_{RSS} from the datasheet) at V_{DS2} = 25 V for *MN* and *MP* is $C_{DS(VDS2=25V)}$ = 12.75 pF. Therefore, the total switching loss from both power transistors can be calculated from,

$$P_{Switching\ loss} \approx 4\sqrt{V_{DS2}} f_S C_{DS(V_{DS2})} \sqrt{V_{DDH}^3}. \quad (5)$$

Since the Schottky diodes $D_{3,4}$ are mostly reversed biased, their large junction capacitances vary with the driving voltage. Similarly, their contributing loss can be estimated from (2).

The conduction loss caused by R_{DS} and R_C depends on the load current. Assuming a high transducer's quality factor, a sinusoidal current, $I_{peak} \sin \omega_s t$, passes through piezoelectric transducer's R_S in Figure 2 at the first harmonic (f_S) of the driving pulses with the duty cycle of $D = 0.5 - T_d \times f_S$. For a unipolar square wave (V_{SSH} = 0 in Figure 2), the amplitude of the fundamental component is $(2V_{DDH} \times sin(\pi D))/\pi$. Thus, the total conduction loss is,

$$\mathrm{P_{Conduction\ loss}} = (\mathrm{R_{DS} + R_C})\mathrm{I_{load,rms}^2} = (\frac{\mathrm{R_{DS}+R_C}}{2})(\frac{2\mathrm{V_{DDH}}Sin(\pi D)}{\pi(\mathrm{R_S+R_{DS}+R_C})})^2 \quad (6)$$

Figure 2 shows the Butterworth-Van Dyke (BVD) electrical model of a piezoelectric transducer consisting of two branches, R_S+C_S+L_S and C_P. At the resonant frequency ($f_S = 1/\sqrt{L_S C_S}$), the impedance is reduced to $C_P \parallel R_S$. Only the energy dissipated in R_S contributes to the acoustic power, and the rest is wasted on C_P as heat through charging/discharging via power transistors:

$$P_{dynamic\ loss,PZT} = f_S C_P V_{DDH}^2 \quad (7)$$

$$P_{Accoustic} = R_S I_{Load,rms}^2 = \frac{R_S}{2}(\frac{2\mathrm{V_{DDH}Sin}(\pi D)}{\pi(\mathrm{R_S+R_{DS}+R_C})})^2 \quad (8)$$

Finally, the total power consumption of the HV driver can be found from,

$$P_{PA,\mathrm{total}} = DC_{PRF} \times (P_{Switching\ loss} + P_{Conduction\ loss} + P_{SBDs} + P_D + P_{dynamic\ loss,PZT} + P_{Accoustic}), \quad (9)$$

where DC_{PRF} is the duty cycle of the *PRF* signal, as shown in Figure 2.

2.2. Beamformer: software-hardware co-design platform and FPGA implementation

The software-hardware co-design platform for implementing the beamformer with adjustable sonication pattern consists of a Xilinx-based FPGA, Artix-7 (XC7A200T 484FBG-1, AMD, Santa Clara, CA), along with a compatible development board, XEM7310MT-A200 (Opal

Kelly, Portland, OR), and an associated Opal Kelly breakout board, BRK7310MT. The XC7A200T FPGA, with its large number of system logic cells (flip-flops, lookup tables, and distributed/block random-access memory cells), provides the necessary computational resources and onboard memory for high-performance, dynamic digital signal processing tasks. The XEM7310MT-A200 development board includes several key peripherals, such as a USB 3.0 microcontroller, a significant amount of system and FPGA flash memory, expandable DDR3 SDRAM, and high-frequency crystal oscillators. The USB 3.0 microcontroller facilitates seamless communication between the PC's Windows-based microprocessor and the FPGA, making it an ideal software-hardware co-design platform. Such a platform offers a user-friendly application programming interface (API), which is used for US transmit beamforming in this work.

The API is supported by Opal Kelly's *FrontPanel*, a user-friendly software platform designed to simplify FPGA implementation by providing a suite of built-in functions accessible through various high-level programming languages, including Python, C++, and Java, among others. Once the FPGA is configured with the desired architecture, the USB 3.0 microcontroller serves as a communication bridge, enabling dynamic control of the FPGA endpoints from the PC via the *FrontPanel* interface. This capability is essential for dynamically tuning the sonication parameters in the FUS experiment, including the transmit delays for different channels, *TT, ISI, SD, PRF, TBD,* f_S, and T_d (as shown in Figure 2). In this design, Python 3.7 with Spyder 5.1.5 editor was used as the back-end software on the PC to calculate and transmit 16 delay values to the FPGA endpoints for dynamic beamforming.

The Opal Kelly Host Interface (*okHost*), which contains pre-synthesized logic-controlled USB microcontroller, serves as the gateway for *FrontPanel* to control the endpoints within the FPGA. To use *FrontPanel* APIs for dynamic communication, one *okHost* must be included in the design. It is essential to note that, in addition to the user-defined module, the *okHost* interface must be instantiated, synthesized, and appropriately mapped to the FPGA, as shown in Figure 3. The current version of *FrontPanel* supports three functionally distinct types of endpoints: *Wire*, *Trigger*, and *Pipe*. Each endpoint can operate bidirectionally, either from the *okHost* to the end-points or from the end-points to the *okHost*. Examples of available pre-synthesized hardware description language (HDL) modules include *okWireIn*, *okWireOut*, *okPipeIn*, *okPipeOut*, *okTriggerIn*, *okTriggerOut*, and *okRegisterBridge*. In this design, only the *okWireIn* HDL module was incorporated, as it can be seen in Figure 3.

As shown in Figure 3, a user-defined custom module called *Tx_Delay* (written in Verilog) was developed. This module functions as a waveform generator with reconfigurable transmit delays for 16 channels, as well as configurable sonication parameters (*TT*, *ISI*, *SD*, *PRF*, *TBD*, f_S, T_d). An *okHost* HDL module with 16 *WireIn* endpoints was instantiated and integrated with the *Tx_Delay* module. Vivado™ ML Edition 2021.2 (AMD, Santa Clara, CA) was used to create and assimilate all necessary source files, synthesize the design, create necessary testbenches for verifying the *Tx_Delay* module functionalities by behavioral simulations, implement the design, and finally generate bitstreams that can be dynamically loadable from the Widows PC.

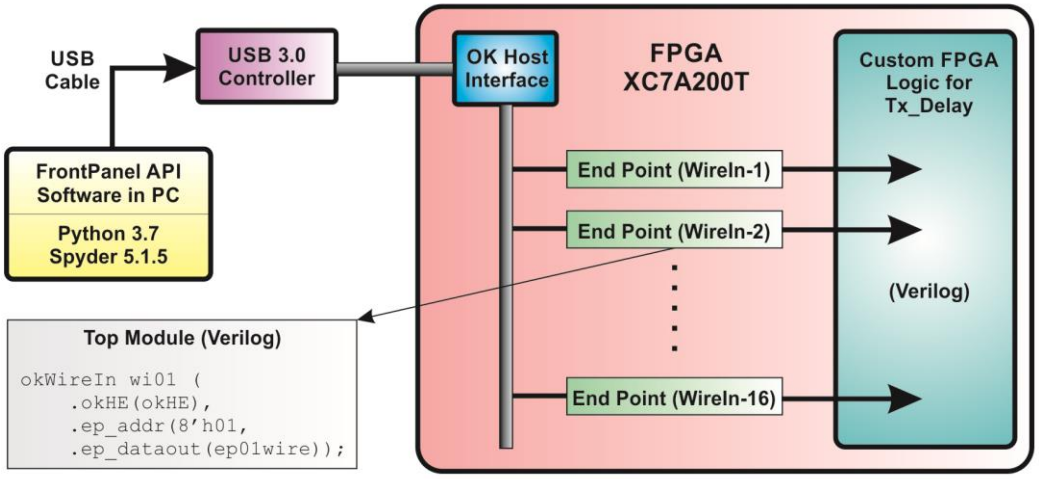


Figure 3. Architecture of the FPGA implementation for sonication pattern generation and dynamic transmit beamforming with reconfigurable FUS parameters.

In the current design, while the transmit delays are dynamically reconfigurable via a Python wrapper from the PC, the sonication parameters can only be reconfigured within the *Tx_Delay* module using Vivado™, requiring a new bitstream to be generated. It is worth mentioning that when using *FrontPanel* APIs, each end-point operation must adhere to a specified address range for proper functionality. For instance, *WireIn* endpoints operate within the address range of 0x00 to 0x1F (as detailed in the *FrontPanel* user guide by Opal Kelly). Therefore, only *WireIn* endpoints were used in this design, which supports asynchronous signaling. Since the number of *WireIn* channels is limited to 16 (each having 32 bits length), dynamic reconfiguration of transmit delays was prioritized for dynamic beam focusing and steering through beamforming, whereas the sonication parameters were reconfigurable within the *Tx_Delay* module.

To maximize flexibility, the *Tx_Delay* module was designed using both top-down and bottom-up approaches in parallel. High-level patterns, such as *ISI* and *1/PRF* (as shown in Figure 2), were generated as periodic trigger pulses, while *SD* and *TBD* were created as periodic rectangular gating signals. It is worth noting that *SD* and *TBD* are defined as *ISI/X* and (*1/PRF/Y*), where *X* and *Y* are *ISI* and (*1/PRF*) dividing integer numbers, respectively. In contrast, low-level patterns, such as nonoverlapping pulses at f_S frequency for driving the P- and N-channel power transistors (Figure 2), were designed independently using a bottom-up approach. For example, first a single cycle of the sonication pulses (with duration of $1/f_S$) was synthesized from the main system clock (200 MHz). This pulse has a duration of $N_{high}+N_{low}$ cycles of the main 200 MHz clock, where N_{high} is the integer number of main clock cycles the pattern remains high, and N_{low} is the integer number of main clock cycles the pattern remains low. This fundamental single cycle (with duration of $1/f_S$) is then repeated N_{cycle} times to form $TBD_{effective}$. As a result, *TBD* (generated using the top-down approach) and $TBD_{effective}$ (created via the bottom-up approach) do not necessarily match, but $TBD_{effective}$ can be gated by *TBD* for a maximum duration to achieve the desired sonication pattern. By integrating

both approaches, a unique sonication pattern generator and transmit-delay logic module was developed, offering unprecedented flexibility.

After successfully designing and verifying the *Tx_Delay* module, a new HDL module (*Top*) was created to integrate it with the *okHost* module, as illustrated in Figure 3. Both *Tx_Delay* and *okHost* modules were instantiated within the *Top* module. Due to the complexity of creating a test bench for the complete design, no additional simulations were performed. Instead, the integrated design was synthesized and implemented directly. For placement and routing, the pin-mapping list provided by Opal Kelly was followed, and a constraint file was created accordingly. The summary of resource utilization and power estimation of the implemented design is included in Figure 4. The highest resource utilization was observed for the I/O pins (29%), followed by the mixed-mode clock manager, MMCM (9%). Power consumption was estimated at 148 mW for static power and 192 mW for dynamic power, with 55% of the dynamic power consumed by the MMCM, making it the largest contributor to power usage. Finally, the bitstream was successfully generated and loaded onto the FPGA using the Python wrapper. Overall, this low-cost, highly flexible multi-channel waveform generator provides an alternative to expensive, commercially available US beamforming technologies for a wide range of FUS applications.

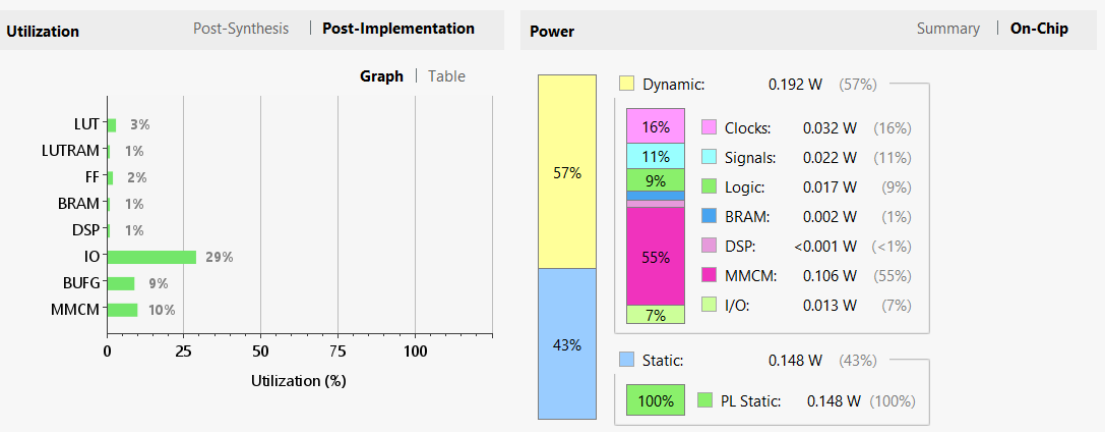


Figure 4. Resource utilization and power estimation summary of the implemented FPGA design from Vivado ™.

2.3. Ultrasound transducer array design and fabrication

As detailed in [21], the geometric design parameters of a linear US phased array transducer play a crucial role in determining its performance. These parameters, shown in Figure 5, include the pitch or inter-element spacing (d), element width (a), element length (L), number of elements (N), total aperture (D), and element thickness (t). To enhance overall system performance, these parameters must be carefully optimized. In [21], a hybrid framework, using k-Wave, a MATLAB toolbox (MathWorks R2023b, Natick, MA) and COMSOL Multiphysics (COMSOL, Inc., Bulington, MA), was presented for optimizing the design parameters of a phased array transducer. The primary objectives were to maximize the US

output pressure (P) while minimizing both the half-power beam volume (V) at the focal point as well as the input power considered through the total effective surface area of the transducer array (NaL). By normalizing the respective parameters exponentially, a new figure of merit was proposed as, FoM = P / ($\sqrt{NaL} \times \sqrt[3]{V}$). Maximizing this FoM enables achieving high US output pressure with high power efficiency and improved spatial resolution.

Unlike US imaging applications where mostly unfocused plane waves are transmitted, the tFUS application requires precisely focused and targeted stimulation. Depending on the design parameters of phased array transducers, unwanted side lobe and/or grating lobe may form, often with magnitudes comparable to the main lobe. Accounting on off-target stimulation, a directivity function was introduced in [31]. Based on this directivity function, the design parameter, inter-element spacing d, is finally selected, which ensures minimization of any off-target sonication. It is worth noting that, by increasing the aperture size D (either by increasing N or d), generally, the directivity can be enhanced. However, the overall improvement becomes marginal with the larger values of N [32], which also is an important consideration for multi-channel electronics design. Following the design methodology outlined in [21], a transducer array was optimized for FUS applications targeting the mouse brain. The design was constrained by the typical dimensions of a mouse head, with maximum allowable D and L of ~ 12 mm and beam focusing and steering range with a focal depth of F = 10 mm. The operation frequency f_S was selected to be 2 MHz. Considering the spatial coverage range, $\theta_{s,max}$ was set to ±45°. Moreover, considering the fabrication constraint of the available minimum dicing blade size, the *kerf* was set as 150 µm. Finally, a 1 mm thick Sylgard-184 layer was put on transducer's surface for electrical isolation and protection.

A 16-element 1D phased array transducer and the corresponding propagation medium were modeled in k-Wave, as shown in Figure 5. The transducer array was aligned parallel to the ***yz*** plane and centered at the origin, with ***xy*** and ***xz*** planes acting as sensors to record the maximum US pressure. To balance high accuracy with manageable computational demands, a grid spacing of 16 points per wavelength (λ) was chosen, corresponding to a grid resolution of 48.75 µm for the operation frequency of 2 MHz with the sound speed of 1540 m/s. The simulation medium was divided into two regions: the initial ***yz*** grid points along ~ 1 mm of the ***x*** axis in Figure 5 (first 20 ***x*** grid points) represented ~ 1 mm thick Sylgard-184 properties, while the remaining region with the volume of ~ 16.2×12.5×6.2 mm^3 (332, 256, and 128 grid points along ***x***, ***y***, and ***z*** axes, respectively) modeled brain tissue. Boundary conditions were managed using a perfect matching layer at the edges of the medium. Acoustic properties, such as sound speed and mass density, were defined for both materials, similar to our previous work [21]. While all the design parameters were optimized in k-Wave, the element thickness (t), which determines the operating frequency (f_S = 2 MHz), was optimized in COMSOL [21].

Following the optimization detailed in [21], the final array dimensions were found to be D×L×t = 11.7×4.3×0.7 mm³. Table 1 summarizes the optimization results, while Figure 6 illustrates the simulated US beam profiles for the optimized 16-element US array. Figure 6 demonstrates the US transducer array capability in focusing and steering US beams at F of 6 mm and 10 mm, with θ_s of 0° and ±45°.

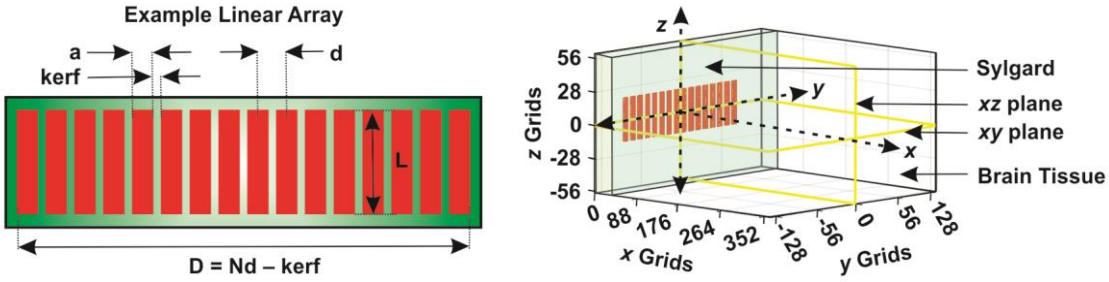


Figure 5. Linear US array and its implementation in k-Wave for its optimization.

Table 1. Optimized US Transducer Array Specifications.

Parameters	Optimal US Array
Sonication Frequency, f_S (MHz)	2
Maximum Focal Distance, F (mm)	10
Number of US Elements, N	16
US Array Aperture, D (mm)	11.7
US Element Length, L (mm)	4.3
US Element Width, a (μm)	520
US Interelement Spacing, d (μm)	670
Maximum Steering Angle, θ_s (deg)	±45
Kerf, *kerf* (μm)	146
US Element Thickness, t (mm)	0.7

After obtaining the optimized design parameters from simulations, we proceeded with the fabrication of the US array. The process, shown in Figure 7(a), began with a large rectangular PZT sheet, 0.7 mm thick, made from APC-855 due to its high electromechanical coupling factor. The sheet was cut into smaller pieces according to the optimized length L = 4.3 mm and aperture D = 11.7 mm, as shown in Figure 7(b). A PCB was designed to interface the array with electronics via a connector. It includes two rows of 18 signal pads and 18 interconnected ground pads, along with a connector mounting layout. The ground pads were coated with conductive silver paint (Leitsilber 200, Ted Pella Inc., Redding, CA) to ensure conductivity. The PZT plate was then mounted on the PCB, and Loctite Epoxy Marine was used to fill gaps and provide mechanical stability during the dicing process, as shown in Figure 7(c). Subsequently, the PZT plate was diced into 18 elements, each approximately 520 μm wide, using a 150 μm thick dicing saw, as depicted in Figure 7(d). Two elements were discarded to account for fabrication imperfections, leaving 16 functional elements, which were manually soldered with 36-AWG wires to their respective excitation pads. In the final step, a layer of Sylgard-184 was applied over the assembled array for electrical insulation and physical protection, as shown Figure 7(e). Finally, the impedance profile of the 16 elements was measured using a network analyzer to verify the ~2 MHz resonant frequency of the fabricated US array, as illustrated in Figure 7(g).

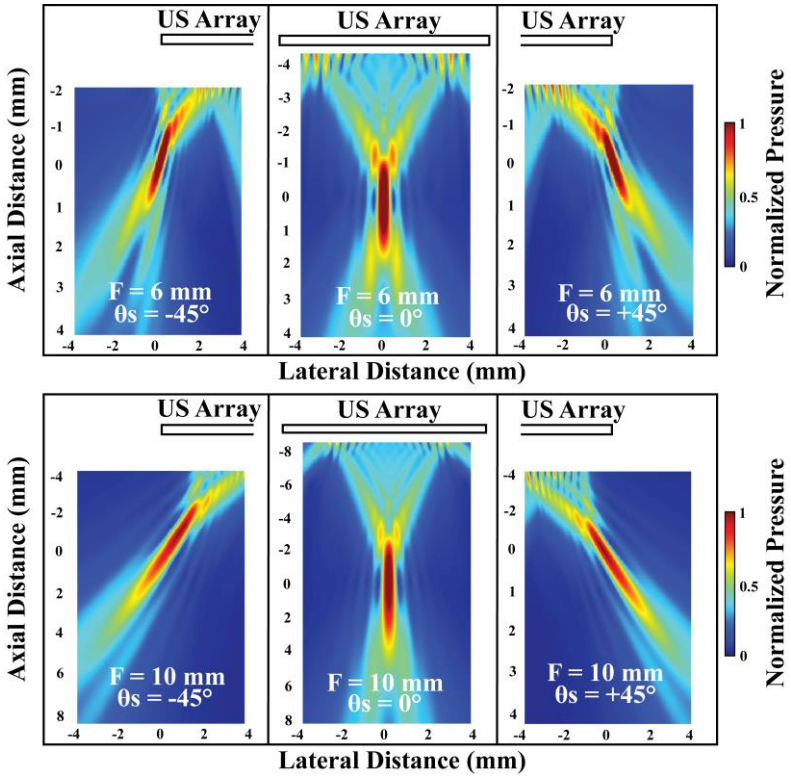


Figure 6. Simulated US beam profiles of the 16-element phased array in Table 1 at focal depths (F) of 6 mm and 10 mm, with beam steering angles of -45º, 0º, and 45º.

3. System Integration and Measurement Results

Figure 8 shows the integrated phased array system and the experimental setup, consisting of US transducer array, HV driver board, beamformer, hydrophone, and 3-axis motorized stage. The US pressure output was measured using a calibrated HGL0085 hydrophone (Onda Corp., Sunnyvale, CA), with a resolution of 85 μm and a bandwidth of 0.25–40 MHz. The hydrophone was positioned using a 3-axis translational stage, equipped with three motorized linear stages (MTS50/M-Z8, Thorlabs, Newton, NJ) allowing for 50 mm of movement along each axis. The hydrophone was connected to a digital oscilloscope through an Onda AG-2010 preamplifier, providing approximately 20 dB of voltage gain. Data acquisition and movement were controlled and automated through a custom MATLAB script. Post-processing of the collected data included filtering out initial electrical interference and generating US beam profiles. The US pressure levels were calculated based on the hydrophone's pressure sensitivity of 38.8 nV/Pa, as per the manufacturer's calibration, with all pressure values reported as peak-to-peak.

Figure 9(a) shows the measured FPGA signals generated for one channel (*N-Ch1*; *P-Ch1*) out of the 32 outputs, driving one *MN-MP* pair in the HV driver. The main system clock used in this design was 200 MHz (one cycle of 5 ns). To synthesize a nonoverlapping sonication waveform at f_S = 2 MHz, the low-level parameters were configured as follows: N_{high} = 40, N_{low} = 60, and N_{cycle} = 10. This yielded a sonication waveform period of $1/f_S = (N_{high} + N_{low})$

× 5 ns = 500 ns, an effective burst duration $TBD_{effective} = (1/f_S) \times N_{cycle}$ = 5 µs, and dead time $T_d = 0.5 \times (N_{low} - N_{high}) \times 5$ ns = 50 ns. The high-level sonication parameters were set as $ISI = 600\times10^6\times5$ ns = 3 s, with an ISI divider X = 10, resulting in $SD = ISI / X = 60\times10^6\times5$ ns = 300 ms; $1 / PRF = 200\times10^3\times5$ ns = 1 ms, and using a divider of Y = 2, this gave $TBD = (1/PRF) / Y = 100\times10^3\times5$ ns = 0.5 ms. Figure 9(b) shows the measured waveforms of the HV driver output (V_{DDH} = 100 V) and the received US pressure, which was converted to electrical signal by the calibrated hydrophone at F = 10 mm ($\theta_s = 0^o$).

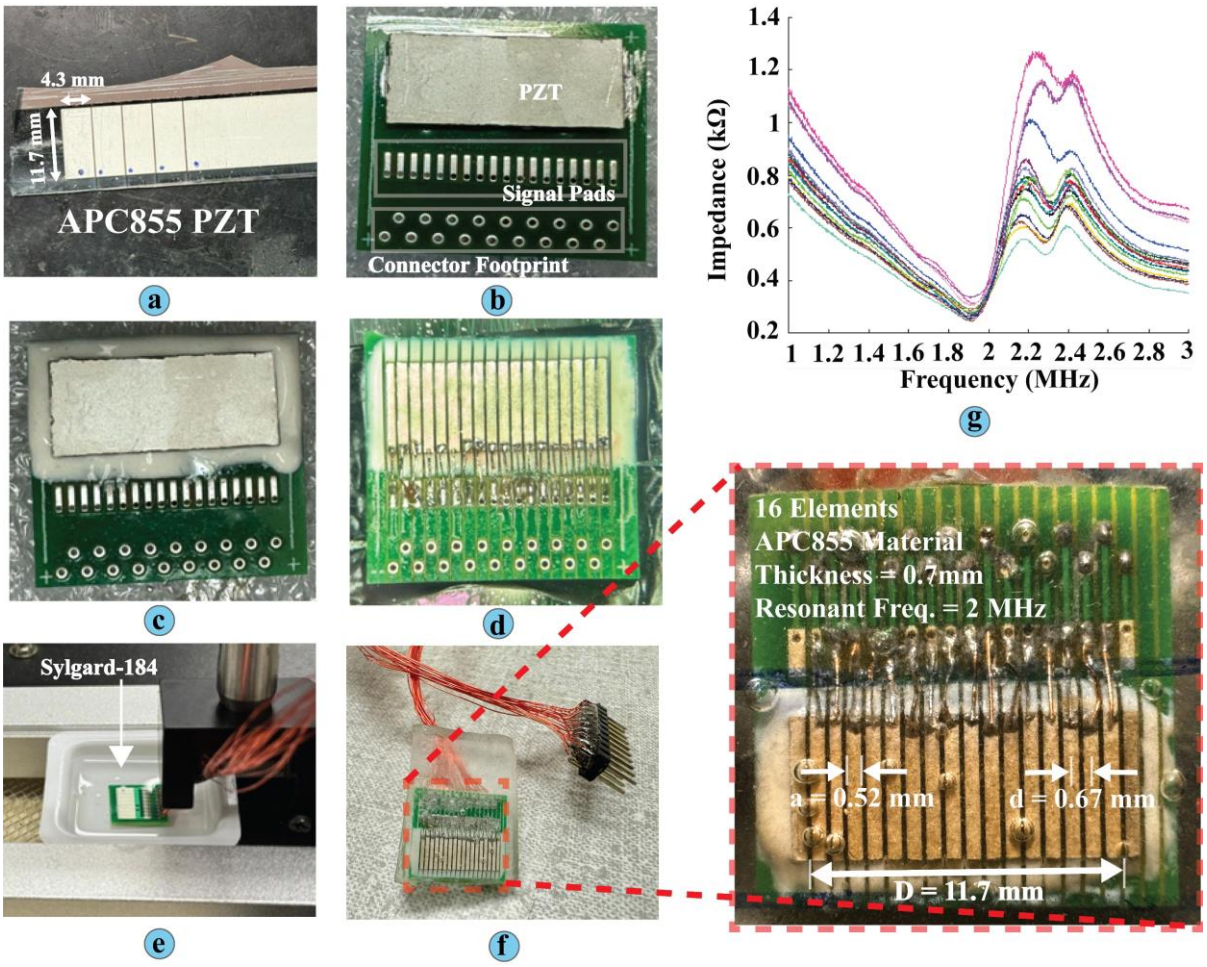


Figure 7. The fabrication steps of the 16-element linear US array. (a) Cut APC 855 PZT sheet to 11.7×4.3 mm^2 rectangular plates. (b) Placement of the PZT plate on a silver paint-coated ground pad. (c) Attachment of the PZT plate to the PCB via epoxy. (d) Connecting top plate of individual elements to their signal pads on the PCB through wire soldering. (e) Coating the device with Sylgard-184 for electrical isolation. (f) Final fabricated device with the detailed microscopic picture. (g) Measured impedance profile of all 16 elements.

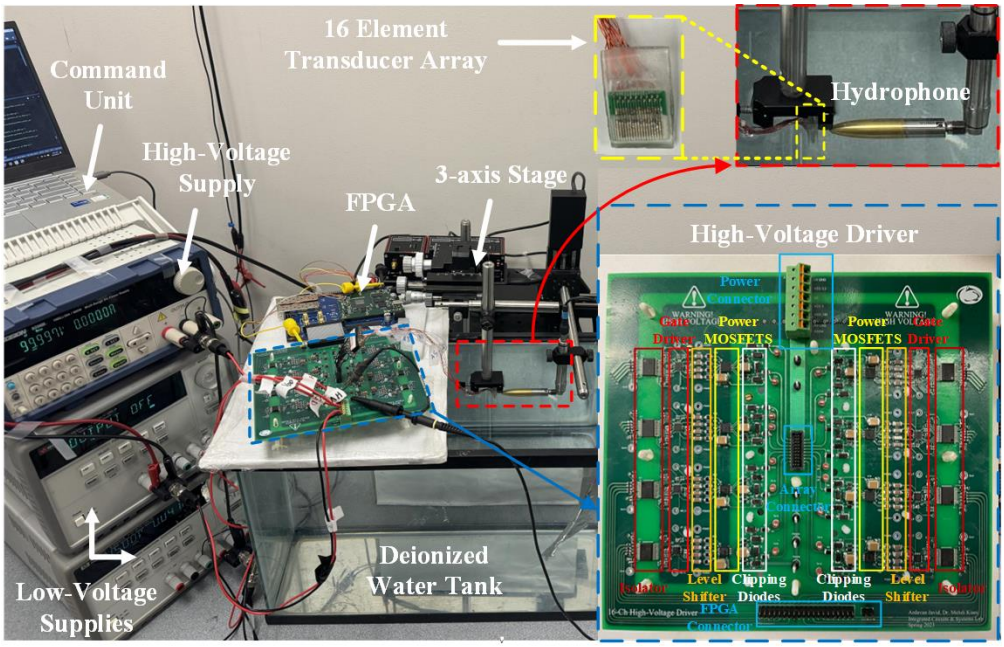


Figure 8. The integrated phased array system and its experimental setup.

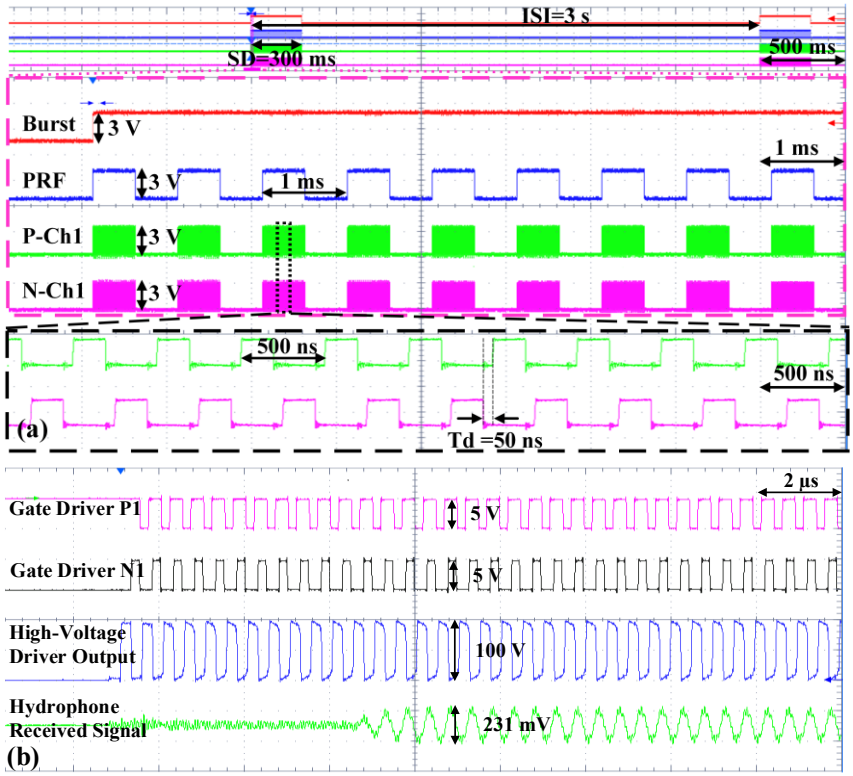


Figure 9. Measured FPGA signals of one channel: *ISI*, *PRF*, zoomed non-overlapping *MP* and *MN* signals at f_S = 2 MHz. (b) Measured waveforms of the gate diver outputs, HV driver output (100 V peak-peak), and received US waveforms from a hydrophone at ~10 mm focal depth with 0° steering angle.

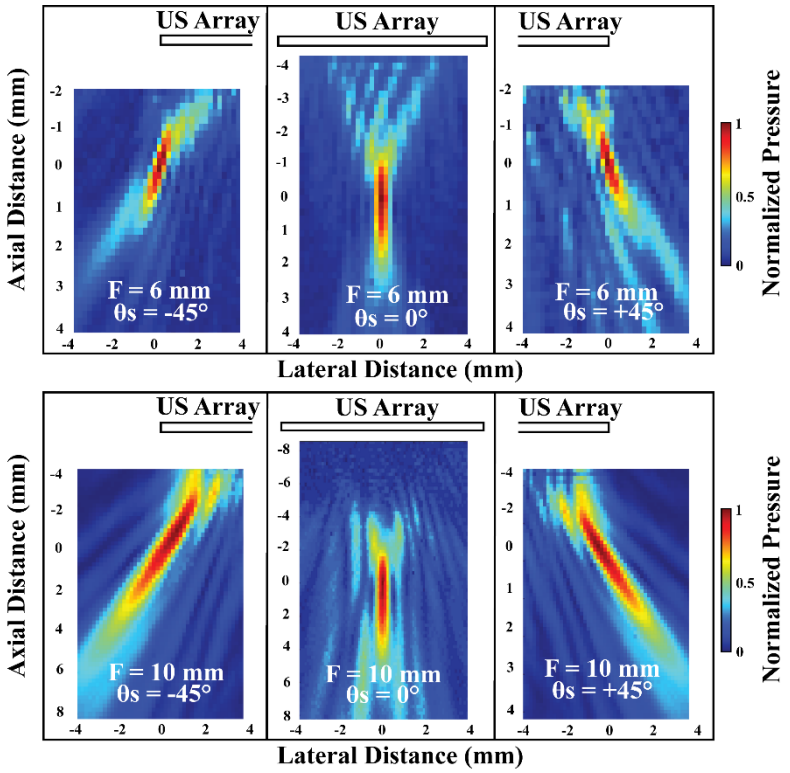
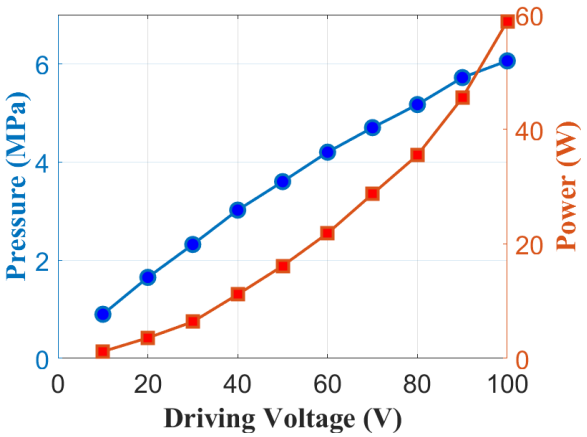


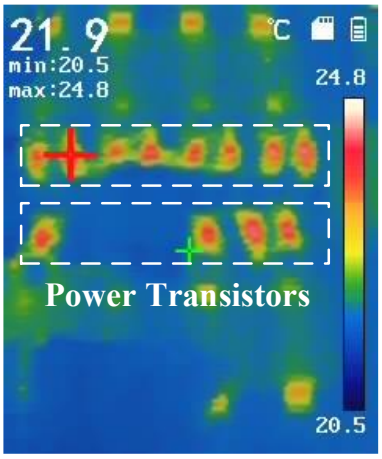
Figure 10. Measured US beam profiles of the 16-element phased array system for beam focusing and steering at focal depth of 6 mm (top) and 10 mm (bottom) with angles of -45º, 0º, and 45º.

The generated US beams by the phased array system were also characterized in measurements by scanning the hydrophone in the lateral-axial plane in front of the array, resulting in 2D beam profiles at different θ_s of –45º, 0º, and 45º at 6 mm and 10 mm focal depths. As shown in Figure 10, the array could successfully focus and steer US beams in different depth and angle scenarios controlled by the PC. The measured focal spot at F = 10 mm and θ_s = 0º exhibited a lateral resolution of 0.6 mm and an axial resolution of 4.67 mm with no significant sidelobes. At shorter F = 6 mm (θ_s = 0º), the lateral/axial resolution improved to 0.46/2.76 mm, which was expected.

Figure 11(a) shows the generated US pressure at F = 10 mm (θ_s = 0º) when the US transducer array was driven by 10-100 V pulses (V_{DDH} of 10-100 V). Other FUS parameters were set to TT = 18 s, ISI = 3 s, SD = 300 ms, PRF = 1 kHz, TBD = 0.5 ms, f_S = 2 MHz, T_d = 50 ns. The system achieved a maximum peak-peak pressure of 6 MPa, which is the utmost range for most FUS applications [2]. Figure 11(a) also shows the measured total power consumption of the HV driver with the same sonication parameters. As expected, power dissipation is nearly proportional to V_{DDH}^2, however, the US pressure output deviates from a linear relationship with V_{DDH} (especially at high voltages), indicating nonlinearity due to the gradual piezoelectrical material saturation. Figure 11(b) shows the maximum registered temperature of the electronics after the test duration of TT = 18 s (V_{DDH} = 100 V). The power transistors were identified as the hottest components on the board, with a temperature increase of only 4.3 ºC above the ambient room temperature of 20.5 °C.



(a)



(b)

Figure 11. (a) Measured US pressure output and HV driver power consumption at F = 10 mm (θ_S = 0º). (b) Thermal image of the HV driver at the end of TT = 18 s.

Table 2 summarizes the calculated power characteristics (power dissipation of different components for a given US output power) of a single HV driver channel at V_{DDH} = 80 V and compares it with the measurement result, showing good agreement particularly considering the difficulty in accurately modeling piezoelectric transducers.

Table 2. Calculated and Measured Power Characteristics of the High-Voltage Driver.

Switching Loss (W)	Cond. Loss (W)	Diodes Loss (W)	PZT Dynamic Loss (W)	US Output Power (W)	Calculated Total Power Cons. (W)	Measured Total Power Cons. (W)
0.18	0.1	0.84	0.31	0.86	2.31	2.0

At V_{DDH} = 80 V, f_S = 2 MHz, D = 40%, DC_{PRF} = 50%.

Table 3 benchmarks the reported phased array system in this manuscript against the prior work for FUS applications. The reported systems in [22–25] and [27] use ASIC and discrete technologies to drive a transducer array, respectively. The ASICs in [22] and [24] utilize bipolar-CMOS-DMOS (BCD) technology to achieve high driving voltage of 60 V, whereas [23] uses standard 5 V CMOS technology. Among the systems, our developed system stands out by achieving the highest acoustic pressure (6 MPa) and longest sonication duration (10 s) while maintaining a comparable lateral resolution (0.6 mm).

4. *In vivo* experimental results for BBB opening

To validate the proposed phased array system in an *in vivo* experiment, it was configured and utilized for BBB opening in mice. The BBB is a highly selective, semipermeable membrane composed of tightly packed endothelial cells, astrocyte end-feet, and pericytes, which form a protective barrier between the circulating blood and the brain parenchyma [33]. The BBB plays a critical role in maintaining the brain's microenvironment by regulating the exchange of molecules between the blood and the brain. However, the selective permeability of the BBB poses a significant challenge for brain drug delivery, as it restricts the entry of most pharmaceutical agents into the brain, thereby limiting the development of effective treatments

for neurological disorders [34]. To overcome the BBB, various strategies have been explored, with FUS combined with microbubbles emerging as a promising technique [35–36]. When FUS is applied in the presence of systemically administered microbubbles, the acoustic energy causes these gas-filled bubbles to oscillate and collapse, generating mechanical forces that induce complex cellular and molecular effects on the vascular endothelium and surrounding neurovascular unit [37–39]. These effects contribute to increased BBB permeability, allowing agents to cross into the brain at higher efficiencies [40–41].

Table 3. Benchmarking of the Developed Phased Array System for FUS Applications

Publication	TBioCAS21 [22]	TBioCAS21 [24]	TBioCAS21 [23]	TUFFC18 [27]	TBioCAS23 [25]	This Work
Electronics Tech.	0.18 µm HV BCD	0.18 µm HV BCD	0.18 µm	Discrete	0.18 µm HV BCD	Discrete
Transducer/ Integration	CMUT / Cable	CMUT / Flip-Chip	PZT / Flip-Chip	PZT / Cable	PZT / Flip-Chip	PZT / Cable
Frequency	5 MHz	2 MHz	8.4 MHz	5 MHz	12 MHz	2 MHz
# of Channels	16 (1D)	1024 (2D)	676 (2D)	128 (1D)	144 (2D)	16 (1D)
Beamformer	Delay Lock Loop (DLL)	Counter	DLL+ Phase Interp.	FPGA	Digital-to-Time Conv.	FPGA
Delay Resolution	12.5 ns	31.5 ns	1.6 ns	-	10.4 ns	5 ns
Peak-Peak Driving Voltage	60 V	60 V	5 V	96 V	20 V	100 V
Level Shifter	Pulse-Triggered Latch	AC-Coupled Capacitor	Cross-Coupled Latch	-	AC-Coupled Capacitor	AC-Coupled Capacitor
[+]Programming	Bluetooth MCU	Bluetooth MCU	FPGA	FPGA	FPGA	FPGA
Lateral Resolution	0.6 mm	0.4 mm	0.2 mm	0.8 mm	*0.173 mm	0.6 mm
US Pressure Output (pp) @ Depth	2.1 MPa @ 5 mm	1.15 MPa @ 5 mm	100 kPa @ 5 mm	~ 2 MPa @ 5 cm	N/A	~ 6 MPa @ 10 mm
Sonication Duration	< 1 ms	< 300 ms	< 1 ms	13 ms	2.5 µs	10 s

[+]MCU: Microcontroller [*]Simulation

While clinically used ultrasound technologies for BBB opening have advanced rapidly, preclinical ultrasound systems still predominantly rely on single-element transducers, which limits flexibility in selecting and targeting specific treatment locations and regions [3]. The phased array system in this work addresses these challenges in preclinical BBB opening systems for small animals. To demonstrate this applicability, we performed BBB opening in a rodent model, using Evans blue dye as a model agent to provide clear visual and quantitative indication of BBB opening. Beam steering was also tested *in vivo* by stimulating bilateral regions of the rodent brain. Post-sonication assessment of *ex vivo* brain tissues confirmed successful BBB opening in both the left and right brain hemispheres, demonstrating the system's precise and flexible steering ability.

4.1. Animal experimental procedure

Five adult female mice (C57/BL, 24 weeks old, Charles River Laboratories, Wilmington, MA, USA) were utilized for this study. A 3D-printed baseplate was designed to position the

transducer array on the mouse's head during the BBB opening procedure. Prior to the study, mice were anesthetized with light isoflurane and secured in a stereotactic frame for head stabilization. After the skin was removed from the top of the head, the baseplate was affixed to the exposed skull using dental cement, ensuring that the geometric center of the baseplate's opening window was aligned with the skull's bregma. Vetbond was applied to seal the skin edges around the skull, and the mice were allowed to recover overnight. Twenty-four hours after baseplate installment, the mice were again anesthetized with isoflurane (2%) and fixed in a stereotactic frame. Degassed ultrasound gel was applied both inside the baseplate and on the surface of the transducer array to ensure acoustic coupling. The transducer array was then carefully inserted into the baseplate to avoid introducing air bubbles into the ultrasound gel. A 3D-printed clasp was secured over the baseplate to secure the transducer array in place during the procedure. The phased array electronics and PC were configured as shown in Figure 1. FUS parameters were set to a peak-to-peak pressure of 0.6 MPa (measured in free-field water), *PRF* of 5 Hz, *TBD* of 6.6 ms and *SD* of 120 seconds. Time delay profiles were generated to target the left and right hemispheres of all 5 mice using coordinates of ±2 mm mediolaterally, 0 mm anteroposteriorly (relative to the bregma), and -3 mm dorsoventrally, to target either the left or right striatum. An additional -2 mm was applied to the dorsoventral coordinate to account for the baseplate and transducer housing thickness, resulting in a calculated beam steering angle of ±22°.

A catheter was prepared in the mouse tail vein by inserting a butterfly needle (SURFLO® Winged Infusion Set, 27G×½", Terumo Medical Corporation, Somerset, NJ, USA) with tubing and a 1 mL syringe filled with saline attached to the end of it. Once configuration was complete, a Hamilton syringe filled with Definity microbubbles (8×10^8 #/mL, 30 µL total volume) was used to inject microbubbles into the tail vein, immediately followed by FUS sonication using one of the generated time delay profiles. Ten minutes after the first sonication, microbubbles were re-injected, and FUS was applied using the opposite time delay profile. After the last sonication, Evans blue dye (4%, 60 µL total volume) was injected through the tail vein. Twenty minutes after the final FUS stimulation, mice were transcardially perfused with 1× phosphate-buffered saline (PBS) while under deep isoflurane anesthesia. Following perfusion, their brains were harvested and placed in 4% paraformaldehyde overnight for tissue fixation.

4.2. Tissue post processing

Fixed brain tissues were sectioned into 1-mm thick coronal slices using a mouse brain matrix (World Precision Instruments, Sarasota, FL, USA). Brightfield and fluorescence images of the brain slices were acquired using an Olympus MVX10 microscope equipped with an Olympus DP23 camera for brightfield (TBF) imaging and a Hamamatsu ORCA-Flash4.0 LT camera (C11440) for fluorescence (Cy5) imaging. All images were captured under 1x magnification and 0.63x zoom, with exposure settings kept consistent per image type.

For each mouse brain, three consecutive brain slices containing visually substantial Evans blue dye were selected to represent the FUS-targeted (FUS+) regions. Three additional

consecutive slices, located directly posterior to the FUS+ tissues, were denoted the non-targeted (FUS-) regions. Fluorescence images of the brain slices were analyzed using MATLAB. Background autofluorescence was determined as three times the standard deviation above the mean pixel intensity of one FUS- tissue per mouse brain. For all FUS+ and FUS- tissues, an ROI was manually drawn around the left and right hemispheres. The extent of BBB opening was measured by counting the number of pixels with intensities above the background autofluorescence. The pixel intensities above the background were then summed to represent the signal intensity of Evans blue delivery. Both the BBB opening volume and Evans blue intensity were normalized to the volumes of the FUS+ and FUS- regions to account for variations in region size.

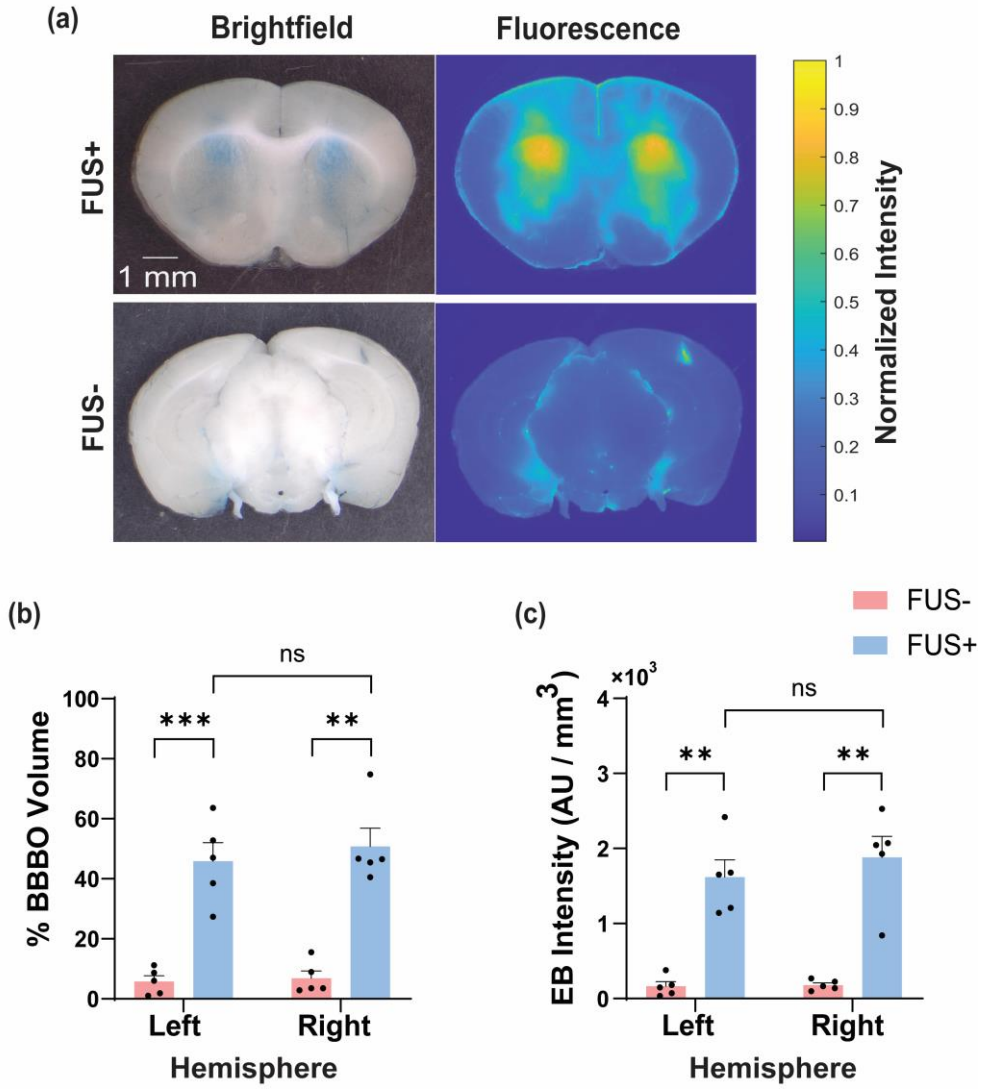


Figure 12. (a) Representative brightfield (left) and fluorescence (right) images of coronal brain slices from FUS-targeted (FUS+) and non-targeted (FUS-) regions. Quantification of BBB opening (BBBO) volume (b) and Evans blue (EB) intensity (c) in left and right hemispheres for FUS+ and FUS- regions.

4.3. In vivo results

The phased array system successfully induced BBB opening, with enhanced Evans blue accumulation observed predominantly in the left and right striatum of the mouse brains, as shown in Figure 12(a). Within these regions, the BBB opening volume averaged 46 ± 12% and 51 ± 12% of the regional volume in the left and right hemispheres, respectively, as shown in Figure 12(b). Additionally, Evans blue intensities were 9.9-fold higher in the left and 10.5-fold higher in the right hemispheres compared to non-targeted regions, as shown in Figure 12(c). Both the BBB opening volume and Evans blue intensity were significantly higher in FUS+ regions compared to FUS- regions for both hemispheres (**$p < 0.01$, ***$p < 0.001$). Notably, no statistically significant difference in BBB opening volume or Evans blue intensity was observed between the left and right hemispheres in the FUS-targeted regions, indicating that the extent of BBB opening and Evans blue extravasation were comparable following beam steering to both hemispheres using the phased array system. Data are expressed as a mean, with error bars indicating the standard error of mean (SEM). Statistical significance was determined using the paired two-tailed Student's t-test ($n = 5$).

5. Conclusion

A high-voltage, 16-channel phased array system for US interventions was developed, offering a high degree of flexibility in waveform generation and US pressure control. The system is capable of steering and focusing US beams with a fine delay resolution of 5 ns and delivering pulses up to 100 V. In experimental measurements, using a 2 MHz piezoelectric transducer array and 100 V pulses, the system generated a US beam with a peak pressure output of 6 MPa at various depths, without significant sidelobes. The system's functionality was thoroughly demonstrated across different steering angles and driving voltages, showcasing its versatility. Both the analytical and experimental evaluations of the HV driver's power consumption and heat dissipation were conducted. These assessments confirmed efficient operation, with manageable heat dissipation, ensuring reliable performance for extended sonication durations. Our *in vivo* study validated the use of the phased array system for precise and flexible BBB opening. These findings highlight the system's potential for applications involving ultrasound stimulation in multiple brain locations, including BBB opening for large-volume brain drug delivery, noninvasive neuromodulation of multiple brain regions, or management of widespread pathological processes, such as amyloid plaque reduction in Alzheimer's disease or diffuse tumor therapy in glioblastoma. The phased array system represents a robust solution for advanced US therapeutic applications, combining high acoustic pressure output, precise and dynamic beam focusing and steering, and flexible operation.

Acknowledgments

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Conflicts of interests

Authors do not have any conflict of interests.

Ethical statement

All animal procedures were reviewed and approved by the Institutional Animal Care and Use Committee at Washington University in St. Louis (Protocol No. 24-0222).

Authors' contribution

A. Javid, R. Biswas, S. Ilham, and M. Kiani conceptualized the modular 16-channel high-voltage ultrasound phased array system. R. Biswas and S. Ilham developed and optimized the FPGA codes and ultrasound transducers, with R. Biswas also leading their implementation and fabrication. A. Javid designed and developed the phased array electronics, and together with R. Biswas, integrated the system and conducted benchtop measurements to characterize its performance. C. Chukwu, Y. Yang, and H. Chen designed and performed the in vivo experiments. All authors contributed to discussions, as well as the preparation and revision of the manuscript. M. Kiani and H. Chen provided project administration and supervision. All authors have read and agreed to the published version of the manuscript.

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