Real-time 5.7 GHz Realization of Multidimensional 2D Hybrid Approximate DFT Spectrum Sensors for RF Situational Awareness

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2024 IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS) | 979-8-3503-8717-9/24/$31.00 ©2024 IEEE | DOI: 10.1109/MWSCAS60917.2024.10658684

***Abstract*—The measurement and perception of the RF spectrum is key for managing the electromagnetic environment of the future. Multichannel spectrum sensors that measure the RF environment can provide situational awareness across dimensions of space and time, leading to information on modulation, bandwidth, and frequency use across multiple directions of propagation. This paper builds upon recent progress on efficient 32-channel 5.7 GHz spectrum sensing by using a multiplierless approximate DFT operating in the spatial domain. In this work, 32 parallel temporal FFTs of size 1024 bins are realized as a parallel processing systolic array on a Xilinx reconfigurable open architecture computing hardware (ROACH-2) FPGA system to enable fine grained spectrum monitoring at about 100 kHz resolution across 32 simultaneous digital RF beams.**

I. Introduction

The electromagnetic radio frequency (RF) spectrum is getting increasingly crowded, especially in the sub-7 GHz bands, with new applications spreading to the FR3 band [1]. With ever increasing density and capacity in urban wireless networks, the legacy FR1 band (up to about 7 GHz) is highly sought after due to its favorable RF propagation characteristics in dense urban environments. Because of increasing demand, this FR1 band spectrum is now scarce and very expensive to license.

The ever-increasing value of FR1 band spectrum necessitates careful management of this resource to ensure investments made in networks and other infrastructure are well protected. Further, numerous defense and scientific use cases that share this band also need a degree of protection from harmful interference due to unintentional and/or malicious emissions (jamming). A key requirement for an improved physics-based spectrum compliance policy and its enforcement is low-complexity, low-power, and sensitive measurements of the RF environment. Such spectrum sensing operations are crucial for providing real-time spatiotemporal information of a given radio environment. RF situational awareness includes measurement of spectral occupancy, direction of propagation, modulation detection, and other parameters.

This work was supported in part by the National Science Foundation (NSF), NTIA (United States) and CNPq (Brazil).

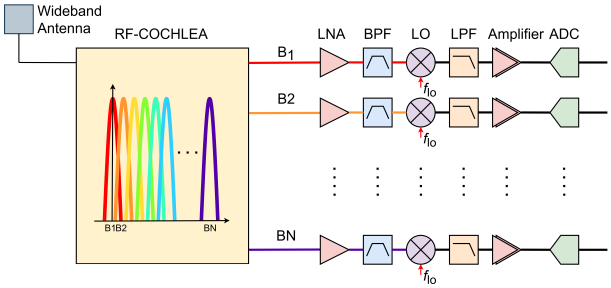

Fig. 1: Conceptual multichannel RF front-end with a channelizer and bandpass LNAs for each channel [2].

II. Design of Wideband RF Front-Ends for High-Resilience to Jamming

In relatively radio-quiet areas, such as a radio astronomy observatory site operating under ideal conditions, there are no strong sources of radio frequency interference (RFI). However, this is an idealized case that is not the reality as the bands get filled with more and more incumbents, some of whom might be non-compliant to FCC regulations, spectral masks set by wireless standards, and other guidelines from international authorities and regulatory bodies. In an ideal world, with low RFI power levels, spectrum sensing and monitoring can rely on a single wideband low-noise amplifier (LNA) and receiver chain that covers the entire FR1 band. However, reality is much more difficult to deal with. Strong RFI can be more than 100 dB above the signals of interest in some cases, for instance when a high power transmitter operates close to a sensitive receiver. In such scenarios, a single LNA design will be saturated by strong RFI, thus preventing reception of anything other than the strongest component, namely the RFI.

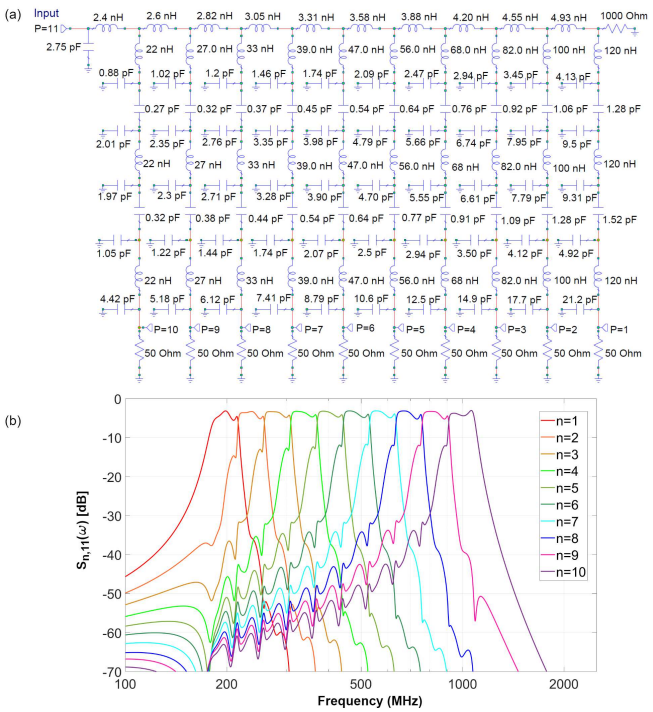

Fig. 2: (a) Circuit diagram of the 10-channel third-order cochlea channelizer [3] and (b) simulated transmission response $S_{n,11}(\omega)$ of each channel $n = 1, 2, \ldots, 10$ of the RF cochlea channelizer. Port 11 is the signal input.

A. Multichannel Front-End

To address this issue, we envision a multichannel RF front-end that uses a passive channelizer to divide the FR1 band into a series of sub-bands using a linear and time invariant (LTI) passive circuit [4]. Such a passive RF channelizer, which is fed by a wideband antenna, can be realized using several design approaches [2]. One hardware-efficient way to synthesize the channelizer is to use an RF cochlea filterbank [3]. Fig. 1 shows a conceptual design of the multichannel RF front-end with channelizer, followed by a bandpass LNA for each of its passbands. By using a separate dedicated LNA per passband, we avoid saturation of LNAs outside the band of the main RFI source. Further, although there will be a small hit in noise figure (NF) due to addition of the analog channelizer, the LNAs themselves are bandpass and can thus be designed to be lower noise than a single wideband LNA.

Fig. 2(a) shows a passive analog RF cochlea design following [5], [6]. This design has ten channels covering a total channelization bandwidth of 200 MHz to 1 GHz. It is designed as a third order channelizer, thus enhancing the stopband rejection and ensuring minimal signal distortion within the passband compared to a first-order design. The channelizer functions as a low-pass non-uniform transmission line with series resonator sections acting as shunt loads. The circuit uses a manifold of inductors to couple the ten channel filters, which are designed incorporating a tubular filter topology. This topology can be designed to offer a series resonator-like response over a wide frequency range, thus facilitating effective filtering [5]. The lowest-frequency channel is positioned at the end of the transmission line, while the highest-frequency channel is positioned at the input. This design employs a constant fractional bandwidth approach, but can be modified to function as a constant absolute bandwidth channelizer by integrating suitable constant bandwidth channel filters and a corresponding manifold. The channelizer was designed and simulated using Cadence AWR RF design Software. Fig. 2(b) shows the simulated transmission responses, $S_{n,11}(\omega)$, of each channel n, where ω represents the RF frequency. The design can be implemented at the board level using high-quality passive components. Alternatively, fully-integrated versions can be used at higher frequencies (up to 8 GHz) [7], [8].

B. RF Front-End and System Overview

In the present work, we limit ourselves to the 5.7–5.8 GHz sub-band since our existing work has been focused on this range. In the future, a wideband design having the capability to channelize the FR1 band will be created to address emerging RFI problems. For now, we adopt an available system having 4-element patch antenna subarrays, 32 subarrays, and 32 channels with dedicated receivers feeding a 32-channel analog-to-digital converter (ADC). Fig. 3 shows the overview of the system for our 32 antenna aperture. The receiver comprises of a LNA that delivers 16 dB gain at 5.8 GHz with a noise figure of 2.4 dB. The amplified signal is then band-pass filtered within 4.7–6 GHz range, effectively eliminating out-of-band noise and interference. The filtered signal is then down-converted using a local oscillator (LO) and low-pass filtered. The resulting intermediate frequency (IF) signal, which has a frequency up to 100 MHz, is further amplified by ≈30 dB [9]. The amplified I channel outputs are then coupled to the ROACH-2 field programmable gate array (FPGA)-based open digital signal processing (DSP) system designed by the Collaboration for Astronomy Signal Processing and Electronics Research (CASPER) collaboration [10]. The ROACH-2 is a standardized platform designed for use by the international radio astronomy instrumentation community with particular focus on the DSP needs of the Square Kilometer Array (SKA) radio telescope. It consists of a Xilinx Virtex-6 sx475t FPGA chip for processing, two ADC cards (each supporting 16 channels), and four parallel 10 Gbps Ethernet ports.

C. Review of DFT Approximation

The discrete Fourier transform (DFT) maps an N-point input signal $\mathbf{x} \triangleq \begin{bmatrix} x[0] & x[1] & \cdots & x[N-1] \end{bmatrix}^\top$ into an output signal $\mathbf{X} \triangleq \begin{bmatrix} X[0] & X[1] & \cdots & X[N-1] \end{bmatrix}^\top$ according to the following relationship: $\mathbf{X} = \mathbf{F}_N \cdot \mathbf{x}$, where $\mathbf{F}_N$ is the DFT matrix of order N whose entries are $f_{k,n} = \exp\left(-\frac{2\pi j}{N} nk\right)$, $k, n = \{0, 1, \ldots, N-1\}$. Computed by definition, the DFT complexity is in $\mathrm{O}(N^2)$, which is a prohibitively high complexity for real-time operations. In practice, the DFT is computed by means of one of many available algorithms,

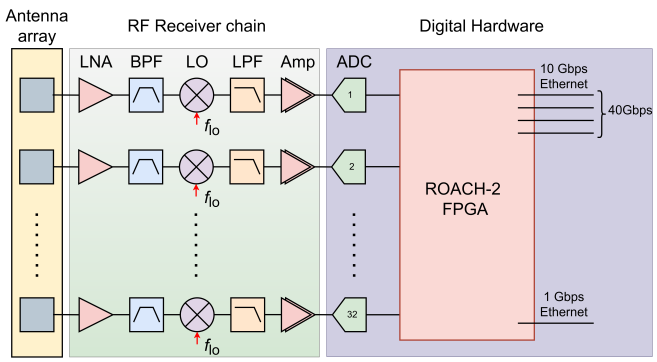

Fig. 3: The overall system architecture, showing 32 parallel channels with direct-conversion receivers.

collectively referred to as fast Fourier transforms (FFTs), which reduce the computational cost to $\mathrm{O}(N \log N)$ [11]. In contexts where the FFT complexity still represents a computational bottleneck, matrix approximations appear as a practical alternative [12]. DFT approximation theory essentially consists of deriving a matrix $\hat{\mathbf{F}}_N$ such that: (i) $\hat{\mathbf{F}}_N$ is close in some sense to the exact DFT matrix; (ii) $\hat{\mathbf{F}}_N$ preserves the sought-after properties of the exact DFT; and (iii) and $\hat{\mathbf{F}}_N$ has a significantly lower computational complexity compared to the exact transformation. The proximity measure is often the Euclidean distance, which tends to preserve the physical interpretation of the transform domain spectrum [13].

Because multiplication operations are computationally more complex when compared to an addition, DFT approximations should be multiplierless. To ensure a low computation cost, DFT approximation matrices are thus designed to possess low-complexity entries that eliminate multiplications. In particular, the DFT approximations introduced in [14] form a special class of low-complexity matrices defined over the set $\{0, \pm 1, \pm j\}$. Such entries allow for multiplierless transform operations, i.e., the evaluation of an approximate DFT (ADFT) requires only addition operations [13].

In this work, we adopt the 32-point ADFT, $\hat{\mathbf{F}}_{32}$, defined in [14] and elaborated in [9], [15]. The approximation $\hat{\mathbf{F}}_{32}$ can be factorized into eight low-complexity, sparse matrices:

$$\hat{\mathbf{F}}_{32} = \mathbf{W}_8 \cdot \mathbf{W}_7 \cdot \mathbf{W}_6 \cdot \mathbf{W}_5 \cdot \mathbf{W}_4 \cdot \mathbf{W}_3 \cdot \mathbf{W}_2 \cdot \mathbf{W}_1, \quad (1)$$

where the matrices $\mathbf{W}_i$, $i = 1, 2, \ldots, 8$, correspond to low-complexity computing stages that require only trivial multiplicands—$\{0, \pm 1, \pm j\}$—which lead to a multiplication-free FPGA hardware design. The precise numerical definition for each matrix $\mathbf{W}_i$, $i = 1, 2, \ldots, 8$, can be found in [9].

Fig. 5(a) shows the magnitude frequency response of the 32-point DFT alongside the frequency response of the considered 32-point ADFT (see Fig. 5(b)). It can be observed that the ADFT provides a worst-case sidelobe level about $1.5\,\mathrm{dB}$ higher than the DFT, which is acceptable for many applications in RF sensing [9], [15]. The benefit is significantly lower computational complexity and power consumption.

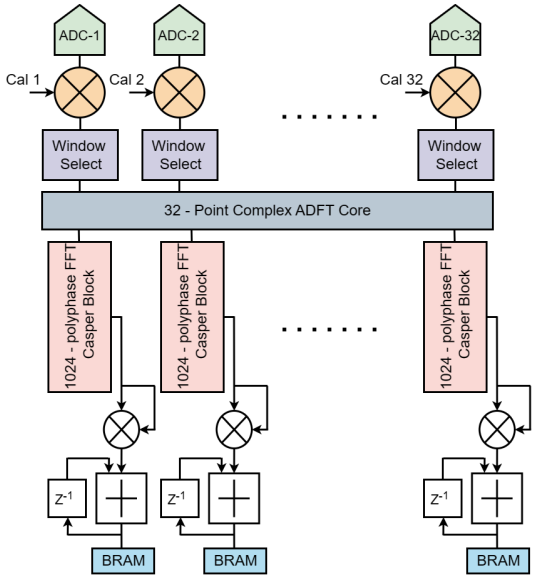

Fig. 4: Block diagram of the overall ADFT and FFT calibration system, including energy integration and BRAM registers.

III. Digital Architecture

The ROACH-2 signal processor contains multiple systolic array processors that are custom-designed for spectrum sensing over multiple simultaneous directions. The first step in sensing is calibration of the internal non-linearities of the ADCs. This is achieved by following the calibration scripts published by the CASPER community [16]. The 32 parallel RF receivers are then calibrated for gain using a custom-designed calibration circuit, as discussed below.

A. RF Receiver Gain Calibration

Fig. 4 shows the design of the receiver gain calibration system. The raw sample values, with calibration coefficients set to unity, are captured from the (calibrated) ADCs. These quantities are squared and integrated to yield energy values which are accumulated for 1024 samples. Then, these energy values are passed to a block RAM (BRAM) on the FPGA which can be mapped into an internal ARM core running Linux. The BRAMs are then read from the host computer using a Python script. The measured energy values are used to calculate the gain calibration coefficients for each channel, which are then programmed for real-time operation. An extension to temporal calibration is currently in progress.

B. ADFT Core

We formed 32 parallel simultaneous RF beams using the ADFT discussed in the previous section. For this purpose, each low-complexity, sparse matrix $\mathbf{W}_i$, $i = 1, 2, \ldots, 8$, was mapped into digital hardware. The ADFT matrix factorization was realized using Xilinx System Generator and the algorithm was functionally verified through MATLAB Simulink. The validated design was implemented on ROACH-2 FPGA using two libraries from the CASPER community [10]. The

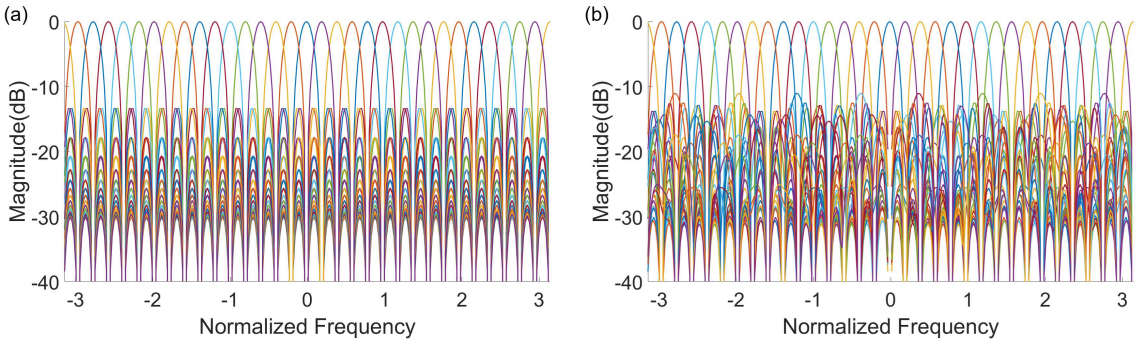

Fig. 5: (a) Magnitude responses of (a) the 32-point DFT (b) the 32-point ADFT [9].

resulting spatial ADFT core takes in 32 inputs from the array receivers and generates 32 output bins that correspond to RF beams. Specifically, each ADFT output bin corresponds to an RF far-field beam directed at a discrete direction given by $\theta_k = \arcsin(k/32)$, $k = -16, -15, \ldots, 14, 15$.

C. FPGA-based Spatiotemporal 2D FFT Architecture

The RF beams were further channelized in the temporal frequency domain using the 1024-point polyphase FFT core from the CASPER digital library [17]. Calculation of these temporal FFTs necessitated 32 parallel temporal FFT cores. The FPGA clock was set to $200\,\mathrm{MHz}$, resulting in a Nyquist bandwidth of $100\,\mathrm{MHz}$ and a frequency resolution for each beam of $\Delta F = 100/1024\,\mathrm{MHz}$.

D. Digital Programmable Spatial Windows

The application of spatial windowing allows control of the sidelobe level, albeit at the cost of widening the beams. The proposed architecture allows several spatial windows to be selected by a control signal accessible through software. The outputs of the 32 ADC channels are applied to a windowing unit that has four possible windows selected via a multiplexer. Three of these options are Butterworth, Hamming, and Hanning windows, while the fourth is a "no windowing" option with unity coefficients. Depending on the spatial windowing requirements, a user can select any of these options.

E. Spectral Energy Readout

The beam-wise temporal FFT outputs result in 1024 complex values corresponding to 1024 discrete frequency bins. The power spectral density (PSD) is estimated by squaring the magnitude of each frequency bin. The estimate is obtained by time-averaging across 1024 temporal FFT evaluations, thus leading to a new PSD measurement every 1 million clock cycles. The PSD update rate is $\approx 200\,\mathrm{update/s}$ for a $200\,\mathrm{MHz}$ clock. A BRAM vector accumulator block is used to accumulate PSD values and pass them to the software process supported by the CASPER design flow. Specifically, the `casperfpga` Python library is used to interact with CASPER hardware to extract values from the shared BRAM. This library can be used to re-configure the firmware and also read/write registers over various communication interfaces.

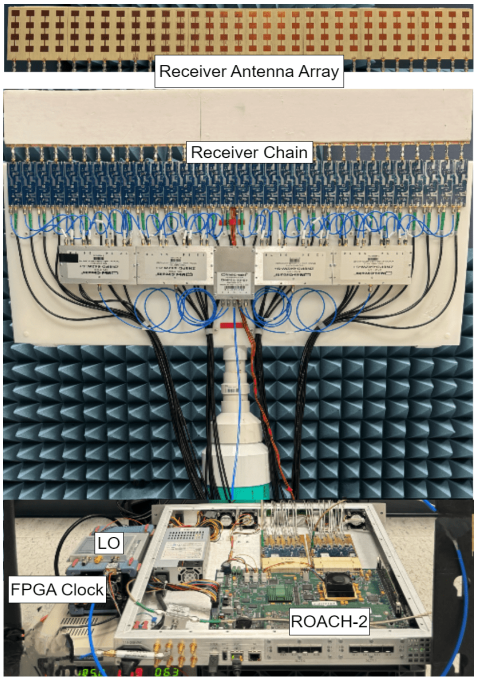

Fig. 6: The experimental setup. The spectrum sensor consists of 32 4-element sub-arrays operating in the 5.7–$5.8\,\mathrm{GHz}$ band. All real-time DSP occurs on a ROACH-2 FPGA system (Xilinx Virtex-6 sx475T FPGA).

IV. Testbed Realization

The spectrum sensor produces fine-grained energy detection ($100\,\mathrm{kHz}$ resolution) across 32 simultaneous directions. Fig. 6 shows the experimental setup in the laboratory. The system supports collection of raw data from the calibrated ADCs for various RF machine learning (ML) applications that require massive amounts of training data. Ongoing work includes multidirectional spectrum sensing, collection of training data for deep learning for RF processing applications, and the embedding of dynamic spectrum sharing (DSA) concepts to the spectrum awareness system at the hardware level using real-time massively-parallel FPGA based DSP.

In the experimental setup, a double ridge guide horn an-

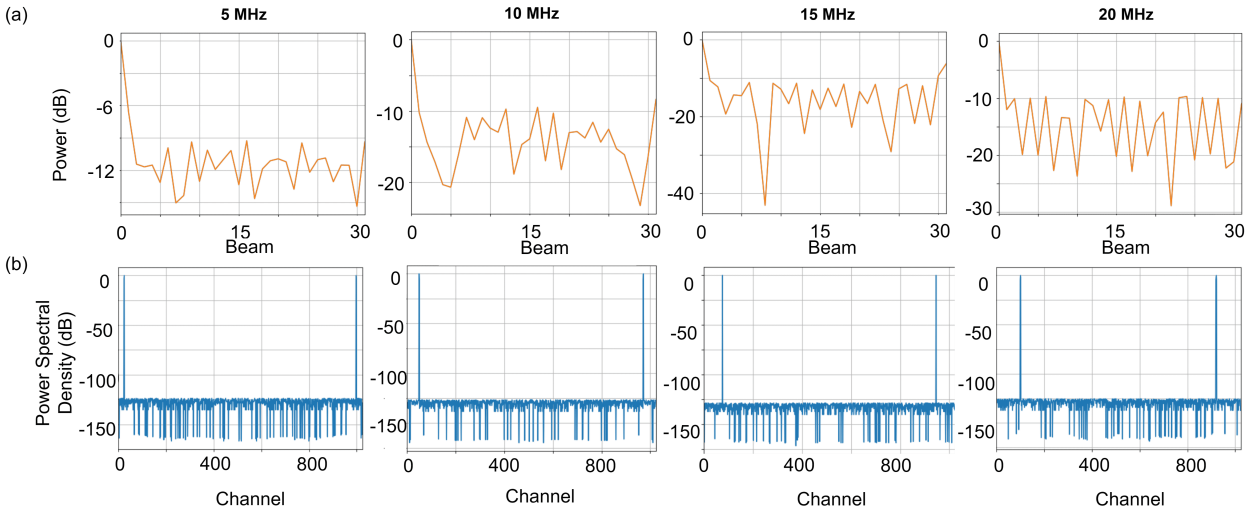

Fig. 7: Real-time measurements: (a) Normalized power over the 32 RF beams for basebands of 5 MHz, 10 MHz, 15 MHz, and 20 MHz, with the signal source placed at broadside 0° in all cases. The results demonstrate >10 dB of directivity. (b) Temporal PSD over the 1024 discrete frequency bins for the particular RF beams at 5 MHz, 10 MHz, 15 MHz, and 20 MHz.

tenna (A.H Systems SAS-571) was used to transmit a tone of 5.71 GHz. Measurements were taken by setting the LO to 5.70 GHz, resulting in an IF of 10 MHz. The down-converted outputs were sampled by the ADC at 200 Ms/s to generate the digitized signal. A VALON 5015 frequency synthesizer (10 MHz to 15 GHz) was employed to generate the LO signal and a NOISE XT low-jitter clock synthesizer (2 MHz–7 GHz) was used to generate the FPGA and 32-channel ADC clock. The measurements were taken with a transmitter-receiver separation of more than 10 m. Fig. 7(a) depicts the measured distribution of normalized power over the spatial axis (32 beams) for the 5 MHz, 10 MHz, 15 MHz and 20 MHz baseband signals when the signal source is positioned on broadside (i.e., a receive angle of 0°). Fig. 7(b) depicts the measured temporal PSD for each baseband frequency.

V. Conclusion

The enhancement of our existing 32-channel 5.7 GHz spectrum sensing system by implementing 32 parallel 1024-bin temporal FFTs on a ROACH-2 hardware platform was discussed. This work experimentally verifies that the proposed architecture is capable of sensing information from multiple directions with a frequency resolution of 100 kHz.

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