An SNR-Enhanced 8-Ary (SNRE-8) Modulation Technique for Wireline Transceivers Using Pulse Width, Position, and Amplitude Modulation

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***Abstract*— This article presents a novel eight-ary modulation technique with improved signal-to-noise ratio (SNR) compared to conventional pulse amplitude modulation 8 (PAM-8). The proposed SNR-enhanced 8-ary (SNRE-8) scheme modulates pulse width, position, and amplitude to improve the SNR. The proposed SNRE-8 modulation leverages the wireline channel loss to perform the modulation. Digital decoding of mutually exclusive eyes generated by the proposed SNRE-8 modulation further improves the eye margin at the receiver. A 27-Gb/s transceiver is implemented in a 65-nm CMOS process employing the proposed modulation. A PAM-8 transmitter is implemented on the same chip for comparison purposes. Compared to the PAM-8 modulation, the proposed SNRE-8 modulation shows an average SNR improvement of 10.6 dB at the near-end eye at the cost of 6.6% eye width reduction. With the aid of a time-domain feed-forward equalizer (FFE) and a continuous-time linear equalizer (CTLE), the proposed SNRE-8 transceiver achieves a bit error rate (BER) of 10^{-8} on a 9-dB loss channel with an energy efficiency of 5.39 pJ/bit.**

***Index Terms*— I/O, pulse amplitude modulation 8 (PAM-8), SNR-enhanced 8-ary (SNRE-8), transceiver, wireline.**

I. Introduction

THE emergence of artificial intelligence (AI)-based applications is increasing the data traffic in data centers. Data rates higher than 112 Gb/s are needed to meet the ever-increasing data traffic demand [1], [2], [3], [4], [5], [6]. Data rates can be increased by either increasing the baud rate, or increasing the order of modulation [7]. Fig. 1 shows published work for wireline transceivers in the last ten years [8]. We can observe that for data rates below 56 Gb/s, the wireline transceivers are mostly using non-return-to-zero (NRZ) signaling [9], [10], [11], [12], [13], [14], [15], [16], [17].

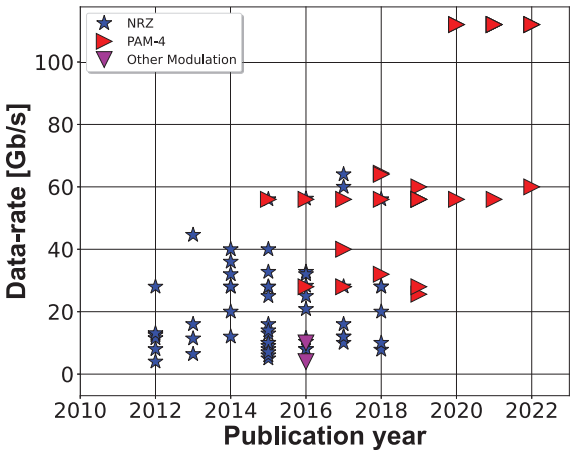

Fig. 1. Published transceivers in the last ten years at different data rates and modulation orders [8].

For data rates of 56 Gb/s and beyond, the pulse amplitude modulation 4 (PAM-4) modulation is more commonly used [1], [2], [3], [4], [5], [6], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. To improve the efficiency, researchers have also published transceivers with other modulation schemes such as quadrature shift keying (QPSK) and quadrature amplitude modulation (QAM) [29], [30]; however, the data rates of the proposed modulation schemes are relatively low with 10 Gb/s in [30] and 4 Gb/s in [29].

Higher order modulation techniques such as PAM-4 and PAM-8 help to reduce the required clock frequency for the transceiver system, and therefore, they relax the power and complexity of clock generation and distribution. For example, if a transceiver is required to transmit 27 Gb/s based on quarter-rate system, then for an NRZ signal, a clock of 6.75 GHz is needed to be generated (with four phases) and distributed on chip. If a PAM-4 signal is used instead, a clock frequency of 3.375 GHz is required. Similarly, if a PAM-8 signal is used, the clock frequency becomes 2.25 GHz. The reduction of the clock frequency reduces the power dissipation of the system and relaxes the jitter and phase mismatch requirements of the system.

The loss profile of a channel consisting of a combination of FR-4 trace and coaxial cables is shown in Fig. 2(a). Three different types of modulations (NRZ, PAM-4, and PAM-8) are considered to transmit a 27-Gb/s signal over this channel.

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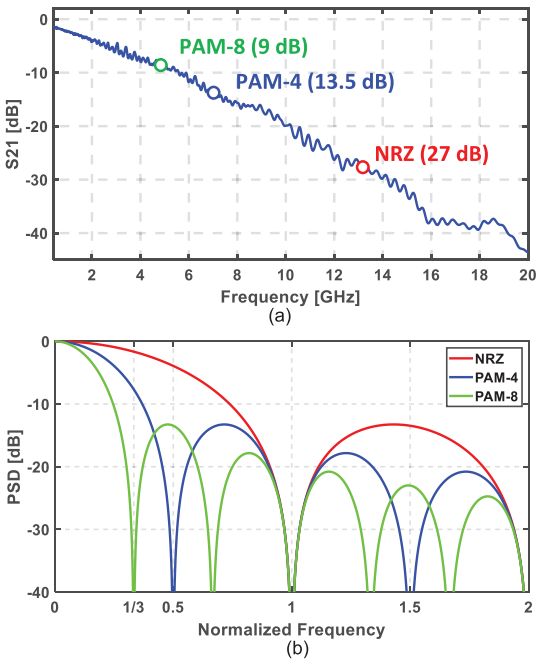


Fig. 2. (a) Measured channel loss profile. (b) PSD at different orders of modulation.

Fig. 2(b) shows the power spectral density (PSD) of different modulation orders. In the case of NRZ, the Nyquist frequency for 27 Gb/s is 13.5 GHz, as shown in Fig. 2(a), and the channel loss at the Nyquist frequency is 27 dB. For PAM-4, the Nyquist frequency is 6.75 GHz, and the loss is 13.5 dB. Finally, for PAM-8, the Nyquist frequency is 4.5 GHz, and the loss is 9 dB. While the channel loss at Nyquist frequency is lower for higher order modulation, this improvement in channel loss does not result in intersymbol interference (ISI) reduction (bigger eye opening) because higher order modulations suffer from higher ISI sensitivity.

Implementing a PAM-8 system faces multiple challenges: signal-to-noise ratio (SNR) reduction, ISI sensitivity, and linearity. A PAM-8 transceiver was demonstrated in [31] and [32], where the problem of receiver front-end linearity is addressed by using a time-domain feed-forward equalizer (FFE).

SNR can be improved by introducing forward error correction (FEC) algorithms such as Turbo codes, low-density parity check decoders (LDPC), and Reed–Solomon coding [33]. FEC can improve the effective SNR of the system by correcting the errors in the received data, and therefore, reduce the bit error rate (BER) [33], [34]. Error correction can be done by mapping n-bit symbols to m-bit symbols where m is larger than n. Errors in the m-bit symbol can be corrected with an upper limit on the number of errors in each m-bit symbol [34]. This sets a lower bound on the pre-FEC BER. Higher pre-FEC BER results in more complex FEC and larger coding overhead. Additionally, larger coding overhead is accompanied by large latency [35] in the wireline link, which is not acceptable in many applications. Therefore, it is essential to improve the pre-FEC BER and the actual SNR of the signal. Other works [36], [37] have demonstrated SNR improvement on PAM-4 by employing sequence encoding on the least

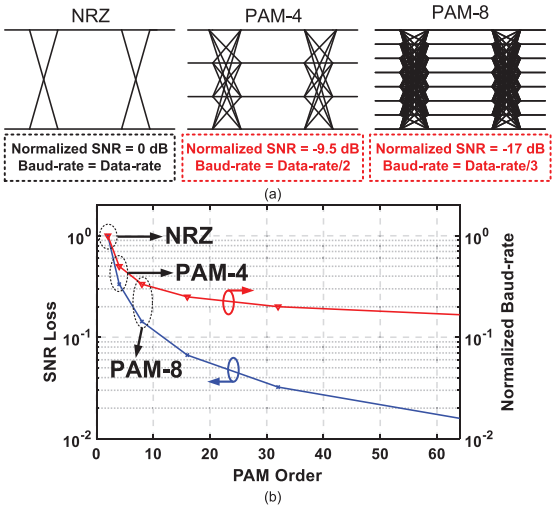


Fig. 3. (a) SNR and baud rate for NRZ, PAM-4, and PAM-8 modulation. (b) SNR degradation and normalized baud rate versus order of modulation.

significant bit (LSB) of a PAM-4 signal. The work proposed in [36] and [37] shows around 5.26-dB SNR improvement with a 12.5% overhead in data rate.

In this work, we present a new eight-ary modulation technique using the pulse width, amplitude, and position to improve the SNR by 10.6 dB compared to conventional PAM-8 [38]. The proposed system employs time-domain FFE as well as a continuous-time linear equalizers (CTLE) to compensate for a channel loss of 9 dB. This article is organized as follows. Section II presents the challenges of using PAM-8 in wireline transceivers. In Section III, we propose the new modulation technique. In Section IV, we present the implementation details of the transceiver system. In Section V, we present the measurement results. Section VI presents a brief discussion of the future directions for the proposed modulation. Finally, the conclusion is presented in Section VII.

II. Challenges of Using PAM-8 in Wireline Transceivers

A. SNR Degradation Versus Baud-Rate Reduction

While PAM-8 helps to reduce the baud rate, the price for this reduction is lower SNR. Fig. 3(a) shows the effect of using higher order modulation on the SNR and baud rate. We consider that NRZ has a normalized SNR of 0 dB. PAM-4 reduces the eye height by 3×, which corresponds to a loss of 9.5 dB in SNR. The baud rate in the case of PAM-4 is 2× smaller than the baud rate of NRZ. If PAM-8 is used instead, then the eye height is reduced by 7× compared to NRZ signaling, which corresponds to a loss of 17 dB in the SNR. The baud rate in the case of PAM-8 is 3× smaller than that of NRZ signaling. It is noted that the SNR reduction when PAM-4 is replaced by PAM-8 is large (from 3× to 7×), whereas the baud-rate reduction is incremental (from 2× to 3×). This shows that there is a diminishing return in baud-rate reduction when the order of modulation is increased.

Fig. 3(b) shows a graphical representation of the effect of increasing the modulation order on the SNR and normalized baud rate (baud rate/data rate), which confirms the diminishing

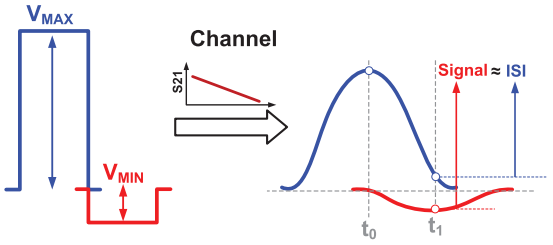


Fig. 4. Effect of higher order modulation on ISI sensitivity.

return of the conventional path of increasing the order of modulation through PAM. For example, moving from NRZ to PAM-64, the eye height is reduced 63× (36 dB) whereas the baud rate reduces by only 6×. This severe degradation in SNR for 6× reduction in baud rate suggests that the path to higher order modulation cannot be achieved without solving the SNR degradation problem.

B. ISI Sensitivity

In addition to the SNR degradation of the PAM-8 signal, the eye margin of the PAM-8 signal is further degraded due to the higher sensitivity to residual ISI [37]. Fig. 4 shows a modulation where the maximum voltage level of a pulse is V_{MAX} and the minimum voltage level of a pulse is V_{MIN}. If a maximum level pulse (V_{MAX}) is transmitted through a lossy channel followed by a minimum level pulse (V_{MIN}), the ISI due to the first pulse (V_{MAX}) becomes comparable to the amplitude of the minimum pulse. As the ratio between the maximum swing to the minimum swing increases ($V_{\mathrm{MAX}}/V_{\mathrm{MIN}}$) in higher order PAM, the effect of ISI on the eye margin becomes larger.

If we consider a channel response where the pulse response has a main tap h_0, and post-cursor and pre-cursor taps h_i (where i is the index of the tap), then the estimated eye height in the absence of noise is expressed as

$$V_{\mathrm{eye}} = h_0 \times V_{\mathrm{MIN}} - \sum_{i\neq 0} |h_i| \times V_{\mathrm{MAX}} \tag{1}$$

where V_{eye} represents the eye height. If the noise is ignored for simplicity, then the condition for successful communication in the presence of ISI is that V_{eye} is larger than zero. Therefore, the condition for successful communication for a given modulation can be expressed as

$$\frac{h_0}{\sum_{i\neq 0}|h_i|} > \frac{V_{\mathrm{MAX}}}{V_{\mathrm{MIN}}}. \tag{2}$$

Equation (2) shows that a higher $V_{\mathrm{MAX}}/V_{\mathrm{MIN}}$ ratio requires less ISI for error-free communication. Therefore, we can use the ratio $V_{\mathrm{MAX}}/V_{\mathrm{MIN}}$ to quantify how sensitive the signal is to ISI. This ratio can be calculated for any PAM-N system as

$$\frac{V_{\mathrm{MAX}}}{V_{\mathrm{MIN}}} = 2^n - 1 \tag{3}$$

where n is the number of bits encoded into one symbol. Equation (3) shows that the ISI sensitivity increases exponentially as n increases, which makes equalizing higher order modulation very challenging. For example, the ratio of $V_{\mathrm{MAX}}/V_{\mathrm{MIN}}$ is 1 for NRZ, 3 for PAM-4, and 7 for PAM-8.

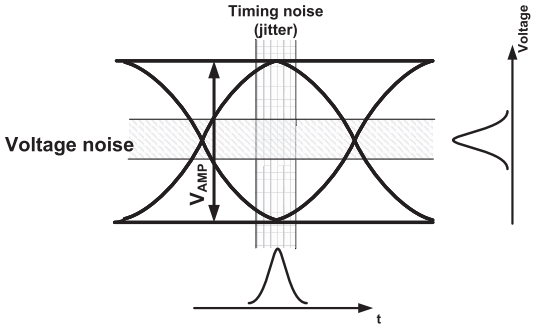


Fig. 5. Sources of noise in sampling the data from a generic eye diagram.

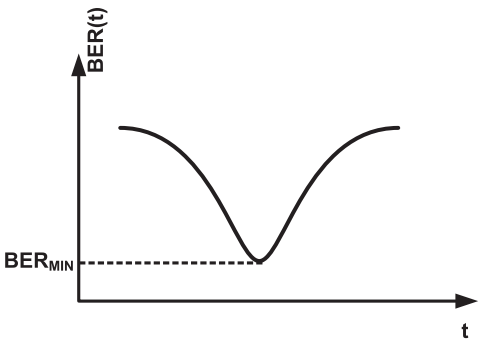


Fig. 6. BER as a function of sampling time.

It should be noted that although the ratio of $V_{\mathrm{MAX}}/V_{\mathrm{MIN}}$ increases for higher order modulation, the summation of $|h_i|$ terms decreases due to Nyquist loss reduction. However, the decrease in the $|h_i|$ terms does not scale as much as $V_{\mathrm{MAX}}/V_{\mathrm{MIN}}$, therefore, ISI sensitivity becomes worse.

C. SNR Effect on Jitter Requirements

The presence of jitter on the sampling clock increases the BER. There are two sources of noise during sampling, voltage noise, and timing noise (jitter) as shown in Fig. 5. In the absence of jitter, the BER can be calculated as [39]

$$\mathrm{BER}|_{t_s} = \frac{1}{2}\mathrm{erfc}\left(\frac{\mathrm{SNR}}{2\sqrt{2}}\right) \tag{4}$$

where SNR is given by $V_{\mathrm{AMP}}/\sigma_n$, σ_n is the standard deviation of voltage noise, and V_{AMP} is the differential height of the eye shown in Fig. 5. In (4), additive white Gaussian noise is assumed. Because the SNR is not constant at different sampling instances of the eye, we can plot the BER as a function of time BER(t), as shown in Fig. 6. The overall BER at a given sampling instant t_s can be calculated as

$$\mathrm{BER} = \int_0^{\mathrm{UI}} \mathrm{BER}(t)n(t)dt \tag{5}$$

where $n(t)$ is the probability density function of the sampling time with a mean value that corresponds to the sampling instant t_s. It can be seen from (5) that the average BER of a system is affected by the BER(t) plot and $n(t)$. From (4), BER(t) is a function of SNR. Therefore, if the SNR of the received signal is increased, the jitter requirement of the system can be relaxed even if the horizontal width of the eye

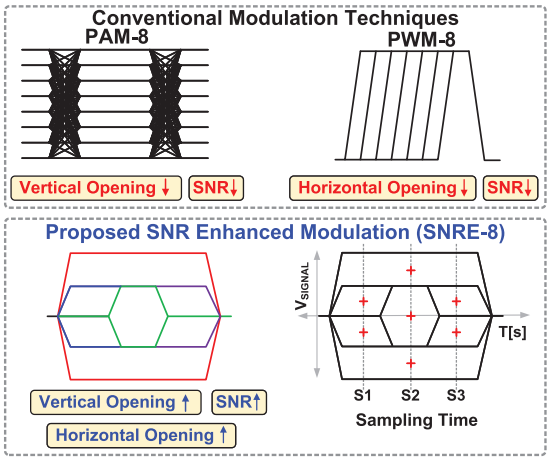


Fig. 7. Comparison between PAM-8, PWM-8, and the proposed SNRE-8 modulation.

is slightly reduced. Consequently, the eye width of a given signal could be traded off for higher SNR with minimal effect on the jitter requirement of the system.

III. Proposed SNR Enhanced Modulation

Based on the analysis in Section II, we can determine that decreasing the ratio V_{MAX}/V_{MIN} is important to increase the SNR and reduce the ISI sensitivity. The problem with the conventional PAM-N modulation is that it encodes the digital information by modulating only one dimension, which is the amplitude of the signal (voltage domain). This leads to larger ratios of V_{MAX}/V_{MIN} with larger orders of modulation. To alleviate this problem, the time domain can be used as another dimension to modulate the signal. For example, pulse-width modulation (PWM) can be used to boost the vertical SNR [40]. However, PWM comes at the price of a degraded horizontal sampling margin at the receiver. Alternatively, if both dimensions are used, time and voltage, a signal can be generated with better SNR than PAM-N while achieving better timing margins than PWM-N [38].

A. Pulse Width, Amplitude, and Position Modulation

The proposed SNRE modulation is performed by modulating pulse amplitude, width, and position. Fig. 7 shows eye diagrams of the proposed eight-ary SNR-enhanced 8-ary (SNRE-8) modulation compared to the conventional PAM-8 and PWM-8 modulations. In the proposed SNRE-8 scheme, the minimum eye height is $V_{MAX}/4$, which is slightly lower than PAM-4 ($V_{MAX}/3$). Therefore, the proposed SNRE-8 modulation theoretically achieves 4.86-dB SNR improvement on a flat (no-loss) channel. Additionally, the ratio of V_{MAX}/V_{MIN} is now reduced to 4 (instead of 7), so this reduces the ISI sensitivity by 4.86 dB. Moreover, the SNRE-8 signal resets to the common mode (zero) after each pulse. This reset adds guard time between different pulses, and therefore, reduces ISI even more. By combining all those factors in addition to another decoding feature (explained in Section III-C), the proposed SNRE-8 modulation shows 10.6-dB improvement in vertical eye-opening (measured) compared to PAM-8 signaling. Based on Fig. 7, the ideal SNRE-8 eye width is around

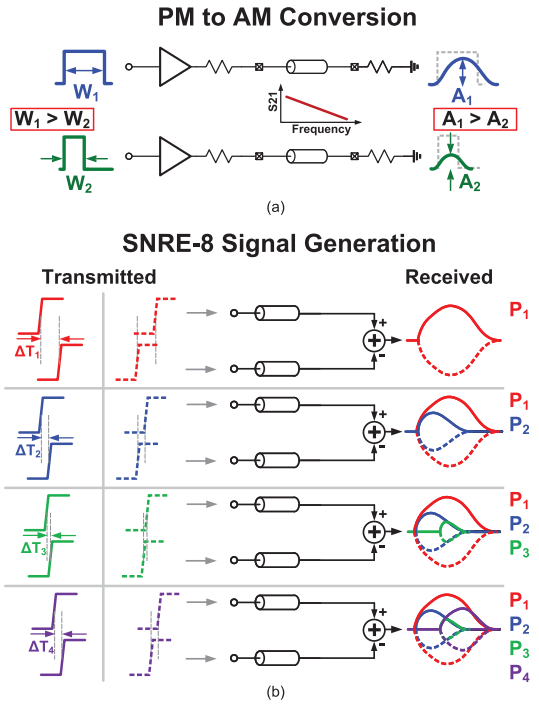


Fig. 8. (a) Phase difference modulation to AM conversion through the channel. (b) SNRE-8 signal generation.

33% of that of an ideal PAM-8 modulation. However, due to the reduced ISI sensitivity, the measured horizontal eye reduction of the SNRE-8 signal on a lossy channel is only 6.6% smaller than that of a PAM-8 signal. Based on the analysis in Section II-C, the proposed SNRE-8 modulation is trading off 6.6% of the eye width for an SNR improvement of around 3× (measured). Consequently, the effect of eye width reduction on the jitter requirement of the system is minimal when compared to conventional PAM-8. Compared to PWM-8, the proposed SNRE-8 modulation has a horizontal sampling margin that is 2.33× that of PWM-8 at the price of having a minimum pulse amplitude that is 0.25× PWM-8. Therefore, the proposed SNRE-8 modulation trades off degraded vertical margins of PAM-8 with horizontal timing margins, and it trades off degraded horizontal timing margins of PWM-8 with vertical margins to improve the overall SNR of the system. Unlike PAM-8, the proposed SNRE-8 modulated signal requires multiple sampling phases and thresholds within the same eye for proper decoding, which adds complexity and power to the receiver.

B. SNRE-8 Signal Generation

To generate the proposed SNRE-8 modulated signal with good energy efficiency, the ISI from the channel is leveraged to perform amplitude modulation (AM). If a signal with a pulse width W_1 passes through a lossy channel, as shown in Fig. 8(a), this signal will suffer from attenuation and dispersion, which results in a signal with amplitude A_1 at the far end of the channel. If another signal with pulse width W_2 is sent through the same channel where $W_1 > W_2$, the signal generated at the far end of the channel (with amplitude A_2) will suffer from more attenuation where $A_1 > A_2$. We leveraged

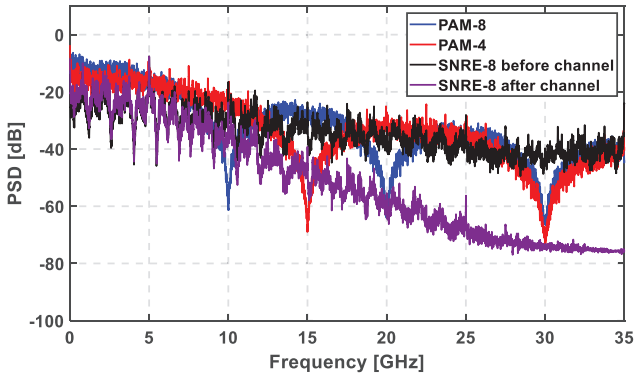


Fig. 9. PSD of PAM-4, PAM8, and the proposed SNRE-8 signals.

this property of the channel to perform AM to achieve good energy efficiency in the transmitter. The SNRE-8 modulated signal is generated by modulating the rising and falling edge delay between two clock signals, as shown in Fig. 8(b). If the delay between the two clock signals is ΔT_1, then the pulse P_1 is differentially received as shown in Fig. 8(b). If the delay between the two clock signals is changed to ΔT_2, then P_2 is generated at the receiver. It should be noted that the starting points of P_1 and P_2 are the same, i.e., same pulse position and different pulse width. By changing the pulse position, more pulses can be generated. For example, using a different pulse position and pulse width (edge delay) of ΔT_3, the signal P_3 can be generated. Similarly, P_4 can be generated by changing pulse width and position. Therefore, P_{1-4} symbols and their complementary symbols can be used to generate the SNRE-8 modulated eye. It is clear from Fig. 8 that the SNRE-8 signal is channel-dependent. If the channel loss is too low, the generated signal becomes a PWM signal. Fortunately, the proposed decoder at the receiver side can decode the eye in the absence of loss. Tuning of the modulator on the transmitter side and the sampling points (voltage and time) at the receiver side might be needed to optimize SNR in low-loss channels. If the channel loss is too high, equalization is needed to compensate for the loss. In our proposed work, a three-tap time-domain FFE and a CTLE are used for equalization. The proposed signal generation method shows that by subtracting rising edges together and falling edges together, common-mode shifts will occur between two consecutive symbols. Common-mode shifts will be filtered by the common-mode rejection of the differential structure in the analog front end and the differential comparators.

Fig. 9 shows the PSD of the proposed SNRE-8 signal as well as the PSD of PAM-4 and PAM-8 signals at a data rate of 30 Gb/s. PRBS31 was used in this simulation. Since the channel is needed to perform AM on the SNRE-8 signal, the PSD plots of the SNRE-8 signal before and after the channel are shown in Fig. 9. The channel has an insertion loss of 13 dB at 5 GHz. The PAM-4 and PAM-8 simulations do not include a channel as their PSD is channel-independent.

C. Mutually Exclusive Eyes

The proposed SNRE-8 modulation has an additional feature of mutually exclusive eyes, which helps to further improve the

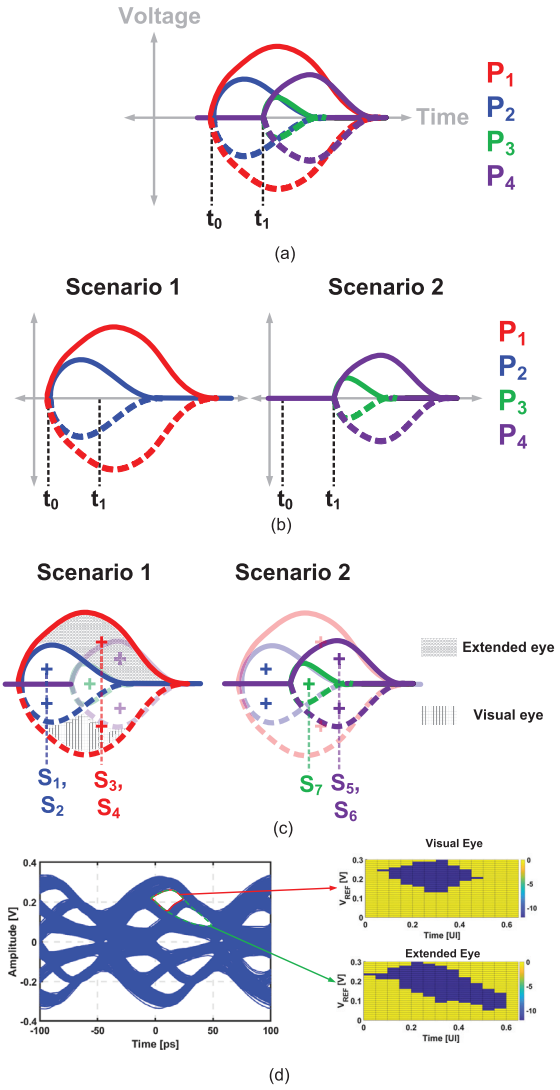


Fig. 10. (a) Proposed SNRE-8 signal diagram with t_0 and t_1 markings. (b) Two scenarios that construct the proposed SNRE-8 signal. (c) Sampler position and eye margins of the two scenarios. (d) Simulation of a 30-Gb/s SNRE-8 signal over 13-dB channel with two types of decoder; visual eye decoder, and extended eye decoder.

eye margin of the received data. The SNRE-8 eye diagram can be decomposed into two mutually exclusive scenarios. Fig. 10(a) shows a sketch of the proposed SNRE-8 signal with two time markings t_0 and t_1. The time markings t_0 and t_1 denote the two instances at which pulses might start to rise (or fall in case of negative pulses). Therefore, the proposed SNRE-8 signaling can be decomposed into two scenarios, a scenario where the pulses start rising/falling at time t_0, which is called scenario 1, and a scenario where the pulses start rising/falling at time t_1, which is called scenario 2. Fig. 10(b) shows a diagram of scenario 1 and scenario 2, where pulses P_1 and P_2 are in scenario 1, and P_3 and P_4 are in scenario 2. Since only one pulse is transmitted at a time, the transmitted signal can be in either scenario 1 or scenario 2, i.e., scenario 1 and scenario 2 are mutually exclusive. If this information is used by the receiver, better sampling margins (vertical and horizontal) can be achieved. Fig. 10(c) shows scenarios 1 and 2 in the presence of samplers S_{1-7}. In scenario 1, pulses P_3 and P_4 do not exist, therefore the outputs of samplers S_{5-7} are irrelevant

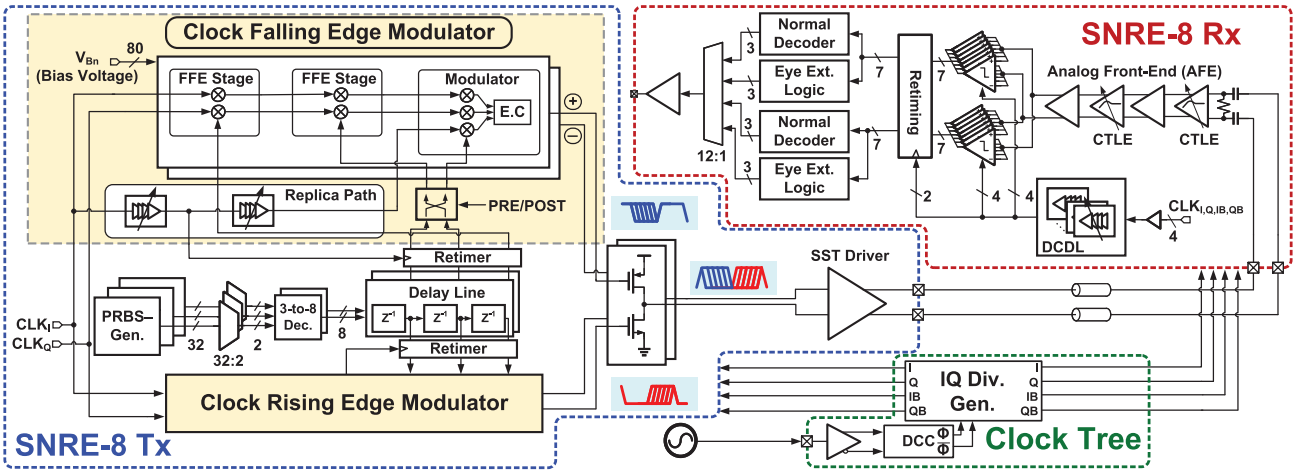


Fig. 11. Schematic of the proposed SNRE-8 transceiver architecture.

to the decoded data. This allows us to extend the margins of S_{3and4} samplers by using this mutually exclusive information. These extended eye boundaries are shown as a shaded region in the top part of the eye in Fig. 10(c). On the other hand, if we do not use this mutual exclusive information at the receiver and rely on the visual eye, the eye boundaries are smaller, as shown in the shaded area in the bottom part of the eye in Fig. 10(c). Similarly, in scenario 2, information from S_{3and4} is irrelevant because P_1 and P_2 do not exist in scenario 2. It should be noted that the results of S_{1and2} samplers are critical in both scenario 1 and scenario 2 as S_{1and2} information can determine which scenario the transmitted signal belongs to. Due to the importance of information from S_{1and2} samplers, their margins must be large enough for correct detection as their margins do not benefit from eye extension. Fig. 10(d) shows a simulation result of the SNRE-8 eye on a 13-dB channel and 30-Gb/s data rate. In situ eye is simulated using two types of decoders: visual eye decoder and extended eye decoder. Visual eye decoder does not utilize the mutual exclusive scenarios and the extended eye decoder utilizes the mutual exclusive scenarios. It can be observed that the eye margins of the in situ eyes are larger when the extended eye decoder is used.

IV. Proposed SNRE-8 Transceiver

The schematic of the proposed SNRE-8 transceiver architecture is shown in Fig. 11. The proposed transmitter consists of three pseudo random bit sequence (PRBS) generators for each of the three modulated bits. The output of the PRBS generators (32 bit wide) is fed into three half-rate 32-to-2 multiplexers. The output of the multiplexers is one-hot encoded, and it is passed through a delay line to generate time-delayed versions of the data for equalization. The proposed transmitter has the programmability to either use one main-tap and two post-cursor taps or one main-tap, one post-cursor tap, and one pre-cursor tap. The outputs of the delay line are then used to modulate the rising edge and falling edge of two clock signals separately. More details about the modulator structure are shown in Section IV-A. The outputs of the Clock Rising Edge Modulator and Clock Falling Edge Modulator are combined using PMOS pull-up and NMOS pull-down transistors, respectively. A single slice source-series terminated (SST) output driver is used to transmit the double-edge modulated data. Since the AM is done by leveraging the channel loss, the transmitter output driver generates only two output levels at the near end of the channel that get subtracted at the receiver. Multiple voltage levels are generated by the ISI of the channel and the delay values from the modulator at the far end of the channel. Therefore, the linearity of the driver is not a concern. Any mismatch between the positive and negative slices of the driver can be corrected by introducing an offset in the delay values between the positive and negative sides of the modulator. The receiver consists of two CTLEs and two amplifiers as an analog front end followed by half-rate samplers, and two different types of decoders. The normal decoder is based on the visual eye, and the eye extension logic decoder is based on the extended eye shown in Section III-C. Digitally controlled delay lines (DCDLs) are used to generate different sampling phases for the samplers and retimers. Clock generation is done using a quadrature divider to generate I-Q phases.

A. Clock Edge Modulator

The schematic of the clock edge modulator is shown in Fig. 12. The clock edge modulation is performed by changing the strength of a pull-down network based on the incoming data. The slowed-down edge rates are then recovered by a chain of buffers. The data bits are one-hot encoded DEC_{0-7} to have only one pull-down branch enabled at a time. This allows for independent control of delay corresponding to different symbols as only one branch is enabled at a time. Bias voltages are used to control the strength of the pull-down network. The values of the bias voltages are supplied from on-chip resistive ladder digital-to-analog converters (DACs). The value of the digital control from each DAC is manually calibrated in the measurement using external control. Transistor M1 is used to remove the memory from the pull-down node X by pulling up the voltage of node X to V_{DD} after each falling edge.

The proposed SNRE-8 system requires the modulator to generate delays as large as 0.8 UI. This large delay is difficult to achieve using the proposed modulator in Fig. 12. The reason is that to generate 0.8-UI edge delay, the edge rate must

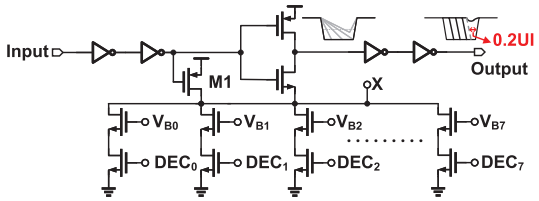


Fig. 12. Schematic of the proposed SNRE-8 edge modulator.

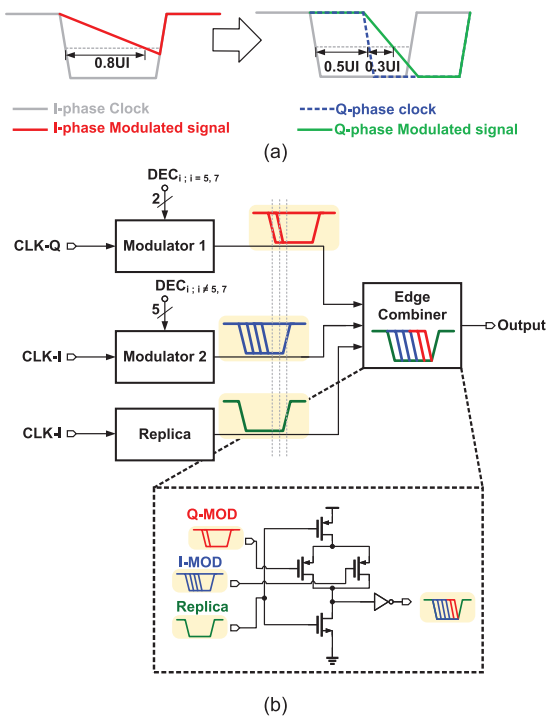


Fig. 13. (a) Waveform of I-phase modulator versus Q-phase modulator to generate 0.8-UI delay. (b) Schematic of the proposed edge combiner.

be very slow, and the slow edge barely crosses the inverter threshold, which leads to the disappearance of the 0.2-UI pulse that should have been generated, as shown in Fig. 12. To address this limitation in the modulator, a Q-phase modulator is used to generate large delays. By using a Q-phase clock for modulation, an inherent 0.5-UI delay exists in the incoming clock. Fig. 13(a) shows how Q-phase modulation (PM) relaxes the edge rate requirement. Fig. 13(a) (left) shows how 0.8-UI delay can be generated using the I-phase for modulation, which results in an incomplete discharge of the output node. The right side shows that if a Q-phase clock is used for modulation, the modulator needs to introduce only a 0.3-UI delay to the falling edge. Therefore, complete discharge of the output node is achieved. However, the rising edge of the Q-phase modulator is not aligned with the rising edge of the I-phase modulator. Therefore, an edge combiner circuit is used to align the rising edge. Fig. 13(b) shows the operation and schematic of the edge combiner circuit. To generate delays smaller than 0.5 UI, the I-phase modulator is enabled, otherwise, the Q-phase modulator is enabled. Since only one symbol is transmitted at each rising/falling edge, only one modulator is enabled at each rising/falling edge (I-phase modulator or Q-phase modulator), i.e., only one modulated edge arrives

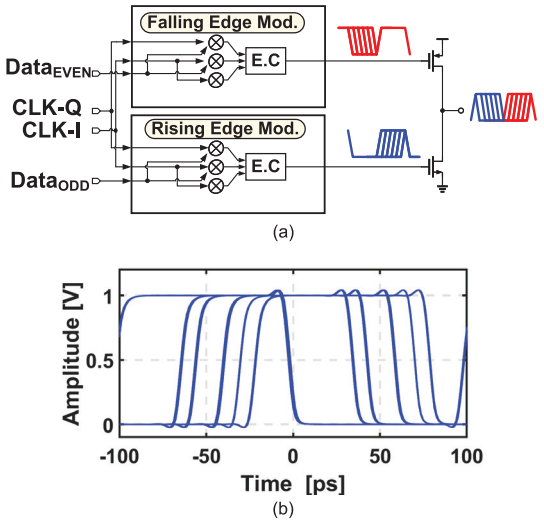


Fig. 14. (a) Schematic of the double edge modulator. (b) Simulation result of the double edge modulator at 30 Gb/s.

at the input of the edge combiner every clock cycle. The edge combiner circuit requires a replica un-modulated I-phase clock. The replica circuit controls the pull-down transistor of the edge combiner and, therefore, generates one rising edge (after inversion). The pull-up is controlled by either I-phase or Q-phase modulator outputs, which are mutually exclusive. A similar modulator is implemented to modulate the rising edge of the clock. To generate double edge-modulated signal, the rising edge-modulated signal is used to control a pull-down NMOS transistor whereas the falling edge-modulated signal is used to control a pull-up PMOS transistor as shown in Fig. 14(a). Fig. 14(b) shows a simulation of the double-edge modulator at 30 Gb/s.

The proposed SNRE-8 modulator can be tuned to compensate for process, voltage and temperature (PVT) variation. Fig. 15(a) shows the simulated differential output of the modulator at different process corners. Due to the process variations, the delay varies across corners. However, the correct delay values can be set by tuning the bias voltages of the modulator to compensate for the process variations as shown in Fig. 15(b).

B. Time-Domain FFE

The proposed SNRE-8 modulation is done in the time domain, therefore the differential signal has a variable pulse-width. This makes the conventional voltage-domain FFE not a viable option to compensate for ISI. Therefore, a time-domain FFE is used instead. Fig. 16(a) shows the concept of the time-domain FFE where the differential transmitted signal at the transmitter side is shown on the left. In the absence of equalization, if two positive pulses followed by a negative pulse are transmitted, as shown in Fig. 16(a) (top left), the channel loss will introduce ISI, which will affect the height of the received negative pulse as shown on the top right. However, if the second positive pulse has a reduced width at the transmitter, as shown in Fig. 16(a) (bottom left), then the ISI will be reduced at the receiver (bottom right) due to two reasons.

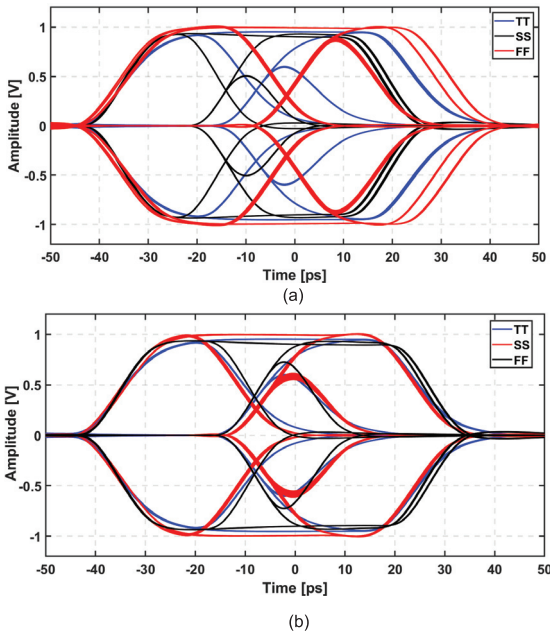


Fig. 15. (a) Simulated differential output of the modulator at different process corners without tuning the bias voltages. (b) Simulated differential output of the modulator at different process corners after tuning the bias voltages.

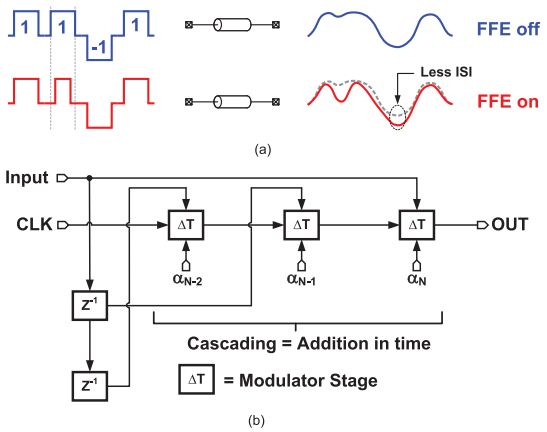


Fig. 16. (a) Example of the proposed time-domain FFE. (b) Block diagram of the proposed time-domain FFE.

1) PM to AM conversion reduces the amplitude of the second positive pulse, thereby achieving a similar effect to a voltage-domain FFE.
2) More guard time is introduced between the pulses, leading to less effect of ISI.

To build the time-domain FFE, three cascaded stages of the modulator are used since addition in time can be done through cascading. Each stage is controlled by a delayed version of the data. Since all equalization is done in the time domain, a single slice SST driver is needed, which reduces the power dissipation of the driver. Setting the values of the delays is similar to a voltage-domain FFE. In the absence of FFE, each symbol generates a certain delay. When FFE is used, this given delay is scaled by the FFE coefficients (corresponding to the pre-cursors, main cursor, and post cursors), which are chosen so that they add up to unity. Since the information is carried in the delay difference between two clock signals, the delay

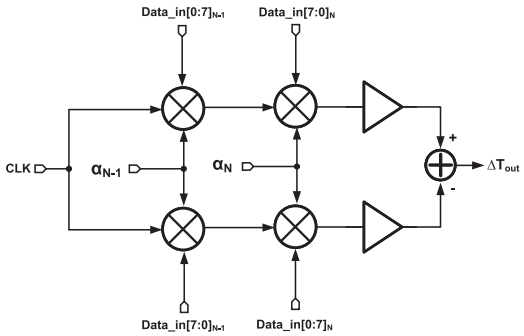


Fig. 17. Schematic of two-tap time-domain FFE.

difference can be mathematically described by

$$\Delta T_n = T_n - T_{7-n} \tag{6}$$

where n is the symbol index that varies from 0 to 7, and T_n and T_{7-n} are the time delays of the two clock signals. It should be noted that the value of ΔT_{7-n} is equal to $-\Delta T_n$ because we have four positive pulses and four negative pulses after subtracting the two clock signals. A two-tap FFE is considered as an example for simplicity. Fig. 17 shows a schematic of a two-tap FFE implementation. The one-hot encoded data that is driving the post-cursor modulator has a flipped polarity compared to the data that is driving the main cursor modulator. Therefore, the polarity of the delay for the post cursor is flipped with respect to the main cursor. If two consecutive ΔT_n are sent through the modulator, the final output ΔT_{out} is given by

$$\Delta T_{\text{out}} = \alpha_N \Delta T_n + \alpha_{N-1} \Delta T_{7-n} \tag{7}$$

where α_N and α_{N-1} are the coefficients for main and post cursors, respectively. By substituting (6) into (7), the final output can be defined as

$$\Delta T_{\text{out}} = (\alpha_N - \alpha_{N-1}) T_n - (\alpha_N - \alpha_{N-1}) T_{7-n}. \tag{8}$$

For example, if ΔT_n is 0.8 UI, then if α_N is 0.9, the final output will have a pulse width of 0.64 UI according to (8). Therefore, when two consecutive symbols are sent through the modulator, the overall pulse width is reduced similar to voltage-domain FFE where the pulse amplitude is reduced. In the presence of a negative post-cursor in the channel, the FFE can compensate it by adding an option to flip the polarity of the data controlling the post-cursor modulator stage. This has not been implemented in the current design. Since each cursor (modulator stage) has eight possible output delays for eight possible input data symbols, eight bias voltages need to be tuned for a single coefficient change. For example, in the absence of FFE, the main cursor can generate eight different delays T_{0-7} which are generated by eight different bias voltages V_{B0-B7}. If the value of α_N is changed, then the delays need to be changed from T_{0-7} to $\alpha_N T_{0-7}$. Therefore, eight new bias voltages need to be tuned to generate the new delays. Therefore, the proposed FFE is more difficult to tune than a conventional voltage-domain FFE as for each modulator stage eight control voltages need to be tuned.

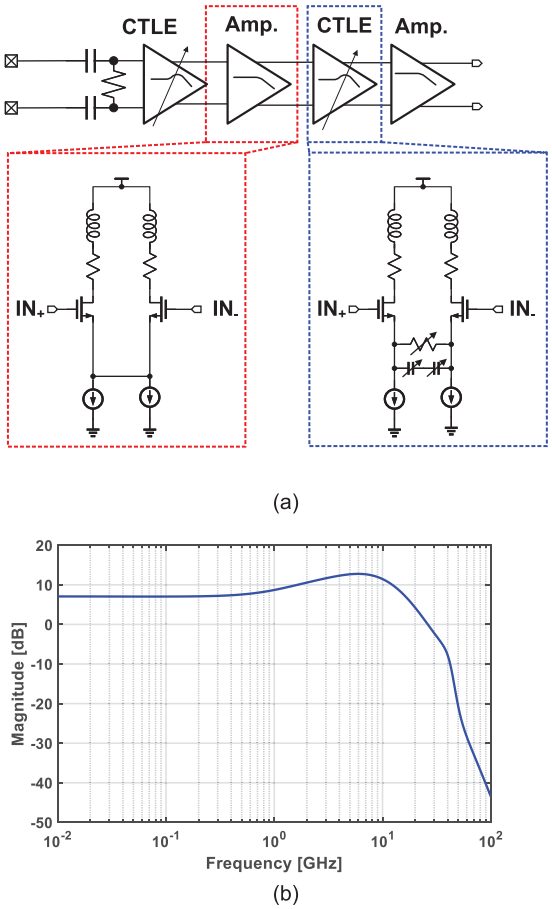


Fig. 18. (a) Schematic of the analog front end. (b) Post-layout simulation of the analog front end.

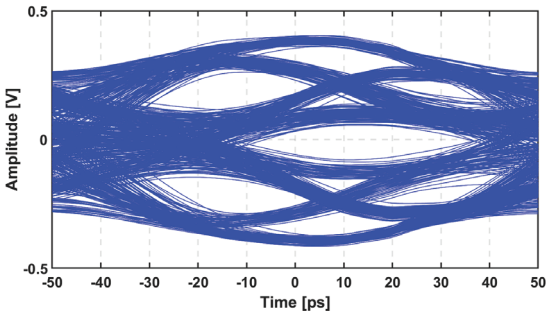


Fig. 19. Simulation of the analog front-end differential output.

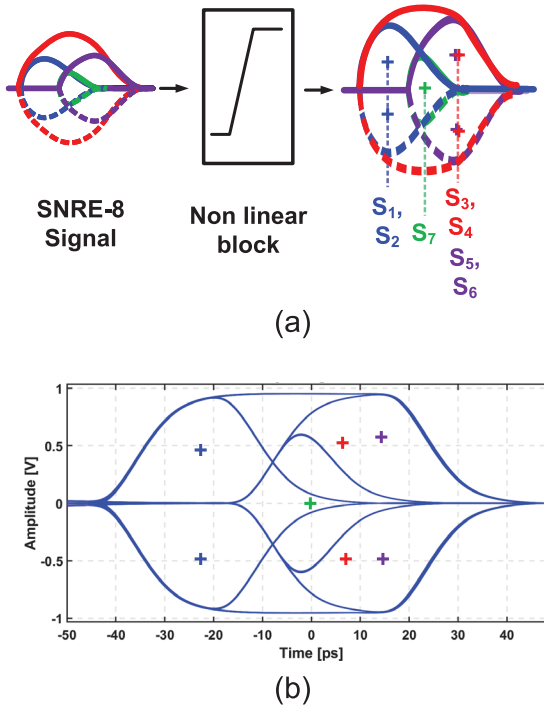


Fig. 20. (a) Effect of non-linearity on SNRE-8 signal detection. (b) Detection of SNRE-8 signal in the absence of ISI.

C. Receiver

The receiver consists of a two-stage CTLE and a two-stage amplifier as an analog front end. The schematics of the CTLE and amplifier stages are shown in Fig. 18(a). Fig. 18(b) shows the post-layout [resistor and coupling-capacitor (RCC)] simulation result of the entire analog front end, which has a gain of 7 dB, peaking of 5.7 dB, and a bandwidth of 20.3 GHz. Fig. 19 shows a simulation of the SNRE-8 differential output of the analog front end at a data rate of 30 Gb/s. The channel used in the simulation in Fig. 19 has a 13-dB insertion loss at 5 GHz. The minimum eye opening is 110 mV and the integrated noise at the output (including input referred noise of the comparators) is 2.4-mV rms, therefore, the SNR at the output of the analog front end is 33.2 dB. The linearity requirement of the analog front end is relaxed when the SNRE-8 signal is detected with the extended eye decoder. If the SNRE-8 signal is passed through a non-linear block as shown in Fig. 20(a), it can be shown that by aligning the samplers $S_{3\text{and}4}$ and $S_{5\text{and}6}$ (from Fig. 10) the SNRE-8 signal can be decoded using the eye extended decoder explained in Section III-C. Fig. 20(b) shows the output of the modulator in the absence of ISI (i.e., signal is PWM). The samplers can be set as shown in Fig. 20(b) using the same extended eye decoder. It should be noted that the reduced amplitude of the S_7 eye is due to the finite bandwidth of the modulator output. Despite the visual closure of the S_7 eye, the mutual exclusivity between the pulses of P_2 and P_3 (from Fig. 10) ensures that the S_7 eye is functionally open.

A half-rate architecture is used with a strongARM latched comparator as a sampler. To generate the different sampling phases for different eyes, DCDLs are used to control the delay of the sampling clock of each comparator, as shown in Fig. 11. For the purpose of this design, the static control of the DCDL was manually calibrated externally during measurement. For a practical implementation, feedback logic will be needed to set the clock phases automatically. The schematic of the DCDL is shown in Fig. 21. No comparator offset correction is implemented in this design. Offset correction can be implemented by sensing the offset of the comparator during calibration and tuning the reference voltage to cancel the value of the offset.

D. PAM-8 Transmitter

To perform an apple-to-apple comparison with a PAM-8 system, an on-chip PAM-8 transmitter is implemented on the same chip. The schematic of the PAM-8 transmitter is shown

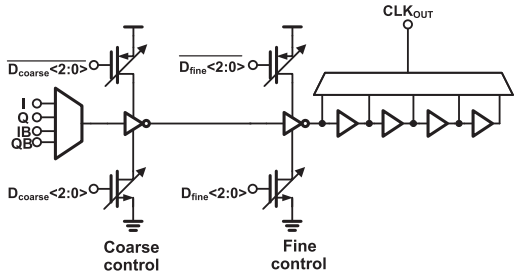


Fig. 21. Schematic of the DCDL.

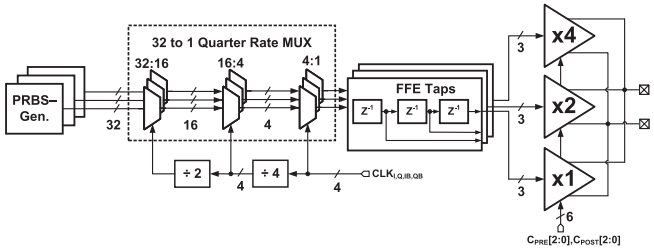


Fig. 22. Schematic of the implemented PAM-8 transmitter.

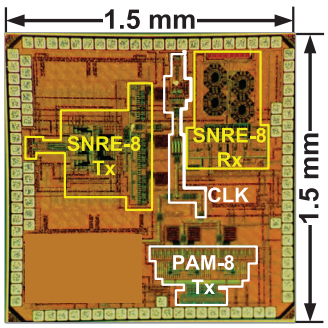


Fig. 23. Chip micrograph.

in Fig. 22. The PAM-8 transmitter consists of three PRBS generators, and three quarter rate 32-to-1 multiplexers with a three tap delay line to generate main, pre, and post cursors for the FFE. A segmented SST driver is used to generate an FFE equalized PAM-8 signal with a 3-bit resolution for equalization.

V. Measurement Results

The proposed SNRE-8 transceiver along with the PAM-8 transmitter are implemented on a 65-nm CMOS process. Fig. 23 shows the chip micrograph. The chip area is 2.25 mm^2 and the active area is 0.6 mm^2. The proposed SNRE-8 transceiver occupies an area of 0.479 mm^2, while the PAM-8 transmitter occupies an area of 0.127 mm^2. Chip-on-board assembly is used to minimize bond-wire and package parasitics. Fig. 24 shows a diagram of the measurement setup. Two boards are used, one for the transmitter and the other one for the receiver. An external clock generator (HP83640B) was used to generate a clock reference for both the TX and the RX. The output of the transmitter was monitored using a high bandwidth oscilloscope (CSA8200) at both the near end and far end of the channel. The output of the receiver was monitored using the BERT (BSA286CL) to measure the BER. Three channels are used in the measurement, as shown in Fig. 25(a). Channel 1 corresponds to the near-end channel,

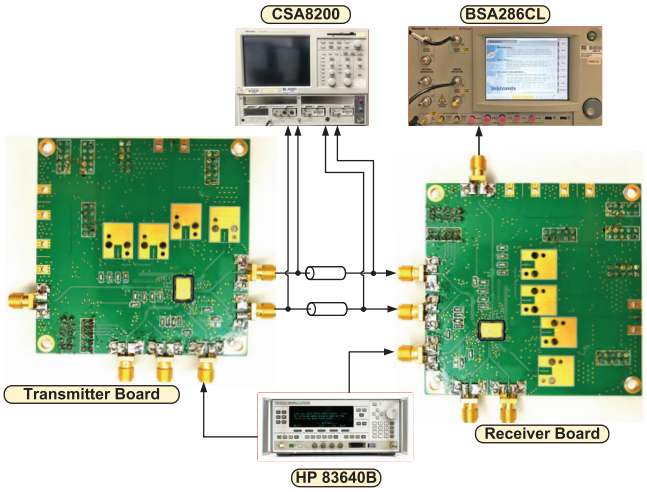


Fig. 24. Measurement setup.

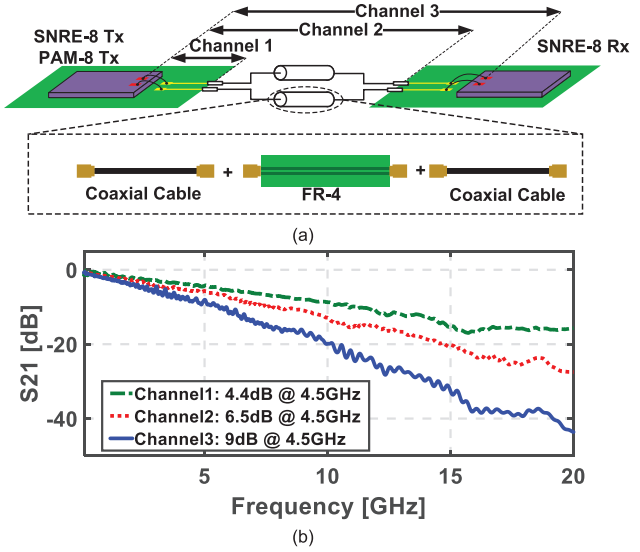


Fig. 25. (a) Diagram of the three measured wireline channels. (b) Insertion loss of the three measured wireline channels.

which consists of the transmitter board FR-4 trace and a coaxial cable. The loss of Channel 1 is 4.4 dB at 4.5 GHz (for a data rate of 27 Gb/s), as shown in Fig. 25(b). Channel 2 consists of Channel 1 in addition to more FR-4 traces and coaxial cables. The loss of Channel 2 is 6.5 dB at 4.5 GHz. Channel 3 consists of Channel 2 in addition to receiver FR-4 traces with a loss of 9 dB at 4.5 GHz.

Fig. 26 shows the measured eye diagrams at 27 Gb/s for Channels 1 and 2 for the PAM-8 and SNRE-8 transmitters when using PRBS7 pattern. Both the PAM-8 driver and SNRE-8 driver have the same supply voltage of 1.1 V. When Channel 1 is used, both voltage-domain FFE for the PAM-8 transmitter and time-domain FFE for the SNRE-8 transmitter are turned off. At Channel 1 output, the average vertical eye margin is 68.8 mV for PAM-8, as shown in Fig. 27. If the visual eye only is considered in the measurement, the average SNRE-8 vertical eye margin is 204.8 mV, which corresponds to a 9.5-dB boost in SNR, as shown in Fig. 27. If eye extension logic is enabled, the average SNRE-8 vertical eye margin becomes 232.95 mV, which corresponds to 10.6-dB

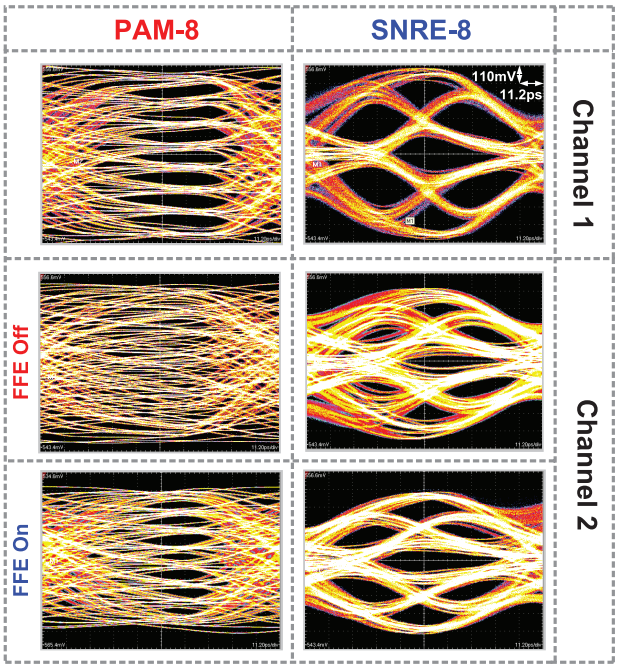
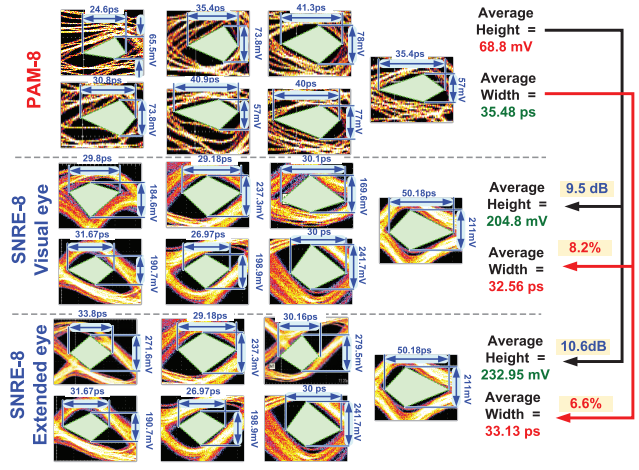


Fig. 26. Measured eye diagrams at 27 Gb/s for PAM-8 and SNRE-8 transmitters.



	PAM-8 Eye	SNRE-8 Visual Eye	SNRE-8 Extended Eye
Average Eye Height [mV]	68.8	204.8	232.95
Average Eye width [ps]	35.48	32.56	33.13

Fig. 27. Eye margin measurements for PAM-8 and SNRE-8 transmitters at 27 Gb/s for Channel 1.

SNR boost. Similarly, the horizontal eye margin reduction due to using the SNRE-8 modulation is 8.2% for the visual eye decoding, and 6.6% with the eye extension decoder (see Fig. 27). Channel 2 eye diagrams (see Fig. 26) show that in the absence of any equalization, the SNRE-8 eye is still open whereas the PAM-8 eye is shut. When the FFE is enabled in both systems, the PAM-8 eye is slightly open. The SNR boost for the proposed SNRE-8 modulation for Channel 2 with the time-domain FFE is 8.7 dB.

Fig. 28 shows the measured in situ eye diagrams for the SNRE-8 eyes at the receiver when transmitted on Channel 3 (9-dB loss) at 27 Gb/s. S_1–S_7 eyes correspond to the eyes sampled by comparators S_{1-7} that are shown in Fig. 10(c).

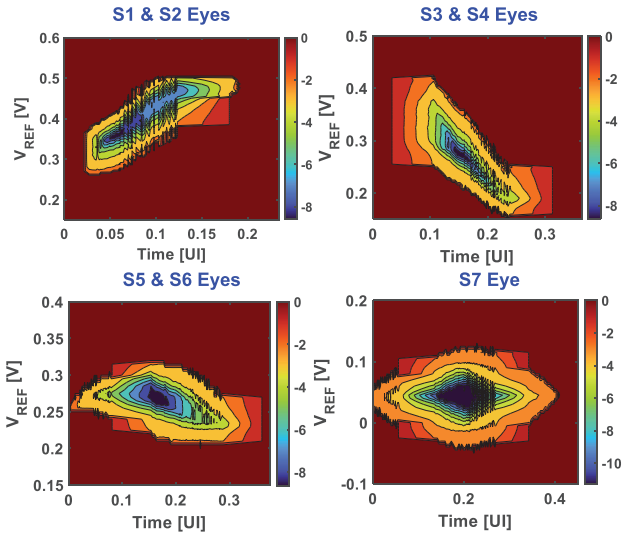


Fig. 28. Measured in situ eye diagrams at the output of the receiver when transmitted over a channel of 9-dB loss at 27 Gb/s.

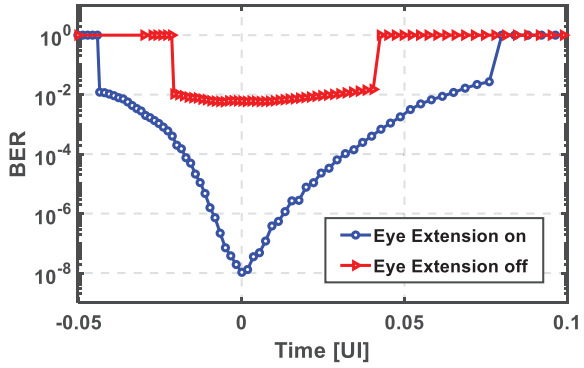


Fig. 29. Measured bathtub plot at the output of the receiver when transmitted over a channel of 9-dB loss at 27 Gb/s.

The decoder that was used in Fig. 28 measurement is the eye extension decoder which exploits the extended margins for S_3 and S_4 eyes. The FFE is turned off for this measurement and only the CTLE is used for equalization. The bathtub plot measurement was done for the proposed SNRE-8 modulation with Channel 3 and 27-Gb/s data rate, as shown in Fig. 29. When the eye extension decoder is used, the BER of the proposed SNRE-8 modulation can reach 10^{-8}, whereas when visual eye decoder is used the proposed SNRE-8 modulation can only achieve a BER of 6×10^{-3}. The power breakdown of the proposed SNRE-8 transceiver at 27 Gb/s is shown in Fig. 30. The proposed SNRE-8 transceiver dissipates 145.62 mW, whereas the PAM-8 transmitter dissipates 72.87 mW. The power overhead in the proposed SNRE-8 transmitter is 23% compared to the PAM-8 transmitter. While the power consumption of the proposed SNRE-8 transmitter is higher than that of the PAM-8 transmitter, we believe that the additional power in the SNRE-8 transmitter is justified by achieving a 10.6-dB SNR gain over PAM-8.

A comparison with prior works is shown in Table I. The selected works for comparison are PAM-8 [31], PAM-4 [41] transceivers of similar process technology, an SNRE transceiver [37], other published PAM-8 transmitters [42], [43], a 28-Gb/s NRZ transceiver [17], and a

TABLE I
COMPARISON WITH PRIOR WORK ON WIRELINE TRANSCEIVERS

	SNR Enhancement Links			Conventional Links					
	This work		Aurangozeb, JSSC'20 [37]	Y. Chun, ESSCIRC'19 [31]	A. Roshan-Zamir, JSSC'17 [41]	J. Yang ISSCC'23[42]	T. Dickson VLSI'22[43]	J. Im VLSI'18 [17]	P. Upadhyaya, ISSCC'18 [19]
Process	65nm CMOS		28nm FDSOI	65nm CMOS	65nm CMOS	40nm CMOS	4nm FinFET	7nm FinFET	16nm FinFET
Bits/symbol	3		2	3	2	3	2-3	1	2
Modulation	SNRE-8 (Tx + Rx)	PAM-8 (Tx only)	Sequence Encoded PAM-4	PAM-8	PAM-4	PAM-8	PAM-4 and PAM-8	NRZ	PAM-4
Equalization	3-tap FFE + CTLE	3-tap FFE	3-tap FFE, Sequence encoding, CTLE, Trellis Decoding	4-tap RX FFE	3-tap FFE + 2-tap DFE	3+1 Hybrid FFE	8-tap FFE	3-tap FFE+ 15-tap DFE+ CTLE	4-tap FFE + CTLE + 1-tap DFE (DSP) + 14-tap RX FFE (DSP)
Data Rate (Gb/s)	27	27	28	36 - 39.6	32	100Gb/s	144/216	0.5-28	19-56
Channel Loss (dB)	9	-	30	12.7, 14	13.5	9.4	8.8	30	7.4, 32
BER	10^{-3} * / 10^{-8}	-	10^{-12}	10^{-6}, 10^{-4}	10^{-12}	-	-	10^{-15}	10^{-12}
SNR Gain (dB)	9.5* / 10.6	-	5.26	-	-	-	-	-	-
Data-rate Overhead	0	0	12.5%	0	0	-	-	-	-
Tx Power (mW)	89.77	72.87	38	-	158.6	335	288	-	-
Tx Power Efficiency (pJ/bit)	3.32	2.7	1.1875**, 1.357***	-	4.96	3.35	2,1.33	-	-
TxRx Power (mW)	145.62	-	93	311.4 ,342.9	176.3	-	-	283	360, 545
TxRx Power Efficiency (pJ/bit)	5.39	-	2.9**, 3.32***	8.66, 8.65	5.5	-	-	10.1	6.4, 9.7
Area (mm^2)	0.48	0.127	0.4	0.39	0.074	0.362	0.047	2.75****	8.778****

* Eye extension logic off
** Based on baud-rate
*** Based on effective data-rate
**** Full chip area that includes four channels

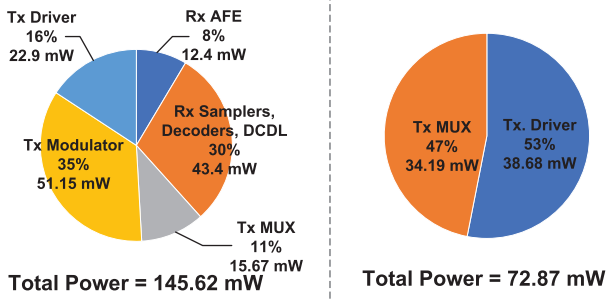


Fig. 30. Power breakdown of the proposed SNRE-8 transceiver and the PAM-8 transmitter.

56-Gb/s PAM-4 transceiver [19]. Compared to the prior published PAM-8 transceiver [31], [32], the proposed SNRE-8 transceiver dissipates 37.7% less energy per bit. Compared to the SNRE transceiver in [37], the proposed SNRE-8 modulation achieves 5.34-dB more SNR improvement. The work in [37] shows lower BER at higher channel loss. However, Aurangozeb et al. [37] uses a 64-UI delay trellis decoder in addition to a data rate overhead of 12.5%. According to [37], the decoder can improve the BER from 10^{-6} to 10^{-12}. The proposed SNRE-8 system can achieve 10^{-8} BER using direct detection without any latency penalty. Introducing a low-latency FEC decoder can help achieve a BER of 10^{-12}. Compared to the PAM-8 transmitter in [42], the proposed SNRE-8 transmitter achieves similar power efficiency; however, Yang et al. [42] operates at a much higher data rate. The eye diagram in [42] shows healthy margins due to the use of high supply voltage for the driver to improve the SNR. Dickson et al. [43] achieve very high energy efficiency and data rate using 4-nm FinFET technology. In [41], the system operates at a slightly higher data rate with slightly worse power efficiency at the same technology level. The channel loss in [41] is 13.5 dB when the PAM-4 signal is used. Fig. 2(a) shows that using PAM-4 on the SNRE-8 channel results in a loss of 13.5 dB. Therefore, the physical channel in [41] is similar to the channel used in the proposed SNRE-8 system. However, using a higher order modulation results in a lower channel loss of 9 dB compared to 13.5 dB in the case of PAM-4. In [17], a power efficiency of 10.1 pJ/bit is shown on a 7-nm FinFET technology on a 30-dB channel. The channel shown in Fig. 2(a) shows that the channel loss is 27 dB if NRZ signaling is used. This means that compared to [17] the proposed SNRE-8 achieves a better energy efficiency over almost similar data rate and channel using an older technology node (65 nm). It should be mentioned that the work in [17] includes a fast-locking clock and data recovery (CDR), which adds to the power of the system. In [19], the energy efficiency of a PAM-4 system at a low loss of 7.4 dB is 6.4 pJ/bit, which is worse than the proposed SNRE-8 energy efficiency operating at a higher loss for eight-ary modulation (9 dB) despite the technology advantage for [19]. It must be noted that the work in [19] also includes the power consumption of a PLL and a DSP-based CDR.

VI. FUTURE DIRECTIONS FOR SNRE-8 TRANSCEIVER

The key contribution of this article is the presentation and initial proof point demonstration of a new technique (SNRE-8), which is worth further exploration. The edge modulator tuning, the receiver clock phases tuning, and the reference voltages tuning for the comparators are all done manually in this work. For a fully automated tuning of the system parameters, the system must undergo some training before the link is up. In this type of training, a PRBS data pattern is sent through the link and all the reference voltages and clock phases must be tuned until successful PRBS-detection is achieved at the desirable BER. To build a CDR for the proposed SNRE-8 system, a phase detector that can provide phase error in the sampling clock phases is required. Such a phase detector is an open research problem due to the existence of multiple sampling points in the SNRE-8 eye. One of the biggest challenges to scaling the proposed SNRE-8 modulation for the next-generation standards (100G/200G/400G per lane) is the generation of the narrow pulse width of 0.2 UI. Since the shortest pulse serves only as a method to reduce the effect

of ISI, one can relax this 0.2-UI pulse width at the expense of using some other equalization techniques in the transmitter or the receiver. The use of fine technology nodes such as 5 nm could also help to alleviate some of the challenges in generating narrow pulse width. We also hope that more research and investigation in finding innovative ways of generating the SNRE-8 modulation, which does not require generating a narrow pulse width, may help to overcome the scalability challenges of the current SNRE-8 transmitter architecture.

VII. Conclusion

This article presents a new eight-ary modulation that aims to boost the SNR compared to a conventional PAM-8 system. By implementing an eight-ary modulation system, the clock frequency is reduced by 33% over conventional PAM-4 which reduces the power of clock generation and distribution. However, this also results in more power due to the increase in the number of samplers and the required number of clock phases. The proposed SNRE-8 system leverages pulse width, position, and AM to achieve SNR improvement. Moreover, due to changing the pulse position, the proposed SNRE-8 modulation has mutually exclusive eyes, which further helps to improve the eye margins. The proposed SNRE-8 signal traded off 6.6% eye width reduction for a 3× eye height increase compared to PAM-8. The proposed SNRE-8 transceiver was implemented on a 65-nm process along with a PAM-8 transmitter for comparison purposes. The proposed SNRE-8 modulation achieves 10.6-dB SNR improvement over PAM-8 at 4.4-dB channel loss. The SNRE-8 transceiver achieves a BER of 10^{-8} at 9-dB channel loss while operating at 27 Gb/s with a power efficiency of 5.39 pJ/bit.

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