# Minimum Power Point Design of Inverter Based Continuous Time Linear Equalizer (CTLE)

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***Abstract*—This paper presents the approach to design the inverter based CTLE at the minimum power consumption point and at minimum noise power product point while meeting the desired specification target. Lagrangian function for constrained optimization is formed. Mathematical close form expressions of the CTLE parameters are derived. Using the proposed design approach, an inverter based CTLE architecture with four different design constraints was designed and simulated in 16nm FinFET and in 65nm CMOS technology to validate existence of minimum power point design.**

***Index Terms*—CTLE, transconductance, noise, inverter-based.**

## I. Introduction

Data intensive applications and large distributed AI models such as GPT-3/4, Persia etc. have trillions of parameters that need to be moved from one processor to another [1]. The performance of these applications depend on the bandwidth and latency of data movement. As a result, the data rates have been increasing consistently to keep up with the growing demand [2]–[4]. In today's computer systems, the short reach communication channels used in wireline links between processor to memory and other peripheral is copper trace, these channels exhibit insertion loss, which increases with frequency. This insertion loss results in inter-symbol-interference (ISI) of the transmitted data. As a result, wireline links must employ equalization techniques to overcome the ISI and recover the data error free.

Continuous-time linear equalizers (CTLEs) is one of the popular equalization techniques to compensate for channel loss [5]. Conventional CTLE architectures offer limited voltage swing [6]–[9], which makes them difficult to meet desired specification in FinFET technology, which operates on sub-1V power supply and in higher order modulation, such as PAM-4, which suffers from lower SNR. More recently, inverter based CTLE architecture is gaining popularity [10], [11], due to its high energy efficiency, small area footprint, and most importantly its ability to provide large output voltage swing at low operating supply voltages. While the inverter-based CTLE is energy efficient, there are no clear design guidelines in the literature on how to size and optimize the CTLE architecture to operate at minimum power point and minimum noise power product point. In light of this deficiency, this work provides the closed form expression and design flow to design the inverter based CTLE architecture at the most energy efficient point. We validated our mathematical analysis though circuit simulations in two technology nodes: 65nm CMOS and 16nm finFET process across four different design specifications.

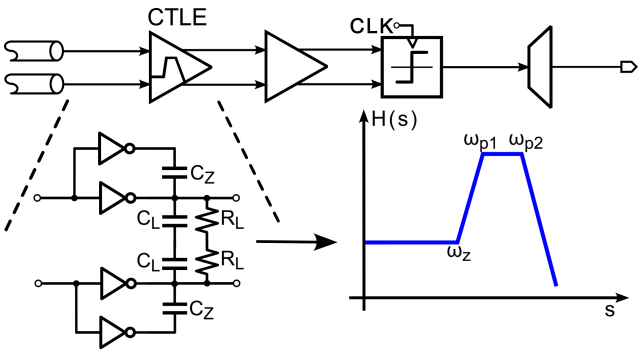


Fig. 1. A pseudo differential inverter based CTLE in the wireline receiver.

Following are the key contributions of this work:

- Mathematical analysis of the inverter based CTLE architecture to show the existence of minimum power point and minimum noise power product point.
- Derived closed form expressions to estimate the CTLE design parameters to arrive at the minimum power point.
- Validation of the minimum power point using CTLE design simulations in 16nm finFET and 65nm CMOS technology nodes.

Rest of the paper is organized as follows. Section II introduces the inverter based CTLE architecture, small signal model, and mathematical derivation of minimum power point. Section III presents a noise analysis. Section IV presents simulation results, and Section V concludes this paper.

## II. Inverter-Based CTLE Architecture

The Inverter-based CTLE architecture and its position in the wireline receiver front-end is shown in Fig. 1. The architecture consists of two inverters joined by a coupling capacitor $C_Z$ driving a load capacitance $C_L$. Load resistance $R_L$ models the output load resistance, which is added to achieve the desired DC gain in the CTLE. The transfer function has one zero $\omega_z$ and two poles $\omega_{p1}$ and $\omega_{p2}$.

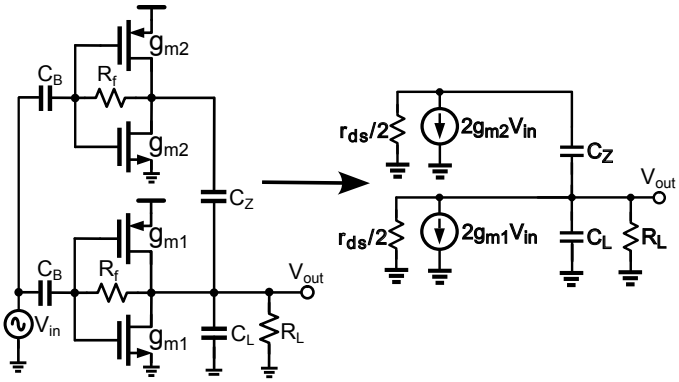


Fig. 2. Single ended CTLE schematic and associated small signal model.

The transistor level implementation of the single-ended inverter based CTLE and its equivalent small signal model is shown in Fig. 2. The inverters are sized and biased such that each inverter has a equivalent trans-conductance of $g_{m1}$ and $g_{m2}$, respectively. Received signal from the transmission line is coupled with each inverter using a DC blocking capacitor $C_B$. Output of the CTLE drives the amplifier and its load is modeled using capacitance $C_L$. To simplify the mathematical derivation for the minimum power analysis, it is assumed that both PMOS and NMOS transistor has same output resistance $rds$. The feedback resistors $R_f$ stabilizes the output common mode of the inverters. Since the value of $R_f$ should be sufficiently large, it has negligible affect on the inverter gain. Therefore, $R_f$ is removed from small signal model to greatly simplify the mathematics without losing accuracy.

### A. Transfer Function, Poles and Zeros

Gain transfer function of the CTLE using the small signal model in Fig. 2 is expressed as:

$$H(s) = \frac{-2r_{ds}R_L(sr_{ds}C_z(g_{m2}+g_{m1})+2g_{m1})}{s^2r_{ds}^2R_LC_zC_L+sr_{ds}(4R_LC_z+r_{ds}C_z+2R_LC_L)+2r_{ds}+4R_L} \quad (1)$$

The CTLE has two poles and one zero. Assuming two poles are located far away from each other, they are mathematically expressed as:

$$\omega_z = \frac{2g_{m1}}{r_{ds}C_z(g_{m1}+g_{m2})} \quad (2)$$

$$\omega_{p1} \approx \frac{(2r_{ds}+4R_L)(r_{ds}R_LC_LC_Z)}{4R_LC_Z+r_{ds}C_Z+2R_LC_L} \quad (3)$$

$$\omega_{p2} \approx \frac{4R_LC_Z+r_{ds}C_Z+2R_LC_L}{r_{ds}R_LC_LC_Z} \quad (4)$$

The DC Gain of the CTLE can be expressed as:

$$A_0 = -2g_{m1} \times \frac{r_{ds}R_L}{r_{ds}+2R_L} \quad (5)$$

### B. Minimum Power Point Derivation

In the CTLE design, the load capacitance ($C_L$), DC gain ($A_0$) and peaking gain ($\omega_{p1}/\omega_z$), which includes the peaking frequency of the CTLE, are the design specifications. The minimum power point analysis in this sub-section finds the design parameters $g_{m1}$, $g_{m2}$, $C_Z$, and $R_L$ such that CTLE consumes minimum power while meeting all design specifications.

Transconductance $g_{m1}$ and $g_{m2}$ of the two inverters directly correlates with the power consumption of the CTLE. Therefore, to minimize the power consumption, one must minimize cost function $g_{m1}$ + $g_{m2}$. The constrained optimization problem can be mathematically written as:

$$\begin{aligned}
&\text{Cost Function:} \quad F = g_{m1}+g_{m2}\\
&\text{Constraints:}\\
&C_1 = 2g_{m1}-\omega_z r_{ds}C_Z(g_{m1}+g_{m2}) = 0\\
&C_2 = A_0(r_{ds}+2R_L)+2g_{m1}r_{ds}R_L = 0\\
&C_3 = w_{p1}^2r_{ds}^2R_LC_zC_L - w_{p1}r_{ds}(4R_LC_z+r_{ds}C_z+2R_LC_L)\\
&\quad +2r_{ds}+4R_L = 0\\
&\text{Lagrangian Function:} \ \mathcal{L} = F-\lambda_1C_1-\lambda_2C_2-\lambda_3C_3
\end{aligned} \quad (6)$$

where $C_1$ corresponds to the constraint on $\omega_z$ arrived from equation (2), $C_2$ corresponds to the constraint on $A_0$ arrived from equation (5), $C_3$ corresponds to the constraint on $\omega_{p1}$ arrived from the denominator of equation (1), and $\mathcal{L}$ represents the Lagrangian expression with these three constraints. The optimal component values can be calculated by taking the partial derivative of $\mathcal{L}$ with respect to: $g_{m1}$, $g_{m2}$, $R_L$, $C_Z$, and $\lambda_{1-3}$, to get 7 separate equations all set to 0, solving that system of equations to find the minimum of cost function $F$ and optimal set of CTLE parameters. For minimum power point operation of CTLE, the $(g_{m1})_{opt}$ can be calculated as:

$$(g_{m1})_{opt} = \frac{|A_0|}{r_{ds}}\left(\frac{\omega_{p1}r_{ds}C_L}{2}+\sqrt{\frac{\omega_{p1}r_{ds}C_L}{2}}\right) \quad (7)$$

Optimal values of the other CTLE design parameters can be calculated using the design flow described in Fig 3. First $g_{m1}$ is calculated because it leads to a convenient process of substituting one value into the other as shown in the design flow. The value of $g_{m1}$ dominates the power drawn from the supply. If one were given the CTLE design specifications at the top of Fig. 3, the CTLE design process would be to first fix the value of $g_{m1}$, next calculate $R_L$ to satisfy DC gain requirement, next calculate $C_Z$ to satisfy first pole frequency (peaking frequency) requirement, and finally calculate $g_{m2}$ to satisfy the zero frequency requirement, which results in meeting the peaking gain ($\omega_{p1}/\omega_z$). The relationship between $g_{m1}+g_{m2}$ and $g_{m1}$ can be expressed as equation (8), which can be found using equations (2), (5), and the denominator of equation (1).

$$g_{m1}+g_{m2} = \frac{\omega_{p1}}{\omega_z r_{ds}}\frac{2g_{m1}^2r_{ds}+g_{m1}A_0(\omega_{p1}r_{ds}C_L-2)}{2g_{m1}+A_0\omega_{p1}C_L} \quad (8)$$

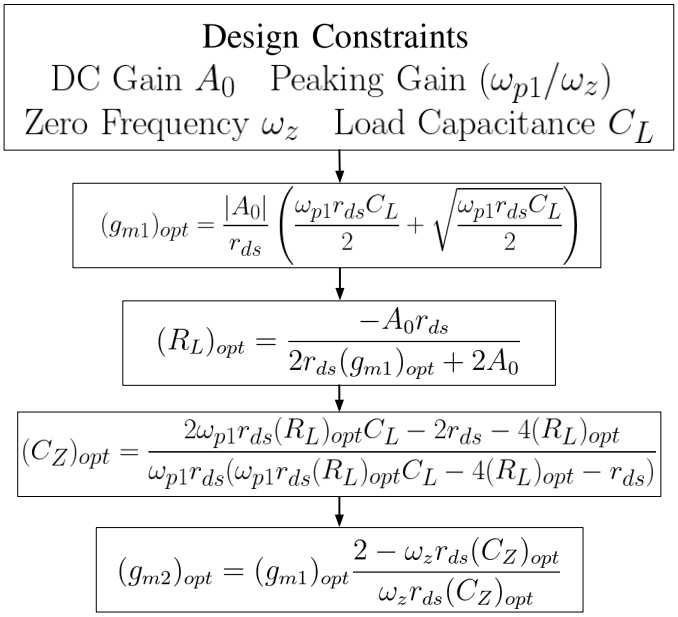


Fig. 3. Design flow to estimate CTLE parameters for minimum power.

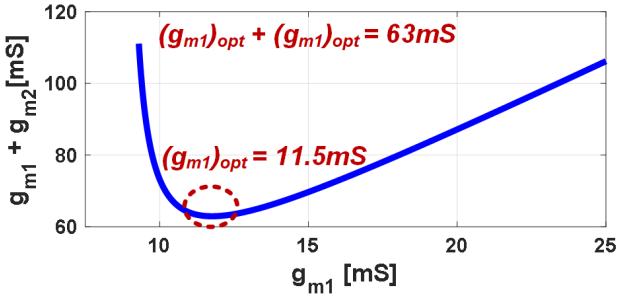


Fig. 4. Sum of transconductance as function of $g_{m1}$.

*Example*: Given the specifications of CTLE 0dB DC gain ($A_0$), 12dB peaking gain ($\omega_{p1}/\omega_z$), 28GHz peaking frequency ($\omega_{p1}$), 100f load capacitance ($C_L$), and 1kΩ drain-to-source resistance ($r_{ds}$), using equation (8), a plot of $g_{m1} + g_{m2}$ as a function of $g_{m1}$ is shown in Fig. 4. It can be observed that there exits a point where the sum of transconductance reaches the minimum value, which corresponds to the minimum power point of CTLE. The minimum is reached at the optimal $g_{m1}$ value of 11.5mS as described in equation (7). Substituting the optimal value of $g_{m1}$ into equation (8) the minimum sum of transconductance can be calculated as 63mS. Using the design flow in Fig. 3, all other CTLE parameters can be calculated.

## III. Noise Analysis

This section analyses the thermal noise contribution of the CTLE and finds the design parameters to minimize the product of noise and power. Since the value of the coupling capacitor $C_Z$ is smaller than the load capacitance $C_L$ (see Fig.2), to help simplify the derivation of integrated noise, it is assumed

$$\frac{1}{sC_Z} >> \frac{1}{sC_L} \parallel R_L \parallel \frac{r_{ds}}{2} \tag{9}$$

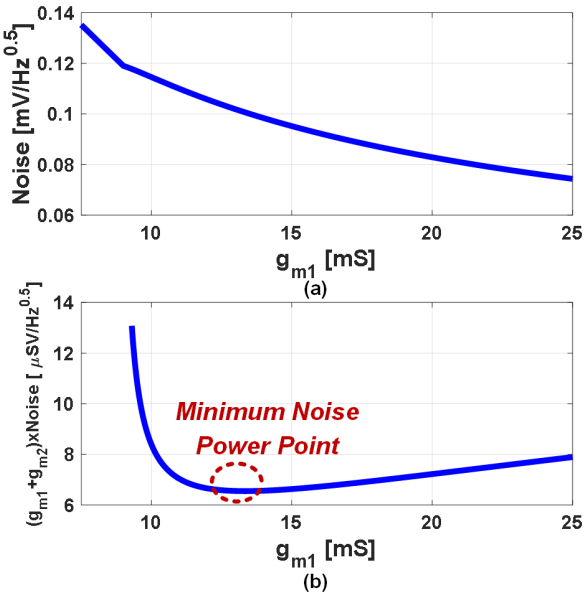


Fig. 5. (a) Integrated input noise of CTLE as a function of $g_{m1}$. (b) Product of transconductance and integrated input noise of CTLE as a function of $g_{m1}$.

This assumption will lead to a slight over estimate of total integrated noise. To calculate the total integrated output noise, the noise from individual noise contributors to the CTLE output are calculated independently and they are summed together as shown below:

$$\overline{V_{n,out}^2} = 4kT\left(\left(\frac{1}{R_L} + \frac{1}{R_f} + 2\gamma g_{m1}\right) + \left(\frac{1}{R_f} + 2\gamma g_{m2}\right)\left(\frac{sr_{ds}C_Z}{sr_{ds}C_Z + 2}\right)^2\right)\left(\frac{r_{ds}R_L}{sr_{ds}R_L C_L + r_{ds} + 2R_L}\right)^2 \tag{10}$$

where $\gamma$ is channel thermal noise coefficient, $k$ is Boltzmann constant and $T$ is the temperature in Kelvin. To estimate the input referred noise of the CTLE, equation (10) is divided by the CTLE transfer function written in equation (1) and integrated as shown below:

$$\overline{V_{n,in}^2} = \sqrt{\int \frac{\overline{V_{n,out}^2}}{H(s)^2} ds} \tag{11}$$

A plot of integrated input noise voltage as a function of $g_{m1}$ is shown in Fig. 5(a). Assuming similar design specifications as used in the example in Sub Section II-B, input referred integrated noise of the CTLE designed to meet the specs is plotted vs $g_{m1}$ (Fig. 5(a)). It can be observed that the input referred noise decreases as the $g_{m1}$ increases, which corresponds to an increase in the CTLE power.

Point-by-point multiplication of input referred integrated noise of CTLE and $g_{m1}$+$g_{m2}$ was done to find the noise power product, as shown in Fig. 5(b). Because the total power increases faster than input referred noise decreases, the product

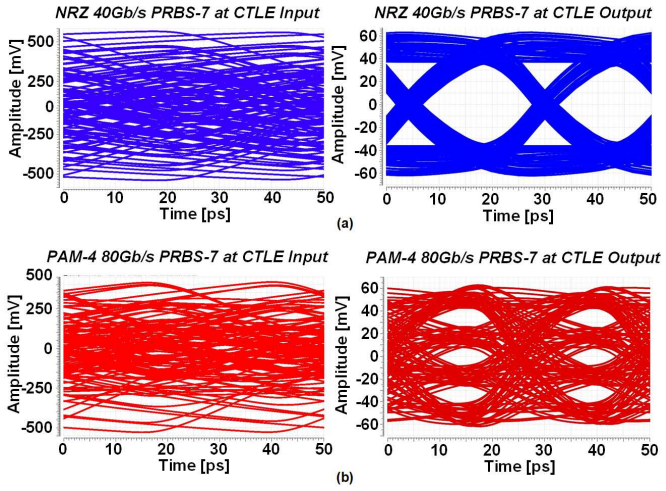


Fig. 6. (a) Simulated eye diagrams of 40Gb/s NRZ data after 15dB channel loss @20GHz and after CTLE. (b) Simulated eye diagrams of 80Gb/s PAM-4 data after 14dB channel loss at @20GHz and after CTLE.

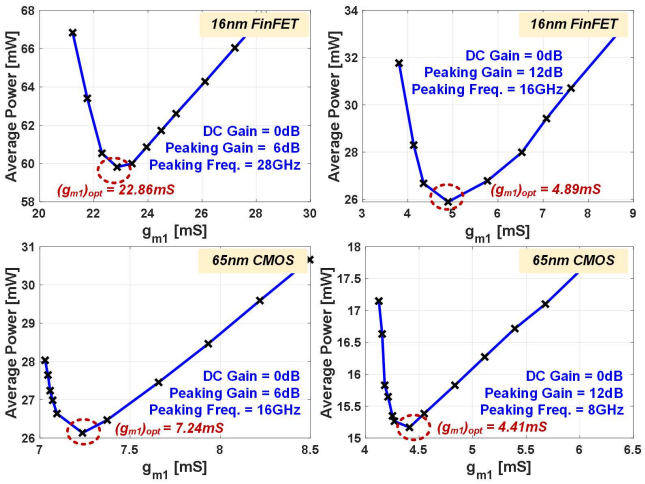


Fig. 7. Simulated power consumption vs $g_{m1}$ of CTLE designed in 16nm FinFET and 65nm CMOS meeting four design constraints.

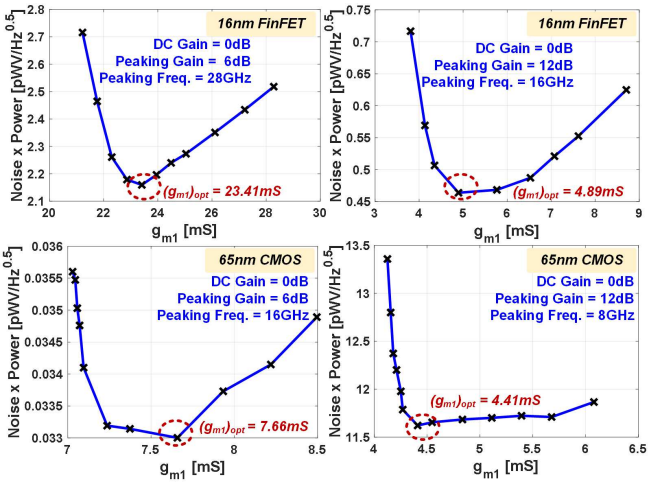


Fig. 8. Simulated noise power product vs $g_{m1}$ of CTLE designed in 16nm FinFET and 65nm CMOS meeting four design constraints.

of noise and power is largely dominated by power. It can be observed that the noise power product reaches its lowest point closer to the optimal $g_{m1}$ and again increases for the higher values of $g_{m1}$. Since several CTLE design tries to balance both the noise and power, designing the CTLE at minimum noise power product point is an efficient design strategy.

## IV. Simulation Results

Energy efficient design of CTLE at the minimum power point is verified by designing and simulating CTLE in two different technology nodes: 16nm FinFET and 65nm CMOS. The verification was done by designing CTLE with four different design specification constraints of DC gain, peak gain, and peaking frequency (a) 0dB, 6dB, and 28GHz, (b) 0dB, 12dB, and 16GHz, (c) 0dB, 6dB, and 16GHz and (d) 0dB, 12dB, and 8GHz, respectively.

The CTLE is designed in Cadence with 16nm FinFET to demonstrate equalization of the channel and open the closed eye. Two transient simulations were performed with 40Gb/s PRBS-7 NRZ data at 15dB channel loss at Nyquist and 80Gb/s PRBS-7 PAM-4 data at 14 dB channel loss at Nyquist. Fig 6 (a) shows the 40Gb/s NRZ eye diagram at channel far-end and at CTLE output. Vertical and horizontal eye opening at the CTLE output is 60 mV and 20 ps, respectively. Fig 6 (b) shows the 80Gb/s PAM-4 eye diagram at channel far-end and at CTLE output. Minimum vertical and horizontal eye opening at the CTLE output is 15 mV and 9 ps, respectively.

To demonstrate the existence of minimum power point, CTLE is designed and simulated in Cadence while meeting four different design constraints in 16nm finFET and 65nm CMOS. A plot of CTLE power versus $g_{m1}$ is shown in Fig. 7. It is to be noted that the design constraints of the CTLE were met at all the points in the plot by calibrating the transistor widths, $R_L$, and $C_Z$. It can be observed that for each of these design constraints, there exists an optimal $g_{m1}$, $g_{m2}$, $R_L$ and $C_Z$, which results in minimum power consumption. Simulated input referred noise power product of the inverter based CTLE for the same four design constrains is shown in Fig. 8. It can be observed that the CTLE achieves minimum noise power product at similar or closer to the optimal values of the $g_{m1}$.

## V. Conclusion

This paper presented a design approach to design the inverter based CTLE with the minimum power consumption and at minimum noise power product point while meeting the desired specifications. Mathematical close form expressions of the CTLE parameters are derived. Design and simulation of CTLE to demonstrate the minimum power point was done in 16nm FinFET and in 65nm CMOS technology nodes.

## VI. Acknowledgment

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