VSAGE: An End-to-End Automated VCO-Based ΔΣ ADC Generator

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***Abstract*— This article presents VSAGE, an agile end-to-end automated voltage-controlled oscillator (VCO)-based ΔΣ analog-to-digital converter (ADC) generator. It exploits time-domain architectures and design mindset, so that the design flow is highly oriented around digital standard cells in contrast to the transistor-level-focused approach in conventional analog design. Through this, it speeds up and simplifies both the synthesis phase and layout phase. Combined with an efficient knowledge-machine learning (ML)-guided synthesis flow, it can translate input specifications to a full system layout with reliable performance within minutes. This work also features a compact oscillator and system modeling method that facilitates light-resource accurate computation and network training. The generator is verified with 12 design cases in 65-nm and 28-nm processes, proving its capability of generating competitive design with good process portability.**

***Index Terms*— ΔΣ modulator (DSM), analog-to-digital converter (ADC), circuit generator, voltage-controlled oscillator (VCO).**

I. Introduction

ANALOG mixed-signal (AMS) integrated circuit design automation (DA) is in rapidly growing demand in the face of a blooming sensing application market, workforce shortage, and increasing productivity imbalance between analog and digital design in advanced processes. From a methodological perspective, existing AMS DA tools can be roughly categorized into two branches. The first branch follows a circuit-agnostic approach, where the tools are formulated as a black-box optimization problem and often employ machine learning (ML) techniques. State-of-the-art examples include Wang et al. [1], Lyu et al. [2], and Li and Carusone [3], who exploit reinforcement learning and Bayesian optimization for transistor-level sizing. For analog layout automation, MAGICAL [4] and ALIGN [5] enable fully automated layout generation capability through a combination of graphical neural networks and optimization algorithms. Nonetheless, these generic tools do not scale well with circuit size due to their black-boxed nature. While being highly effective for handling smaller pure analog topologies like operational amplifiers (OPAMPs) or voltage regulators, they lose efficiency and reliability quickly for designing larger-scale AMS subsystems, such as analog-to-digital converters (ADCs) and phase-locked loops (PLLs). To that end, the second branch of the AMS DA tool follows the mindset of circuit-algorithm co-design, where the tools are designed as a circuit-specific script-based generator. By trading the versatility, they become capable of end-to-end automation, i.e., producing tape-out-ready layouts from top-level specifications, even for complex AMS subsystems. So far, a variety of end-to-end generated AMS subsystems covering but not limited to PLLs, low-dropout regulators (LDOs), temperature sensors and ADCs have been reported by Berkeley analog generator (BAG) [6], Krishna Chekuri et al. [7], FASoC [8], TAFA [9], and OpenSAR [10]. While these automated tools are not yet perfect, they show great promise in accelerating the design process, making them increasingly valuable in meeting industry demands for faster time-to-market without compromising reliability. Certain circuit generator approaches [6], [8] have been adopted by IP companies such as Blue Cheetah [11] and Movellus [12]. In contrast to circuits and techniques presented at solid-state circuit conferences, which aim to push for better performance of circuits through meticulous manual design, circuit generators prioritize streamlining the design process, making it more agile and time-efficient. Relying on mature architectures and adapting based on the number of similar blocks, circuit generators primarily reduce labor-intensive manual work, and the reliability of automated circuits should not differ significantly from that of manual designs.

Among various AMS subsystems, ADCs are deemed one of the most challenging and time-consuming to design owing to their analog-intensive nature and tough accuracy requirements. To balance the energy efficiency and complexity tradeoff, ADCs adopt different architectures for different application targets. For instance, the successive-approximation-register (SAR) ADC is often picked for medium-resolution (e.g., 6–11 bits) applications, while the ΔΣ ADC is widely chosen for high-resolution (e.g., >12 bit) designs. The vast majority of existing *end-to-end* ADC generators are all tailored to the SAR ADC [10], [13], [14], [15], [16]. While SAR ADCs meet the needs of a wide range of current IoT applications, the growing demand for higher precision sensing modalities has positioned ΔΣ ADCs as a key component in many systems. Consequently, the development of ΔΣ ADC generators has become increasingly important. However, this task is nontrivial, as ΔΣ ADCs require a distinct design

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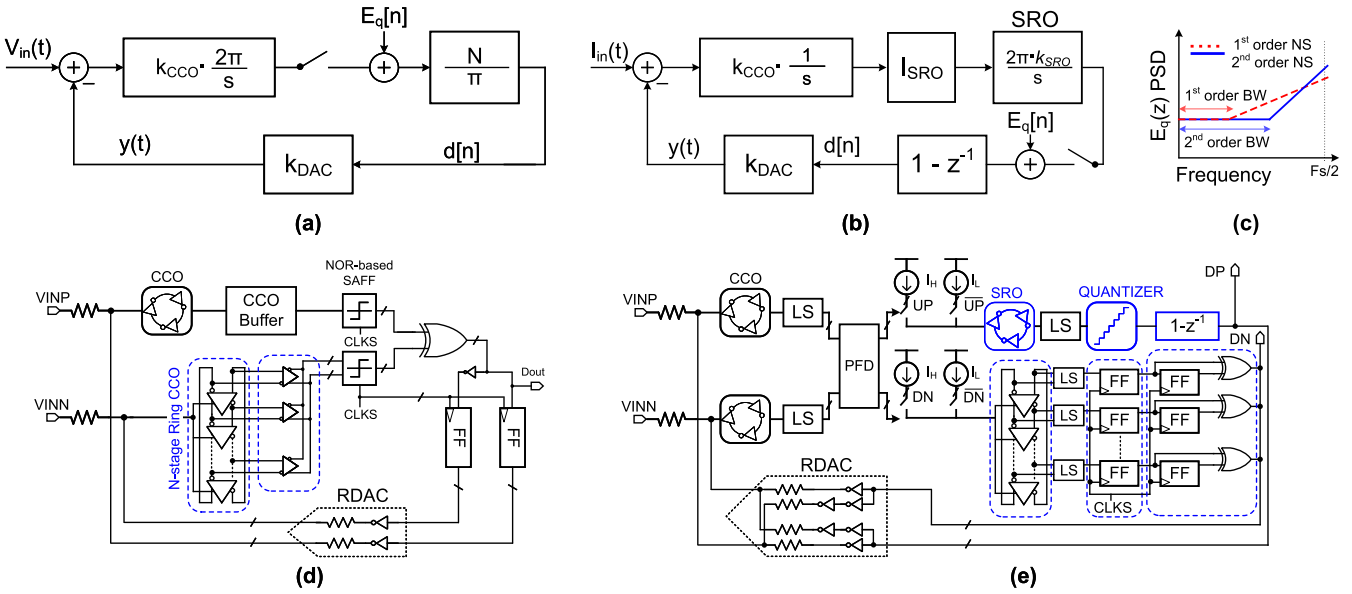

Fig. 1. Abstracted signal flow of (a) first- and (b) second-order $\Delta\Sigma$ ADC with noise-shaping effect comparison in (c). Circuit diagram of the target (d) first- and (e) second-order VCO-based $\Delta\Sigma$ ADC.

methodology that differs significantly from that of SAR ADCs, rendering SAR generators unsuitable for reuse. To the best of our knowledge, efforts in $\Delta\Sigma$ ADC DA have primarily focused on high-level coefficient synthesis or layout (e.g., MAGICAL [17]), and no coherent *end-to-end* flow has been fruitful to date.

This article presents VSAGE: an agile, fully automated, specification-to-GDS VCO-based $\Delta\Sigma$ ADC generator. To the best of our knowledge, this is the first automated generator of its kind. Instead of relying on traditional voltage-domain $\Delta\Sigma$ ADCs, the proposed generator focuses on time-domain VCO-based $\Delta\Sigma$ ADCs. This approach is motivated by the increasing relevance of time-domain circuits in advanced process nodes, where low voltage headroom and reduced transistor gain make designing voltage amplifiers and precision comparators more challenging, while time-based designs become more practical. Automating the design of VCO-based ADCs enhances flexibility for integration and deployment in modern systems, including CPU monitoring functions (e.g., temperature and voltage), SoCs, AI accelerators, and compute-in-memory architectures.

The proposed generator highlights the following key features.

1) The entire design is constructed into a digital-like structure. This allows the generator to work on the digital standard-cell level and seamlessly integrate into digital place-and-route (P&R), which significantly speeds up and simplifies both the design and layout.
2) We propose a hybrid knowledge-ML-guided synthesis flow to obtain key circuit parameters quickly and accurately. The knowledge flow provides reliable initial conditions for the ML optimization process. The hybrid flow facilitates simpler modeling in both the knowledge and ML phases compared when using either alone.
3) An efficient oscillator and system surrogate modeling method is developed. It only requires a one-time model-building process, after which the resource-heavy SPICE model can be obviated.
4) We develop an automated layout template, which can automatically adjust the floor plan for the layout according to the generated design.
5) The framework can generate a design with bandwidth (BW) ranging from 10 kHz to 10 MHz, and SNDR to near 75 dB, which can cover most general-purpose applications including biomedical usage.

With these innovations, the VSAGE framework performs full ADC generations within minutes, and can be easily transferred between processes without any need for circuit redesign, with consistent and even better performance as the process scales down. This is verified with 12 ADCs generated with different specifications and processes. This work is made available as an **open-source**[1] framework, allowing for wider accessibility and contribution from the research community.

II. Circuit Architecture

This section introduces the basics of the underlying ADC architecture of VSAGE. On the high level, a $\Delta\Sigma$ ADC can be viewed as a quantizer placed in a filter loop, as shown in Fig. 1(a) and (b). It is an oversampled system, meaning that the BW of interests is much less than the Nyquist frequency (i.e., $F_s/2$). The quantization error $E_q[n]$ is high-pass shaped due to the dynamic of the negative feedback filter loop, which brings considerable noise suppression within the BW of interest, making them a strong candidate for high-resolution applications. The noise-shaping effect enhances with higher filter order (the number of integrators) [see Fig. 1(c)]. In short, a higher order design facilitates less oversampling overhead, at the cost of larger power and area. In the VCO-based ADC, the VCO assumes the role of the filter through its frequency-to-phase integration nature. This mechanism can be realized

[1]https://github.com/Califer1221/VSAGE

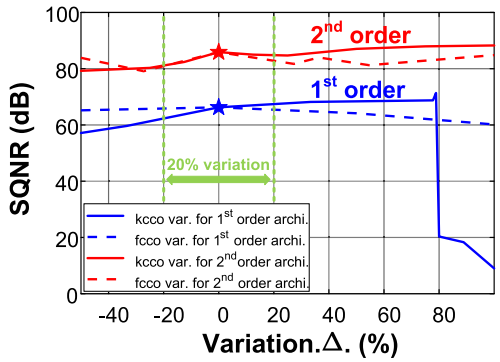

Fig. 2. Stability simulation of SQNR under k_{cco} and f_{cco} variation for 1st-order architecture and second-order architecture.

by mostly digital structures, leading to better performance with advanced processes than conventional voltage-based filters.

The circuit schematics of the first-order and second-order VCO-based ADCs are shown in Fig. 1(d) and (e), which are mainly based on [18] and [19]. RDACs are used in both architectures to enhance synthesis compatibility. In this work, the VCOs are realized in the form of current-controlled oscillators (CCOs), which do not alter the operation principle but can provide better linearity to the integration. Essentially, each CCO pair plays the role of the integrator block ($2\pi k_{CCO}/s$). The outputs of the CCO will be processed by fully digital phase detectors, turning the integration result directly into digital code without the need for comparators. Feedback digital-to-analog converters (DACs) are implemented simply as inverter-driven resistors. Both architectures are highly insensitive to mismatch in feedback DAC, thanks to an intrinsic element rotating mechanism provided by the CCOs. Although the CCO tuning gain (i.e., k_{cco}) and free-running frequency (i.e., f_{cco}) are prone to process–temperature–voltage (PVT) variation, the chosen architecture can tolerate large variation with negligible degradation in performance. As shown in Fig. 2, both architectures are insensitive to f_{cco} and they can work in a large variation of k_{cco}. In addition, a few tuning current entry points can also be prepared to provide extra fail-safe in the generated circuit. The entire structure can be expressed in Verilog code thanks to the highly digital construction. This provides a robust circuit-level foundation for the proposed VSAGE framework.

III. ADC Generator and Methodology

A. Framework Overview

The workflow of VSAGE is shown in Fig. 3. The framework consists of a one-time setup and the main generation flow. The purposes of the one-time setup are for 1) augmenting the standard cell library with a few simple custom additions such as resistor and level shifter; 2) creating the CCO surrogate model used in the knowledge-based synthesis step; and 3) training an artificial neural network (ANN) model used in the NN-assisted gradient-decent (GD) optimization process. More details of the one-time steps will also be discussed in Sections III-C and III-D, respectively. The main generation

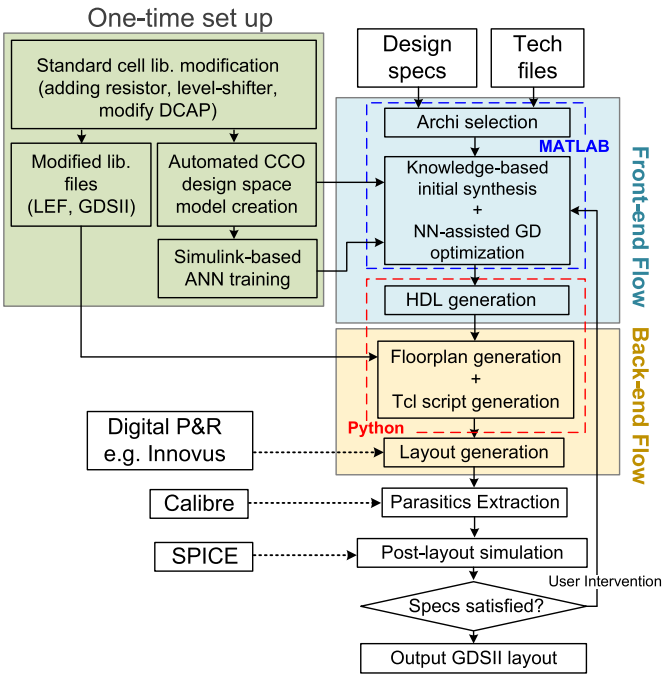

Fig. 3. High-level workflow diagram of the VSAGE framework.

flow requires minimal designer inputs with only design specifications and technology files. The input specifications include sampling frequency (F_s), BW of the signal, maximum input amplitude, and signal-to-distortion-noise ratio (SNDR). The flow will then select the most suitable architecture and proliferate the building block parameters through the hybrid knowledge-ML-guided process. For the current version, first-order and second-order architectures are supported. The generated design will then be described as a gate-level Verilog and passed to the digital P&R engine for layout.

The back-end flow consists of two key steps. The first part is a floorplanner that will create the coordinates and block sizes dynamically according to the circuit, and create a Tcl script that commands digital P&R tools like Cadence Innovus. This step is wrapped in Python code. The second step generates the entire system layout in a standard digital P&R tool.

The entire VSAGE flow can be fully connected and requires only a single command to kickoff. A user intervention mechanism is provided for designers to overwrite the auto-design results for flexibility. In most cases, no iteration is needed to meet the requirement thanks to our robust architecture.

B. Hybrid Knowledge-ML-Guided Synthesis Flow

We first discuss the VSAGE front-end flow, where key design parameters are synthesized from the input specifications. Equation-based analysis used in manual design practices is usually considered unoptimized, whereas the black-box optimization approach adopted by most automated AMS synthesis suffers from long runtime and reliability concern [13]. In VSAGE, we propose a hybrid knowledge-ML-guided synthesize flow to achieve the sweet spot of fast runtime and high-quality-of-results. It starts with

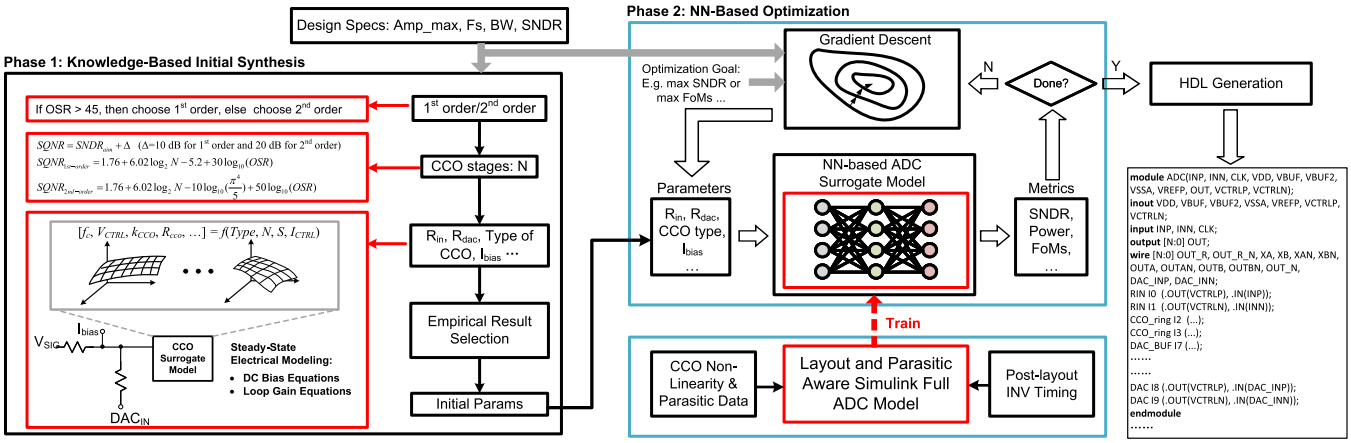

Fig. 4. Translating from ADC specifications to block parameters using the hybrid knowledge-ML flow, i.e., the front-end flow.

a knowledge-based phase, where designer heuristics and mathematical analysis are utilized to obtain the initial parameters, then followed by an NN-assisted GD optimization process for the final parameter search. The overall front-end translation flow is outlined in Fig. 4.

1) Knowledge-Guided Phase: The knowledge-guided phase (**phase 1** in Fig. 4) begins with architecture (loop order) selection and determining the number of CCO stages (N), which determine the upper bound of SQNR of the ADC. These two steps are rule-based following common designer practices, as outlined in the left of Fig. 4. After the architecture and N are determined, the third step generates the rest of the analog-related parameters, including those of the input resistor, feedback DAC, and the CCO, in a holistic manner by analyzing a steady-state electrical model formed by the CCO and its input networks. We highlight the use of a hybrid "top-down + bottom-up" approach in this step, where the bottom-up part is applied to CCO modeling. In the one-time setup, we have simulated different samples of predesigned CCOs that, when given a specific current, output their oscillation frequency and voltage. Based on these data, we can use interpolation functions to construct a surrogate model for the CCO design space as the following:

$$\left[f_c, V_{\text{ctrl}}, k_{\text{cco}}, R_{\text{cco}}\right] = f(\text{Type}, N, S, I_{\text{ctrl}}) \tag{1}$$

where Type reflects the size and load of the CCO unit, S is the number of units per delay stage (S CCO units form a delay stage and N delay stages form a CCO), I_{ctrl} is the current flowing into the CCO. These are inputs of the VCO surrogate model. The oscillation frequency f_c, CCO control node voltage V_{ctrl}, frequency tuning gain k_{cco}, and control node equivalent resistance R_{cco} are the metric outputs of the surrogate model. This approach shares a similar mindset with the widely adopted "G_m/I_D" methodology [20] used in analog transistor sizing, where electrical analysis is performed using precharacterized data charts of the device instead of closed-form equations. In our method, the idea is generalized to block-level design. It can synthesize parameters that provide almost the desired performance "out-of-the-box."

When the ADC is operating at a steady state, the input resistor (R_{in}), equivalent DAC resistance (R_{dac}), and the CCO forms an equivalent RC network as shown in Fig. 5. For all key property that matters, the CCO can be treated as a nonlinear resistor whose I/V characteristics can be looked up through the surrogate model. Assume this is an N-stage CCO. R_{dac} is the lump resistance for the entire resistor DAC (RDAC), consisting of N paralleled unit resistors R_u. Thus, $R_u = R_{\text{dac}} \cdot N$.

The key design equations describe the desired conditions where the VCO-based ADC should achieve for both large-signal (or direct-current, dc) and small-signal (SS) behavior. For the large-signal part, we can assume the input on average will stay around the middle of the ADC full scale. We can treat $((N-1)/2)$ of the resistors in RDAC will be connected to V_{DD}, and others will be connected to GND, giving $V_{\text{dac}} = (V_{\text{DD}}/2)$. This gives us two large-signal-related equations. The first one is about the dc current flowing into CCO I_{ctrl}. Based on Kirchhoff's Current Law (KCL), it can be expressed as

$$I_{\text{ctrl}} = \frac{\frac{V}{R_{\text{in}}} + \frac{\frac{N-1}{2}\cdot V_{\text{DD}}}{R_u} + I_{\text{bias}}}{1 + \frac{V_{\text{ctrl}}}{I_{\text{ctrl}}\cdot R_{\text{in}}} + \frac{V_{\text{ctrl}}\cdot N}{I_{\text{ctrl}}\cdot R_u}}. \tag{2}$$

The second equation describes the maximum input amplitude with respect to resistance and power supply

$$\text{Amp\_max} = \frac{R_{\text{in}}}{R_{\text{dac}}} \cdot \frac{V_{\text{DD}}}{2}. \tag{3}$$

In terms of small-signal behavior, the design equation stems from the requirement that the aggregated small-signal loop gain coefficient (LG) should be around 1 to achieve good stability

$$\text{LG} = \frac{4N \cdot k_{\text{dac}} \cdot k_{\text{cco}}}{f_s} = 1 \tag{4}$$

where k_{dac} is the small-signal current division ratio from the DAC to the CCO, indicating the change in current I_{ctrl} when one bit of RDAC shifts from VDD to GND

$$k_{\text{dac}} = \frac{\frac{V_{\text{DD}}}{R_u}}{1 + \frac{R_{\text{CCO}}}{R_{\text{in}}} + \frac{R_{\text{CCO}}\cdot N}{R_u}} \tag{5}$$

where R_{CCO} is the small-signal resistance of the CCO's control input, which can be obtained from the derivative of CCO's I/V surrogate data.

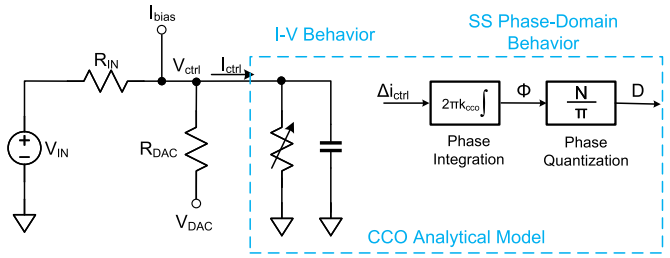

Fig. 5. Analog electrical model of the first-order architecture.

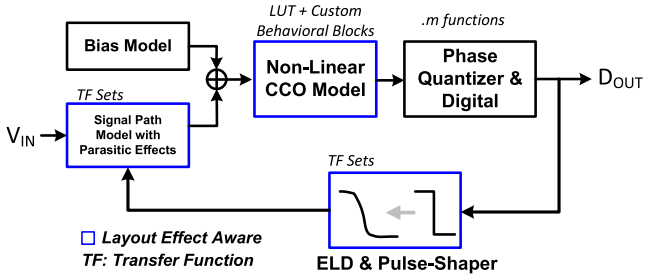

Fig. 6. Layout-aware Simulink model for a first-order ADC.

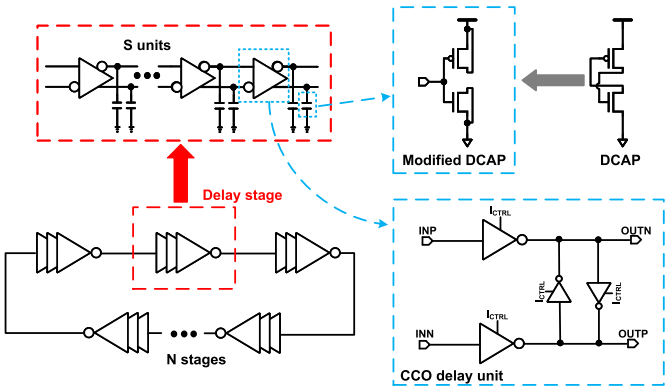

Fig. 7. Implementation of the ring CCO.

Based on (1)–(5), there are five equations to address four key parameters: R_{dac}, R_{in}, CCO type, and I_{bias}, allowing for multiple possible solutions. The script begins by selecting a suitable CCO type and an initial S value (where S delay units make up a single delay stage), then sweeps through I_{ctrl}. As I_{ctrl} varies, the CCO characteristics—such as f_{cco}, V_{ctrl}, k_{cco}, and R_{cco}, defined by (1)—also change. Equations (2)–(5) govern the correct DSM operation. The synthesis process seeks the optimal CCO type and bias point in the design space [as per (1)] to validate the parameters across (2)–(5). Note that (1) is not a closed-form expression but rather a numerical lookup table representing the CCO design space. In other words, due to the high dimensionality of the surrogate model for the CCO, this process may yield multiple solutions for the feasible CCO sizing options. We add designer insight to exclude the unfeasible solutions such as negative R or overly large R to make the resistance and current in a feasible range. We implement this as a priority option in the script. There are three types of priority: area priority will select the one with the smallest resistance, power priority will choose the solution with the smallest current, and economic type will choose the solution with moderate resistance and current.

Note that the analytical approach outlined above focuses on the behavior of one CCO and the main feedback node. It can fully determine the parameters of the first-order architecture. For the second-order architecture, the approach is similar but needs to be slightly adjusted to account for the modeling of the second oscillator. The second oscillator is a switched ring oscillator (SRO), which works as a noise-shaping phase-to-digital converter that digitizes the first CCOs' phase difference and provides order boosting [19]. The main change needed is in the loop gain equation. For second-order, it becomes

$$\mathrm{LG}_2 = \frac{2 \cdot 2\pi \cdot k_{cco} \cdot k_{sro} \cdot k_{dac}}{f_s} = 1 \tag{6}$$

where k_{sro2} is the phase-to-digital gain of the SRO. It needs to satisfy

$$k_{sro} = \frac{N}{2\pi}. \tag{7}$$

With these adjustments, the second-order design parameters can be synthesized holistically similar to the first-order case.

2) NN-Based Optimization Phase: The initial synthesized parameters from the knowledge-based phase are then passed to the next phase, which leverages an NN-assisted GD process to fine-tune the synthesized design parameters (**phase 2** in Fig. 3). The ANN used in this process is a surrogate model that represents the parameter-to-metric function of the full ADC. It assumes the role of the circuit evaluator without the heavy overhead of SPICE simulation, allowing the optimization to be done rapidly. In previous practices, such ANNs are trained by an enormous set of full-transistor-level SPICE simulation data [9], which is costly to obtain and not friendly to process migration. In VSAGE, the ANN is trained using a carefully designed layout-and-parasitic-aware Simulink model, which can closely approximate the postlayout SPICE simulation result of the ADC but consumes much lighter resources. This is made possible as the most critical postlayout nonidealities in the target ADCs are only associated with the analog behavior in the CCOs and feedback DACs, and they can be captured with transfer function (TF) sets and precharacterized *postlayout* CCO/standard cell data from the one-time setup. Other unnecessary transient data such as digital signals can be idealized with negligible impact on the simulation accuracy, enabling significant speedup. Fig. 6 illustrates the setup of the Simulink model used for NN training. The CCO is represented as a nonlinear resistor whose resistance, derived from an interpolation function, changes dynamically in response to varying input currents to the CCO. The relationship between the input current and fcco is also nonlinear and is based on interpolation functions generated from a look-up table (LUT) of data simulated using OCEAN scripts in Cadence. These LUT data are obtained from postlayout simulations of standard cells. In addition, the mismatch in the DAC is another factor that can degrade the ADC's performance, and we have accounted for this by modeling the DAC with the mismatch in our Simulink setup. A critical factor in continuous-time delta-sigma modulators (CTDSMs) is the extra loop delay (ELD)

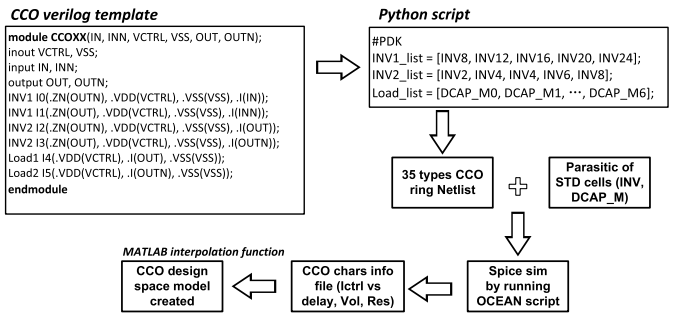

Fig. 8. CCO design space model creation.

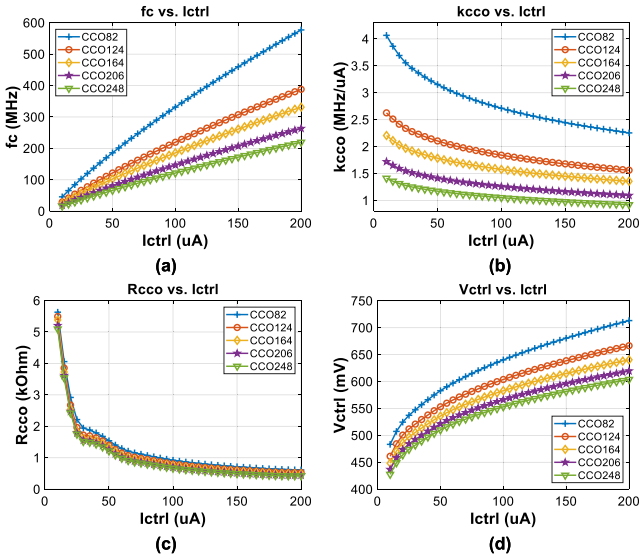

Fig. 9. Part of the CCO surrogate model: characterized metrics for all CCO types under "no-load" conditions, with $N = 15$, and $S = 1$. (a) f_c, (b) k_{cco}, (c) R_{cco}, and (d) V_{ctrl} vs. I_{ctrl}.

caused by the finite DAC transition time, which introduces a pole and can slightly affect performance. In Simulink, we model ELD as a low-pass filter (LPF) within the loop's TF. The LPF resistance is based on earlier parameters, while parasitic capacitance is estimated from the CCO stages and size. For first- and second-order architectures, this enhances the accuracy of our Simulink results. It is worthwhile to mention that, since the trained ANN model captures the high-order dynamic effects of the circuit such as CCO parasitic poles, finite DAC transition slopes, and ELD, the knowledge-based flow can ignore these effects during initial synthesis, thus greatly simplifying the electrical model. Meanwhile, using the knowledge-based results as the starting point for the GD process, the training accuracy of the ANN can be relaxed as the high fluctuation boundary regions of the design space (which contribute the most errors) are inherently avoided. In other words, the knowledge-ML phases facilitate each other reciprocally.

With the analog blocks designed, the rest of the circuits, which process bi-level time-domain or digital signals, can be designed based on simple timing requirements and sized based on sampling frequency. At this point, the schematic-level design is complete. The design is then exported as gate-level HDL form and is ready for layout in digital P&R tools. Layout discussion follows in Section III-E.

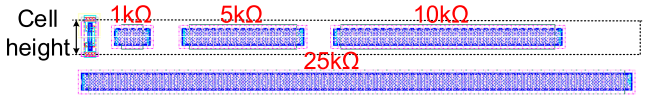

Fig. 10. Customized resistor cells compared to a standard cell.

C. CCO Design Space Characterization and Surrogate Model Creation

This section discusses the key one-time setup procedure: CCO surrogate model creation and relevant design considerations. As shown in the bottom right of Fig. 7, the CCO delay unit adopts a pseudo-differential supply-driven design with four cross-coupled inverters [21] and loading capacitors (C_L). The pseudo-differential structure has lower noise and can facilitate robust level-shifting compared to a single-ended inverter ring. The size ratio of the main inverter to the coupled inverter is set to 4:1. C_Ls are implemented from minor modification of DCAP cell of the standard cells, which are originally used only for power line decoupling, as shown in the top right of Fig. 7. The modification is trivial as only 3 metal wires need to change. The modified DCAP can work effectively for any voltage.

The behavior of the CCO is governed by four factors: the number of stages N, the delay unit size, the unit loading, and the number of units per delay stage S (Fig. 7). Since N is predetermined, the latter three are the optimizable design variables in our flow. The size affects all f_c, k_{cco}, V_{cco}, and R_{cco}, whereas loading and S affects only the first two metrics. Despite overlapping effects, using all three factors as design parameters allows us to have a larger design space to balance tradeoffs. The VSAGE framework provides five different CCO unit size options using different 4:1 inverter pairs available in the standard cell library (e.g., CCO82 means using INVX8 and INVX2). There are seven options for loading, including a "no-load" condition. In total, 35 design "Types" can be chosen for each delay unit. The unit number per stage (S) affects f_c and k_{cco} linearly. Thus, we can simply characterize the 35 unit types in the initial setup with a constant S.

The steps of creating the CCO surrogate model are shown in Fig. 8, a Verilog template for the CCO is used as the basis for our design. The process begins by specifying the PDK name of the inverters and modifying DCAPs in a Python script. This script then utilizes the CCO template to automatically generate 35 distinct netlist variations of the CCO ring, each composed of 15 CCO units. Following netlist generation, parasitics are extracted from the standard cells used within the CCO model. The next step involves running SPICE simulations using a preconfigured OCEAN script. The simulation results, including key CCO characteristics, are written to output files. These files are subsequently processed by a MATLAB script, which produces interpolation functions, forming the surrogate model of the CCO design space. Fig. 9 shows a snapshot of the surrogate model under no load, $N = 15$ and $S = 1$ in a 65-nm process. The complete surrogate model is a high-dimensional surface with different loads, N and S. Thus, by changing those parameters, a wide range of center frequency and k_{cco} can be selected. This will ensure our generator generates VCO-based ADC in a wide range.

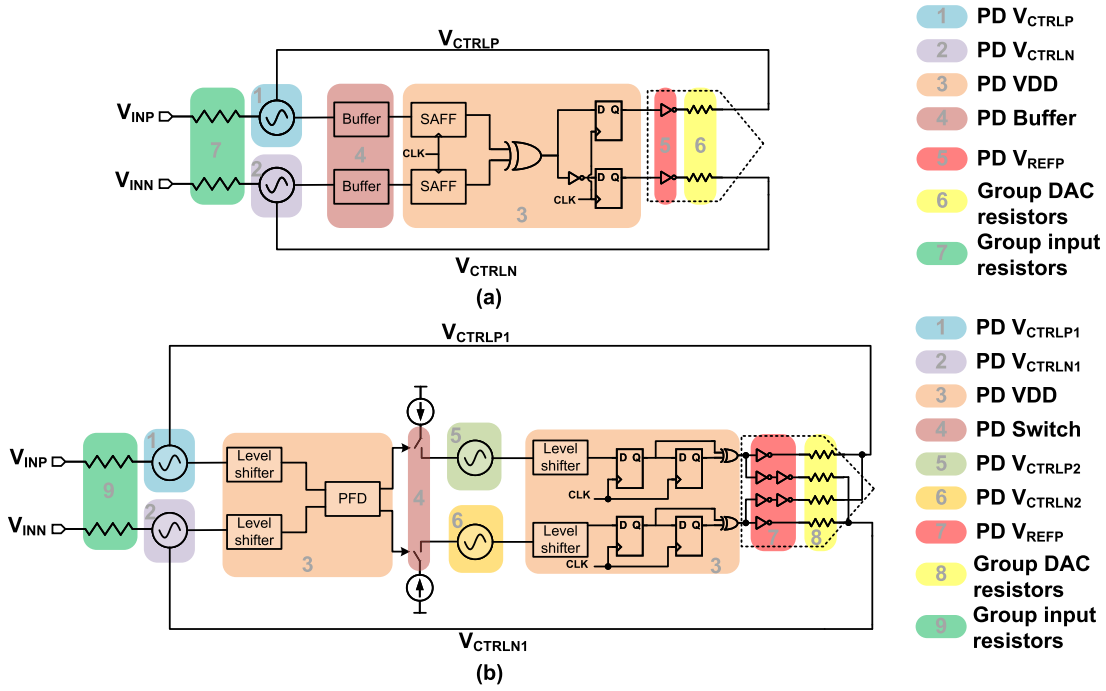

Fig. 11. Decomposed into different power domains and floorplan groups of (a) first-order ADC. (b) second-order ADC.

D. Other Components and Standard Cell Augmentation

In addition to CCO modeling and ANN training, one last step in the one-time setup is to create the technology file with customized standard cells. The proposed design only requires a limited number of custom cells. Since the output voltage of CCO is dependent on the CCO type, working condition, and process we chose, the voltage high will range from 0.3 to 0.8 V, which cannot be detected for digital circuits directly. Thus, level shifters or sense amplifier flip-flops (SAFFs) are needed to transfer the voltage to rail-to-rail voltage. For the first-order circuit, three-input NOR gates-based SAFF is adopted [18]. Since it directly uses digital cells, it can be constructed from native standard cell components. For the second-order design, level shifters are required due to the architecture being incompatible with SAFF. The level shifter employs the design from [22]. The structure is simple and can be easily added to the standard cell library.

Another part that employs custom cells is the RDAC. Four different value resistors are generated (1, 5, 10, and 25 kΩ). They can be combined to form any desired resistance. The resistors are generated by using a poly layer in the technology process library, which only uses M1 for metal and is very similar to other standard cells. Fig. 10 gives four layouts of customized resistors standard cells. All custom cells are designed to have the same height as standard cells. After designing the layout of these augmented cells, we generate a LEF file and merge it with the original LEF file.

E. Layout Generation

The layout of the VSAGE framework is completely performed through standard digital P&R engines (e.g., Cadence Innovus and Synopsys IC Complier) without the need for a separate AMS layout tool. To facilitate the need for multiple supply voltage (MSV), as well as a more organized floorplan, and minimize postlayout degradation, the layout is performed in a hierarchical way based on power domain partitioning. Fig. 11 shows the power domains of the first-order ADC and second-order ADC separately. This is executed through the MSVs design functionality available for most digital P&R tools.

When the top-level design changes, the traditional digital back-end flow will take much time to resetup floorplanning, power planning, standard cell placement, and routing. This is mainly because a changed design will induce different floorplanning. In our design flow, this is taken care of automatically through a dynamic floorplanner in the back-end flow. As is shown in Fig. 12, the back-end Python script consists of two parts. The first part will determine the actual size and coordinates of each block based on the HDL and power-domain plan using a predetermined relative floorplan template. Floorplanning can be parameterized. As is shown in Fig. 12, after block parameters are settled, the areas of each block can be calculated based on the number of cells used in each block. In the script, we set the width height ratio and placement density, so the shape of each block can be obtained. Though the block sizes vary in different designs, the relative locations between blocks are fixed based on symmetry rules. Thus, plus the shape of each block, the coordinate of each block can be obtained fast in the script. Based on the coordinates of each block, the second part of the Python script will output a full Tcl command script with customized floorplanning, power planning, and other necessary steps to complete the full layout. The generated Tcl script is ready to run in the Innovus and will output the DRC and LVS clean layout in minutes. Note that additional cells, such as modified DCAP, resistor, and level-shifter,

TABLE I
PERFORMANCE SUMMARY OF 12 DESIGN CASES

Case	Specifications				Generated results				
	Fs [MHz]	BW [MHz]	SNDR [dB]	Process [nm]	Architecture selection	SNDR [dB]	Power [mW]	Area [mm^2]	FoMs [dB]
1	1	0.01	60	65	1st order	61.6	0.013	0.198	150.4
2	100	0.74	71	65	1st order	72.8	0.207	0.057	168.3
3	200	1.5	65	65	1st order	68.0	0.434	0.019	163.3
4	250	2.0	60	65	1st order	62.4	0.305	0.016	160.6
5	400	3	71	65	1st order	70.7	1.089	0.044	165.0
6	200	1.5	74	28	1st order	74.7	0.602	0.049	168.7
7	400	3	74	28	1st order	74.6	0.494	0.016	172.4
8	100	1.25	70	65	2nd order	68.9	0.52	0.053	162.7
9	200	2.5	71	65	2nd order	71.1	0.885	0.028	165.6
10	200	2.5	71	28	2nd order	72.1	0.331	0.042	170.9
11	400	5	71	28	2nd order	72.2	0.674	0.022	170.9
12	800	10	62	28	2nd order	62.5	1.157	0.018	161.9

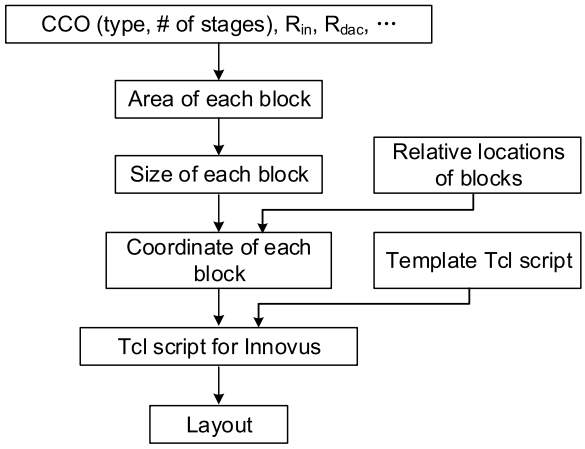

Fig. 12. Translating from block parameters to layout generation.

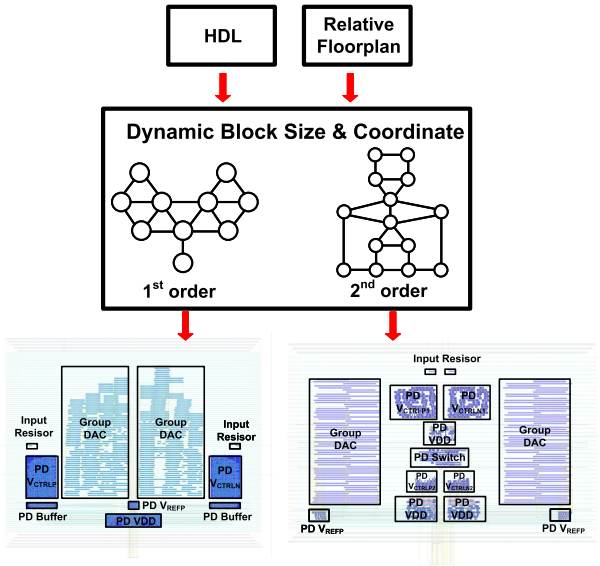

Fig. 13. Example of (a) first- and (b) second-order ADC layout generated by script.

operate in continuous time. As a result, these modules do not require time constraints. Notably, unlike digital circuits that operate with a fixed supply voltage and primarily focus on delay, the CCO is concerned with its f_{cco} and k_{cco}. The CCO operates under varying currents, which lead to different oscillation frequencies. However, it appears that there could be timing concerns at the interface of the CCO and the phase sampling DFFs since the time of the CCO transition and the sampling clock are unknown. However, the set-up and hold-time violation at the sampling DFFs does not cause the failure of the operation. The reason is because the phase quantization scheme we use is the multiphase scheme. An error in the DFF will only cause one LSB difference and the effect is very mild.

Fig. 13 illustrates the first-order and second-order layout generation process according to the relative locations of each block, respectively. The pad ring is not included in the framework because the focus is specifically on the generation of the Delta-Sigma ADC core for general-purpose applications. In this context, the ADC is more likely to be integrated as part of a larger SoC rather than being implemented as a standalone ADC chip. For the power rail design, we utilize a power domain partitioning approach. The ground is managed at the top level, with all horizontal Metal 1 layers globally dedicated to the ground rail. Each floorplan group, defined by its respective power domain, is surrounded by a power ring to establish isolation and efficient power distribution. Within each power ring, we use horizontal Metal 1 for the power rail, ensuring localized power delivery to each domain. This arrangement enables an even distribution of voltage and current across all power domains, helping to minimize IR drop and improve overall stability and performance. The back-end layout generation flow is process-independent since the names and sizes of standard cells are also parameterized.

IV. SIMULATION RESULTS

The VSAGE framework is verified under 65-nm and 28-nm CMOS processes over 12 design cases as shown in Table I. The one-time setup (excluding ANN model training) takes

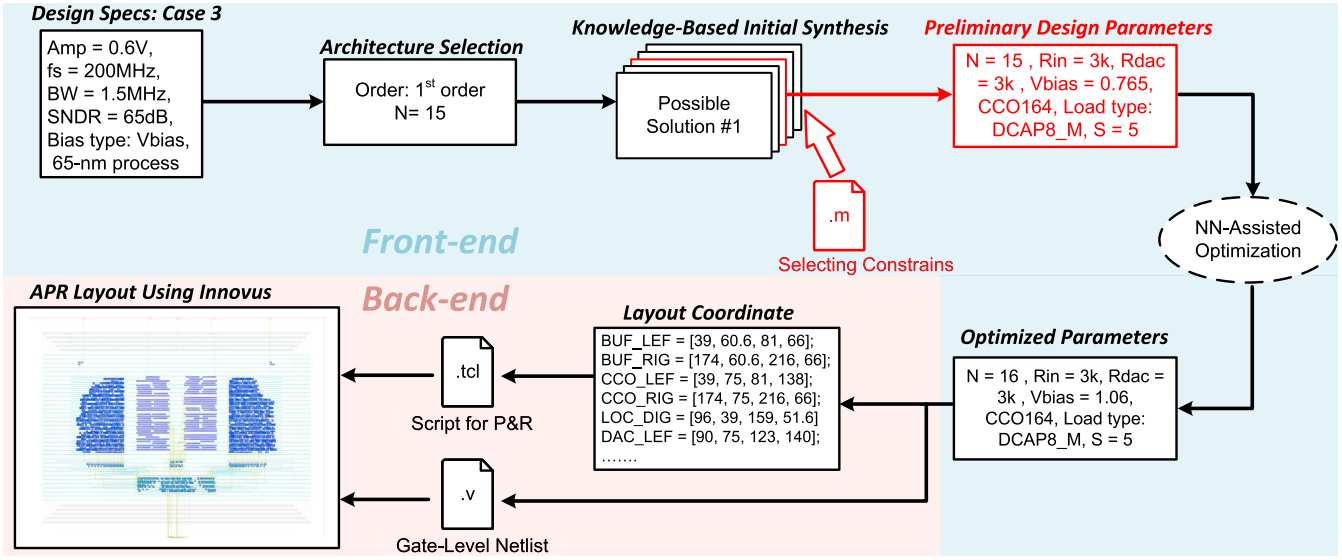

Fig. 14. Example generation flow of case 3.

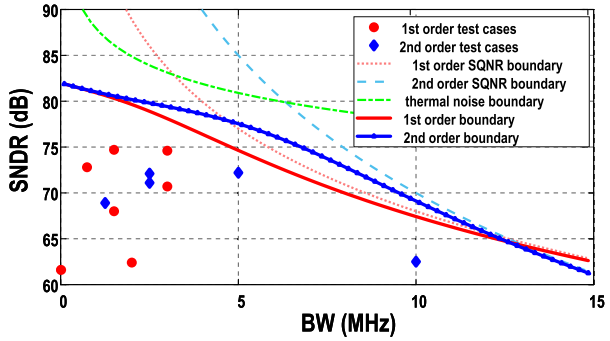

Fig. 15. Performance boundary of the generator.

TABLE II
PERFORMANCE COMPARISON PRE/POST OPTIMIZATION

		Case 7 (1st order)	Case 9 (2nd order)
Before Optimization	SNDR [dB]	72	68.19
	Power [mW]	0.594	0.919
	FoMs [dB]	169	162.5
Simulink-based Optimization	SNDR [dB]	73.87	70.8
	Power [mW]	0.523	0.89
	FoMs [dB]	171.5	165.3
	Time	33 min	27 min
ANN-based Optimization	SNDR [dB]	74.61	71.11
	Power [mW]	0.494	0.885
	FoMs [dB]	172.4	165.6
	Time	< 5 s	< 5 s

around 6 hours. Generating the training dataset and training for ANN took another 20 h in two 18-core 36-threads 3.1-GHz CPUs with parallel computing. A similar approach to [9], the ANN model is chosen to have three hidden fully connected layers with 64, 128, and 64 neurons, respectively, for optimal results. It is trained with 28 000 samples from the Simulink model. The SNDR error of the trained model is around 1 dB, which is effective for optimization in a company with a knowledge-based flow. Compared to the other circuit generators that usually spend hours, VSAGE takes less than 5 min from specifications to DRC and LVS clean layout under a 4-core 3.1-GHz CPU, thanks to the compact knowledge-ML hybrid flow. The results of the 12 designs in Table I are all one-shot designs without human intervention, which shows the robustness of the design. Fig. 14 illustrates an example generation flow for case 3.

As shown in Table I, the generator can output designs with a wide range of sampling frequency and BW, as well as the SNDR, showing its generality. The sampling frequency can range from 1 to 800 MHz, and the BW can range from 10 kHz to 10 MHz. The SNDR can reach to near 75 dB. The postlayout simulated SNDRs are close to the expected SNDRs with an average error around 1.5 dB. Notice that case 5 and case 8 are slightly deviate from the specifications, primarily due to the CCO not operating at its optimal point. Adjusting the bias current could help improve this. In addition, layout mismatches in the CCO may contribute to this degradation. These results are from the initial run, and users can further refine parameters, such as increasing the number of CCO stages, to mitigate these issues. The low FoMs in Case 1 is primarily due to the slightly higher fcco, which causes the digital gates to switch more frequently. In future iterations, adding multiple DCAPs as a load to further reduce fcco could enhance energy efficiency. The area mainly depends on the size of RDAC since it consumes most of the area. The area increases if the number of output stages or the unit resistance of RDAC increases, although multiple output stages ensure high resolution. The area in high F_s is smaller than in low F_s under the same SNDR requirements since high F_s leads to a lower RDAC value. This issue can be addressed with capacitive feedback in future iterations of the generator. Compared to 65-nm designs, 28-nm designs have better energy efficiency. This indicates that VCO-based ADCs are advanced-process friendly. The system noise is also estimated to define the performance boundary of this generator. As is illustrated in

TABLE III
COMPARISON WITH RELATED WORKS

	ASSCC 15 Waters [23] *	**VLSI 18 Ding [13]** *	**ICCAD 21 Liu [10]** †	**CICC 21 Chen [17]***	**DAC 17 Xu [21]†**	**JSSC 20 Zhong [19]***	**This work†**	
Architecture	MASH DTDSM	SAR	SAR	CTDSM	VCO-CTDSM	VCO-CTDSM	**VCO-CTDSM**	
Design automated	No	Yes	Yes	No	No	No	**Yes**	
Layout automated	Yes	Yes	Yes	Yes	Yes	No	**Yes**	
End-to-end time	Weeks	Minutes	2h	Weeks	Weeks	Months	**< 5min**	
Orders	3rd	0	0	3rd	1st	2nd	**1st**	**2nd**
Process [nm]	65	40	40	40	40	40	**28**	**65**
Voltage [V]	1	1	1.2	1.2	1.1	1.1	**1**	**1.2**
Fs [MHz]	150	32	100	1024	750	260	**400**	**200**
BW [MHz]	2.34	16	50	5	5	5.2	**3**	**2.5**
SNDR [dB]	56.3	47.37	56.3	67.4	69.5	69.4	**74.61**	**71.1**
Power [mW]	0.872	0.187	0.76	0.77	1.37	0.86	**0.494**	**0.885**
Area [mm^2]	0.014	N/A	N/A	0.033	0.012	0.086	**0.016**	**0.028**
FoM_W [fJ/step]	348.6	30.7	10.8	40.2	56.2	35.7	**18.7**	**60.3**
FoM_S [dB]	150.6	156.7	164.5	165.5	165.1	167.2	**172.4**	**165.6**

† Post-layout simulation results.

* Tapeout measurement.

Fig. 15, the precision of the architecture is primarily limited by mismatch and thermal noise at low BWs, and by the maximum sampling frequency at high BWs. Combined with an assumed mismatch-limited THD of 82 dB, these factors constrain the SNDR to approximately 80 dB at low BWs and around 67 dB at high BWs.

To verify the effectiveness of ANN-based optimization, Table II shows the pre/post optimization results of two design cases. Case 7 is 400 MS/s first-order in 28 nm, and case 9 is 200 MS/s second-order in 65 nm. The comparison is conducted in three ways, one was without optimization in the overall flow, one used Simulink-based (i.e., replaces the ANN with the Simulink testbench) optimization, and the last one used ANN-based optimization during circuit synthesis. Table II compares postlayout simulation results and their optimization time. After optimization, a noticeable SNDR and power improvement can be seen. Using Simulink-based optimization requires a much longer time than ANN-based optimization. This is because, for one iteration, Simulink will need more than 3 min to output the result, while ANN can output almost instantly. Thus, ANN-based optimization can explore more potential points with different initial parameters. This also proves the effectiveness of our optimization flow. Fig. 16 shows two spectrums of 4096-point FFT of the above two designs, respectively. Both of which demonstrate clear first-order and second-order noise-shaping effects. Notice that for the first-order design, the hump in high frequency seems sharp; this is due to the slightly larger than one loop gain for postlayout simulation. This also indicates the robustness of the design.

Table III presents the summary and comparisons of our work with prior manual-designed, semi-auto-designed ADCs, and auto-designed ADCs. Our approach yields competitive results with manual VCO-based ADC design but can be completed

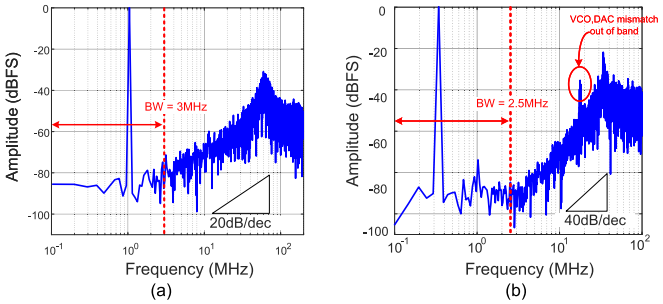

Fig. 16. Postlayout simulation results of the ADC spectrum of: (a) Case 7 and (b) Case 9.

within minutes, contrasting with the weeks or months required for manual and semi-auto designs. Compared with synthesized SAR ADC and other layout-automated $\Delta\Sigma$ ADC, our work has better SNDR, plus our work has minimum generation time and the most straightforward flow. It demonstrates an effective and reliable solution for agile $\Delta\Sigma$ ADC design and intellectual property (IP) reuse.

V. DISCUSSION

There is notable potential for enhancement on the layout side. In floorplanning, using relative locations is currently straightforward, but it limits block placement flexibility. Future versions could employ more advanced algorithms, such as a modified Gordian approach with symmetry constraints, to achieve a more compact and optimized floorplan, leading to enhanced ADC performance. For the P&R process within each building block, it currently relies on default algorithms, which are convenient to implement but fall short in meeting the specific needs of AMS circuits such as symmetry. Default algorithms tend to prioritize total wire length, whereas AMS circuits require a focus on matching. Efforts have been made to enhance analog layout optimization using

digital P&R tools. Examples include ALOE, a simulation-free analog layout optimization flow utilizing digital P&R tools, as referenced in [24], and a hierarchical template-based methodology illustrated in [25]. These optimization attempts aim to address the unique requirements of analog layouts within a digital P&R framework. In future versions, leveraging such optimization flows holds the potential for further performance improvements.

Currently, the generation flow is tailored for first- and second-order architecture. The current quantizers in use are the XOR [26] and phase quantizer [27]. For VCO-based ADCs, several enhanced quantizers have been proposed, such as PEQ [28], PFD [29], and DPFD [30]. Each of these quantizers offers distinct advantages in terms of power efficiency, hardware complexity, and sampling frequency. Future iterations aspire to enhance flexibility in the architecture. The vision is to enable a more adaptable approach, starting from a high-level user-defined Simulink model. By accurately mapping ideal integrators and quantizers to VCO building blocks, the entire flow aims to seamlessly generate the correct circuit netlist and layout, opening possibilities for broader applicability. It is possible that our framework can also be extended to other digital-alike AMS circuits, such as VCO-based and TDC-based comparators [31], [32], digital-alike loop filter built by digital OTA [33], [34], [35] for noise-shaping SAR ADC.

VI. Conclusion

In this article, we present an end-to-end automated VCO-based ΔΣ ADC generator, which is the very first of its kind. With minimal input specifications and minor modifications to the standard library, the generator can swiftly output the DRC- and LVS-clean layout. Our generator shows the advantages and potentials of using digital-alike circuits to realize large-scale AMS circuits in both synthesis and layout. From the synthesis perspective, digital-alike circuits streamlining circuit design by enabling block-level synthesis rather than transistor-level sizing. On the layout side, digital-alike circuits can leverage the digital back-end flow for layout generation, eliminating the need for specialized analog tools and enhancing efficiency. The performance of the generated designs is also competitive with manually designed ones while a huge time was saved.

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