

A 2-Way W-Band Power Amplifier with an Isolated Combining Output Network for Power Back-Off Efficiency Enhancement in 16nm FinFet Technology

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Abstract—This paper introduces a W-band sequential power amplifier (PA) [1] with a novel output network designed to minimize passive and combiner losses, while reducing the overall footprint compared to conventional sequential and Doherty PAs [2]. An isolated output combiner sums two PAs operating in two different modes: the main amplifier operates in class AB and the auxiliary amplifier operates in class C. The measured PA achieves a saturated output power (P_{sat}) of 13 dBm and a gain of 12.5 dB with 3 dB bandwidth from 79.5 GHz to 94.5 GHz. Additionally, it demonstrates a peak Power Added Efficiency (PAE) of 19.4% and a 14.6% PAE at 6 dB power back-off (PBO) at 87.5 GHz. Furthermore, the PA achieves a data rate of 12 Gb/s for a 16QAM signal with an average output power of 5 dBm, an average PAE of 10%, and an EVM (RMS) of -20 dB. The PA was fabricated in 16-nm FinFet technology with core area of 0.15mm². To the authors' knowledge, this PA has the highest PAE at 6dB PBO for CMOS PAs operating in the W-Band.

Index Terms—Power Amplifiers, Sequential, W-Band, High Efficiency, Isolated Combining, EVM, FinFet, CMOS.

I. INTRODUCTION

The escalating demand for elevated data rates propels the exploration of higher frequency bands, such as the W-Band. At these frequencies, overcoming high path loss necessitates the delivery of substantial output power from the PA. In CMOS technology, achieving high output power often involves either stacking more transistors or employing power combining techniques. Stacking, while effective, poses challenges in bulk CMOS technology and is better suited for SOI technologies. Consequently, power combining emerges as the preferred method for achieving higher output power.

However, the introduction of a combining network introduces significant loss, impacting the overall efficiency of the PA and thereby influencing its performance. Furthermore, the pursuit of high data rates necessitates the utilization of high order modulation schemes characterized by a high peak-to-average power ratio (PAPR). The high PAPR requires that the PA operate at an average power significantly lower than its P_{sat} , resulting in a substantial reduction in the average PAE compared to the peak PAE.

Although Doherty PAs are well known for their effectiveness in achieving high efficiency at back-off power levels through load modulation, their utilization at these frequencies faces limitations. The limitations emerge from the need for very short channel length transistors to realize high transit frequency (f_T), which leads to a detrimental reduction in output resistance (r_o). The reduced r_o contributes to a decrease

in the 6 dB back-off efficiency improvement associated with the Doherty PA.

The proposed sequential PA employs two parallel PAs functioning in distinct modes: a main amplifier in class AB and an auxiliary amplifier in class C. Similar to the Doherty PA, the main amplifier operates exclusively at low input power, with both the main and auxiliary amplifiers in simultaneous operation at high input power. Different from a Doherty PA, an isolated combining output network is introduced allowing the main amplifier to function with a load impedance of Z_{opt} at both low and high input power levels, while enabling the auxiliary amplifier to operate with a load impedance of Z_{opt} at high input power. This constant load impedance across power is due to the utilization of the isolated combining output network which prevents load modulation, distinguishing it from the Doherty PA. The technique used in this paper eliminates the dependency of the PAE improvement at 6 dB back-off from the r_o of the transistor. High-speed adaptive bias circuits enable the auxiliary amplifier to contribute an equivalent power level as the main amplifier at elevated input power levels.

II. SEQUENTIAL PA VS DOHERTY PA

The Doherty PA is recognized for achieving $2\times$ improvement over Class B PAs at 6 dB back-off power. Nevertheless, this assertion relies on the assumption that the transistor has infinite r_o . This assumption does not hold true in modern technology, where small channel lengths are used, leading to a decrease in the transistor's r_o . The following simplified analysis illustrates the impact of incorporating the r_o in the examination of both the Doherty PA and the sequential PA in this work.

Fig. 1a shows a single-ended, single-transistor Class B PA featuring load resistance $R_L = R_{opt}$ and a drain current

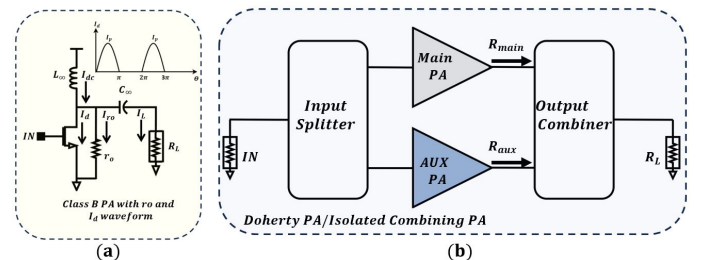


Fig. 1. Class B PA and common block diagram for Doherty/Sequential PAs.

of I_d . Assuming the transistor possesses a maximum current capability of $2I_{max}$, expressed as the maximum value of I_p across P_{in} . The equations governing the current directed to the load I_L , the DC current I_{dc} , and the efficiency of the Class B PA at 6 dB back-off are expressed as follows:

$$I_L = \frac{I_{max}}{2} \frac{r_o}{r_o + R_{opt}}, I_{dc} = \frac{I_{max}}{\pi}, \eta = \frac{\pi}{8} \left(\frac{r_o}{r_o + R_{opt}} \right)^2 \quad (1)$$

Utilizing these equations, one can determine efficiency improvements for both the Doherty PA and the proposed sequential PA in comparison to a class B PA. The block diagram depicted in Fig. 1b serves as a versatile representation, accommodating both the Doherty PA and the proposed PA utilizing different input and output networks for each configurations. In the case of the Doherty configuration, the output network accounts for load modulation and power combining, whereas for the proposed PA, the output network is designed to maintain a constant load across power levels and facilitate power combining.

In both configurations, the main amplifier operates in class AB, while the auxiliary amplifier initiates operation at a 6 dB back-off from the P_{sat} due to its class C operation. Owing to the distinct load conditions between the two configurations, the fundamental current for the main amplifier at 6 dB back-off differs for each case. For the Doherty PA, the fundamental transistor current is $\frac{I_{max}}{2}$ with a load resistance of $2R_{opt}$, whereas for the sequential PA, it is $\frac{I_{max}}{\sqrt{2}}$ with a load resistance of R_{opt} . Thus the efficiency at 6dB back-off for the Doherty PA and sequential PA are given by the following equations:

$$\eta_{Doh} = \frac{\pi}{4} \left(\frac{r_o}{r_o + 2R_{opt}} \right)^2, \eta_{Seq} = \frac{\pi}{\sqrt{2} \times 4} \left(\frac{r_o}{r_o + R_{opt}} \right)^2 \quad (2)$$

These equations indicate that the efficiency improvement of the Doherty PA ($\frac{\eta_{Doherty}}{\eta_{classB}}$) relies significantly on the ratio between r_o and R_{opt} . As this ratio decreases, the efficiency enhancement for the Doherty PA also decreases. In contrast, the efficiency improvement for the sequential PA ($\frac{\eta_{Seq}}{\eta_{classB}}$) is not contingent on this ratio, achieving a 42% enhancement over class B, as illustrated in Fig. 2a.

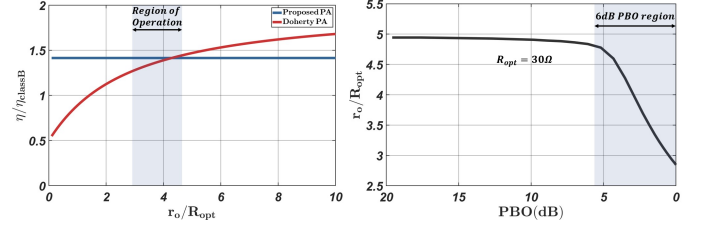
To enhance the PAE at 6dB PBO, it is crucial to carefully assess the ratio r_o/R_{opt} . Figure 2b illustrates this ratio for the main amplifier across various PBO values. Within the 6dB PBO range, the ratio r_o/R_{opt} , with $R_{opt} = 30\Omega$, decreases from 4.7 to 2.8. This indicates that for this operational range, the sequential PA should be favored over the Doherty PA. The main PA parameters are detailed in Section III.

III. CIRCUIT IMPLEMENTATION

A. Isolated Combining Output Network

To characterize the loss in the isolated combining output network, it is crucial to examine two scenarios. The first case involves a 6 dB back-off where the auxiliary amplifier is deactivated while the second case corresponds to P_{sat} where both amplifiers operate simultaneously. The loss in each of these cases is denoted as L_1 and L_2 , respectively.

$$L_1 = 10\log_{10}\left(\frac{P_{out}}{P_{main}}\right), L_2 = 10\log_{10}\left(\frac{P_{out}}{P_{main} + P_{aux}}\right) \quad (3)$$



(a) $(\eta/\eta_{classB})_{6dB PBO}$ for a Do- (b) r_o/R_{opt} for main PA output stage herty PA and the proposed PA.

Fig. 2. Effect of r_o/R_{opt} on the efficiency at 6dB PBO.

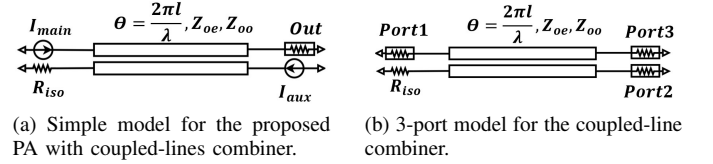


Fig. 3. Coupled line network model.

In this work, a coupled line network with reduced electrical length (θ) is employed as the output combiner, which is different from Doherty PAs and balanced PAs [3] that use 90° couplers. To assess the combiner loss, a simple current source model is utilized, as depicted in Fig. 3a. The 3-port model illustrated in Fig. 3b indicates that, for a coupled line network with $Z_o = 50\Omega$, $Z_{oe} = 110\Omega$ and $Z_{oo} = 23\Omega$, achieving complete isolation between port 1 and port 2 necessitates R_{iso} to be 50Ω regardless of θ . While employing $\theta = 90^\circ$ and $R_{iso} = 50\Omega$ achieves infinite isolation, it introduces substantial loss when $I_{aux} = 0A$, thereby degrading the PAE at 6 dB back-off.

Reducing θ to 30° improves the loss in the case of $I_{aux} = 0A$, but it increases the loss in the case of $I_{aux} = -jI_{main}$ due to the decreased coupling of $-7.5dB$ resulting from the reduced θ , as shown in the Fig. 4a. The loss values are still high and impact the PA efficiency.

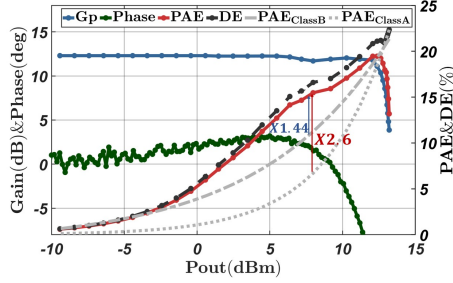
To address this issue, the isolation can be reduced to 20 dB instead of infinite isolation. This can be achieved by incorporating a capacitor $C_{iso} = 20fF$ in parallel to R_{iso} . This modification lowers the loss to less than 0.5 dB in both scenarios, with $I_{aux} = 0A$ and $I_{aux} = -jI_{main}$, while maintaining the impedance seen from output combiner isolated ports within a 15% variation in both cases as shown in Fig. 4b and Fig. 5. This network demonstrates low impedance variation across frequency, in contrast to the Doherty PA, which has a limited bandwidth (BW) due to achieving impedance inversion at a single frequency.

B. Proposed PA Design

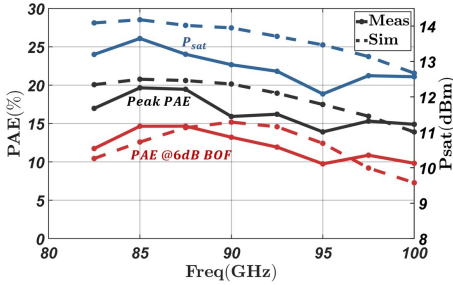
Fig. 6 illustrates the schematic diagram of the PA. The design features a two-stage configuration for both the main and auxiliary amplifiers. In the output stage of each amplifier, a width (W) of $6 \times 11.52\mu m$ is employed, accompanied by a neutralization capacitor C_{neut} of $42fF$. The driver stage utilizes a W of $2 \times 11.52\mu m$ with a neutralization capacitor

TABLE I
COMPARISON WITH STATE OF ART.

Reference	This Work		[4]	[5]	[6]	[7]	[8]
Technology	16nm FF CMOS		40nm CMOS	45nm CMOS SOI	130nm SiGe	90nm CMOS	22nm FF
Supply (V)	0.9		1.5	2	4	2.3	1
Freq (GHz)	87.5		72	60	110	94	75
Power Gain (dB)	12.5		20	12.9	21.8	20	16.6
P_{sat} (dBm)	13		21	20.1	22.7	16.8	12.8
Peak PAE (%)	19.4		12.4	26	18.7	16.4	26.3
PAE @ 6dB PBO (%)	14.6		7	16.6	12.1	5	12.5
PAE/PAE_{ClassB}	1.44		1.13	1.28	1.29	0.6	0.95
Modulation	16QAM	16QAM	64QAM	64QAM	16QAM		16QAM
Data Rate/EVM	8Gbs/-21dB	12Gbs/-20dB	0.8Gbs/-25.6dB	3Gbs/-23.1dB	8Gbs/-19dB		6Gbs/-20.5dB
P_{out}/PAE	7dBm/11.8%	5dBm/10%	15.9dBm/7.1%	13.8dBm/15.7%	13.7dBm/7.8%		5dBm/10%
Active Area(mm ²)	0.12		0.19	0.76	1.11	0.69	0.054



(a) Measured G_p , AM-PM, DE and PAE at 87.5GHz.



(b) Measured v. simulated P_{sat} , Peak PAE and 6 dB PBO PAE across frequency.

Fig. 8. Continuous wave measurements for the Proposed PA.

V. CONCLUSION

This paper introduced a W-band sequential PA featuring load modulation free combining through an isolated combining network. Simple equations are introduced to assess the impact of the transistor r_o on the performance of both the proposed PA and the Doherty PA. The results indicate that, at higher frequencies employing short-channel transistors, the proposed PA exhibits a superior PBO enhancement ratio compared to the Doherty PA. A practical implementation of the output network is demonstrated, focusing on optimizing its loss to achieve the highest PAE. This concept is validated by the measurement results, demonstrating not only high PAE but also a high data rate and good efficiency with high-order modulation.

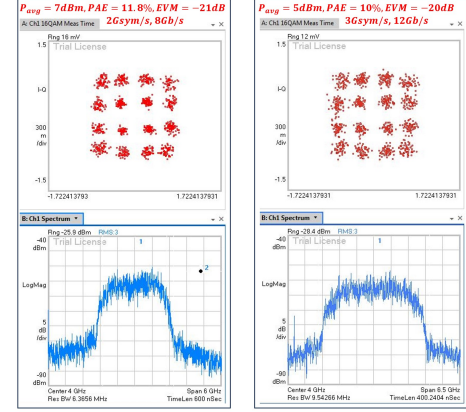


Fig. 9. EVM measurements for proposed PA at different symbol rates.

VI. ACKNOWLEDGEMENT

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