

Digital IC Design of a 45nm CMOS Chua Encryption Architecture for Resource Limited Devices

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Abstract—Theoretically, the behavior and outcomes of a physical system are predictable given a set of initial conditions. However, in practice, physical systems often exhibit randomness due to various factors. This phenomenon is known as chaos. Over the past four decades, chaos theory has emerged into a significant field of study with practical applications including encryption. Recently, it has gained popularity due to the rise of IoT applications and the need for security in wearable devices.

Implantable and wearable devices monitor vital health indicators such as body temperature, heart rate, blood glucose, and blood oxygen levels. Ensuring the security of user data in these devices is critical. Advancing in the age of IWDs necessitates investigating secure communication options. This research leverages Chua's chaotic equations in discrete-time to demonstrate MATLAB simulations for data encryption architecture in digital circuits.

The RTL code obtained from this MATLAB Simulink model was synthesized in Genus Stylus UI Mode. The gate-level netlist produced as a result of synthesis is used for digital IC design in 45nm technology. The project results contribute to the advancement of research involving chaotic circuits. The 100KHz design operates at 0.9V, consumes 0.486 μ W of power with an area of 0.005 mm², with 76% core utilization.

Index Terms—CMOS, Hardware Security, Chua's Chaotic Circuit, Genus, Innovus, Secure Communication, Implantable and Wearable Devices, Physical Design.

I. INTRODUCTION

The COVID-19 pandemic was an eye-opening experience for humankind. For a population with health checkups that were long overdue, we realized the importance of monitoring SPO_2 levels, heart rate, and body temperature regularly. We resorted to low-power, miniaturized, pocket-friendly health monitoring systems in our quest to understand our bodies and enable them to perform at their best.

The evolution of marketed wearable devices since 2013 shows a consistent increase in launches over the decade, with a notable dip in 2020 and 2021, presumably due to the pandemic [1]. Between 2023 and 2033, the global demand for pulse oximeters is projected to grow at a 6.4% CAGR, rising from

\$2.9 billion in 2023 to \$5.4 billion by 2033 [2]. In 2022, the market for wearable medical devices reached \$59.12 billion and is projected to expand to \$428.92 billion by 2031, with a CAGR of 28.6% [3]. Approximately 38% of adults with cardiovascular diseases in the US use wearable healthcare devices to monitor their heart functions [4].

Telemedicine, the use of telecommunication in medical practice, facilitates remote bidirectional communication between healthcare professionals and patients [5]. Dating back to late 1960s when the first prototype was developed [6], telemedicine has evolved to allow remote patient monitoring of vital health indicators. Its relevance has increased post-COVID-19, emphasizing the importance of no-contact diagnosis and treatment. Experts suggest that implementing telemedicine across medical specialties could reduce healthcare costs by 56% and travel costs by 94% [7]. Integration of implantable and wearable medical devices with telemedicine facilitates continuous monitoring and early diagnosis of diseases in patients.

The rise in Body Mass Index (BMI), cholesterol levels, and obesity among adults has led to an increased use of wearable devices for monitoring physical activity, sleep patterns, and energy expenditure [8]. In 2022, the American College of Sports Medicine identified wearable technology as the leading fitness trend, followed by home workouts and group physical activities [9].

In hindsight, Implantable and Wearable Devices (IWDs) carry inherent risks. The exposure of sensitive personal and health-related data of IWD users to significant security and privacy threats is a major concern. For instance, in 2021, researchers at WebSitePlanet uncovered an unprotected database containing approximately 61 million records of smartwatch users. In 2007, Vice President Cheney's cardiologist deactivated the wireless functionality of his pacemaker due to concerns about potential hacking, which could not only compromise data but also lead to controlled attacks via the device. These critical risks highlight the need for a robust hardware security architecture in the manufacturing of semiconductor chips utilized in IWDs.

In this paper we have directly implemented our MATLAB simulated Chua's architecture in Cadence using Genus for synthesis and Innovus for layout design and Pegasus for physical verification. With MATLAB Simulink supporting a dynamic procedure for ASIC design, this RTL extraction facilitates architectural simulation while maintaining the integrity of the RTL process from netlist through a DRC and LVS-clean system on chip. This procedure yields a Chua's architecture with low power and low area consumption, comparable to other state-of-the-art architectures, suitable for resource-limited devices.

II. TRANSCONDUCTANCE-CAPACITANCE-BASED SECURITY ARCHITECTURE FOR IWDs

The utilization of Cardiovascular and Implantable Electronic Devices (CIEDs) continues to rise, catering to various cardiac arrhythmias. These devices commonly employ the Medical Implant Communication Service (MICS) at a frequency of around 400 MHz [10]. On the other hand, cochlear implants, designed to restore hearing for individuals with hearing impairments, operate within a frequency range of 250-6500Hz, with a peak intelligibility rate of 73% [11].

Continuous Glucose Monitors (CGMs) are used by diabetes patients to observe their blood sugar levels. They also help clinicians understand the relationship between glucose spikes in blood and different organ functions. Most CGMs used today typically operate in frequency ranges between 128-135 KHz (low frequency) and 860-960 MHz (ultrahigh frequency) [12]. The 401-406 MHz frequency range is used by general-purpose medical devices for transmitting data, including information from medical implants and body-worn devices [13].

Figure 1 illustrates the area utilization comparison between an inductor-capacitor network and a transconductor-capacitor network when integrated onto a chip. It is evident that within the frequency range suitable for implantable and wearable devices to operate (from a few Hz to MHz), transconductor-capacitor-based circuits occupy a smaller die area than transconductor-inductor circuits. The complexity of signals in an RLC circuit surpasses that of an RC circuit, leading to slower operation of CAD tools during design and simulation. Moreover, extensive modifications to CAD infrastructure are necessary to accommodate inductance effects [14].

Unlike capacitive coupling confined to adjacent lines, inductive lines can interact with distant circuit lines, potentially causing crosstalk—a CMOS circuit issue where electromagnetic coupling occurs between switching and non-switching signal lines [15]. The use of inductors on a chip can result in catastrophic failures and increased power consumption. Digital circuits typically don't use inductors, and their design predominantly uses logic gates and flip-flops.

Ravi et al. [17] provides an overview of security attacks encountered by Implantable and Wearable Devices (IWDs). Securing IWDs involves implementing data security across layers to counter physical, network, software, and encryption attacks. Traditional encryption methods rely on algo-

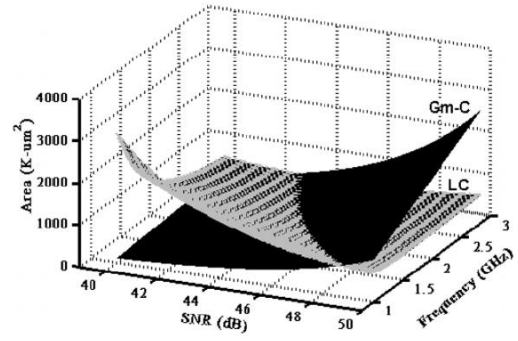


Fig. 1. Die area occupied by trans-conductor-capacitance circuits vs inductor-capacitor circuit for different SNR values [16]

rithms executed through complex software or additional micro-controllers, leading to high power consumption and increased hardware usage. This study leverages Chua's attractor and its randomness to develop an on-chip chaotic architecture for security in IWDs. The objective is to secure data at its source by integrating security measures within the same chip as biomedical sensors in IWDs.

III. LITERATURE REVIEW

The nonlinear dynamic properties of a modified four-dimensional Lorenz-Stenflo system are presented in [18]. This study encompasses the system-on-chip implementation of an analog four-dimensional chaotic oscillator using the TSMC 0.35μm CMOS process for encrypted communication applications. The research introduces a novel four-dimensional chaotic oscillator incorporating a multiplier and a two-stage operational amplifier to achieve increased gain and a wider output range.

Chaos-driven randomness plays a crucial role in applications such as Random Pattern Generation (RPG) and Random Number Generation (RNG). While Pseudo-Random Number Generators (PRNGs) have been historically utilized for security in Implantable and Wearable Devices (IWDs), they are susceptible to attacks due to limited energy and area resources for implementing cost-effective and efficient systems.

Güngör et al. [19] introduces the first monolithic implementation of a chaos-modulated Voltage-Controlled Oscillator (VCO)-based Random Number Generator in the TSMC 180nm process. Compared to designs incorporating inductors, this architecture offers improved immunity to external interference, particularly from side-channel attacks.

Techniques such as frequency band analysis [20], Blind Source Separation (BSS) [21], and Largest Lyapunov Exponent (LLE) [22] have been utilized for monitoring mental health conditions like epilepsy. Smartwatches aid users in tracking sleep patterns and understanding their impact on mood and daily performance. Roh et al. [23] explores a wearable mental state monitoring system incorporating non-linear chaotic analysis.

Paul et al. [24] introduce a dynamic parameter control method to achieve a wide chaotic range. The study presents

two designs implemented in the CMOS 65nm process. The first design occupies an on-chip area of $0.024mm^2$ with a power consumption of 2.33mW, while the second design covers $0.132mm^2$ of chip area and consumes 2.14mW. These designs utilize the concepts of a seed map (dynamic parameter-controlled chaotic map) and a controlled map (oscillator) for their implementation. The output of the oscillator is controlled by the seed map at each iteration, resulting in two distinct chaotic regions in the output map of the chaotic oscillator.

Gu et al. [25] employs a fully differential operational amplifier within the 180nm CMOS process to realize all the switched-capacitor (SC) circuits. The first stage is powered by an external bias current, while the second stage is powered by the common-mode feedback network. The paper presents a technique for concealed communication among IoT network sensor nodes using hyperchaotic maps. A comparison of the state of the art chaos circuits with our work is presented in section VIII.

IV. CHUA'S ARCHITECTURE IN CONTINUOUS AND DISCRETE-TIME

Ravi [17] et al. explores the Chua's model in continuous time and records the results of the FPGA simulation. The Simulink model was interfaced with Xilinx System Generator to obtain FPGA-mapped verilog code. The model was implemented on the Artix-7 Nexys A7 100T FPGA board, an accessible and powerful platform previously known as the Nexys 4 DDR.

The discrete-Time Chua's Model for Digital IC Implementation was implemented based on this design in MATLAB Simulink. The Simulink model described in [17] utilizes continuous-time blocks to generate chaos. Although this model was successfully implemented on an FPGA to observe signal encryption and decryption using chaos, transitioning to an ASIC digital IC implementation requires the design to function in discrete time. To accomplish this, continuous-time integrators were replaced with discrete-time integrators using the forward Euler method. Additionally, to address the issue of algebraic loops in HDL code generation, small unit delays were introduced in the feedback loops. The Simulink model, incorporating discrete-time integrators and unit delays is depicted in the figure 2. The outputs Xr , Yr and Zr are plotted against each other to observe chaotic attractors as illustrated in figures 3 - 6. The RTL code and test bench for this model were extracted using the HDL Coder application in Simulink.

The encrypted signal and decrypted signal were analyzed in the Simulink Data Inspector against the input pulse signal. Figure 7 shows the encrypted signal whose behavior is independent of the input signal. The raw decrypted signal is observed as in 8 which needs further processing and investigation to obtain the original input from the decryption module presented in figure 2.

V. RTL SIMULATION IN XCELIUM

The RTL code generated in Simulink's HDL Coder for the transmitter part of the model depicted in Figure 2, along with the testbench generated with constant input blocks, was simulated using Xcelium. The resulting 16-bit output waveform is shown in figure 9. The simulation was carried with the 16-bit input 1101011001110010 to record the output in figure 10.

VI. SYNTHESIS IN GENUS

The technology-independent RTL code was synthesized using Genus by mapping it to the 45nm technology node library files. The synthesis process involved reading in the RTL code, the Synopsys Design Constraints (SDC) file, and the 45nm technology library files. These inputs were used to perform synthesis, resulting in the generation of a gate-level netlist. This process ensured that the RTL design was converted into a gate-level netlist, meeting specified design, timing, and technology constraints for physical implementation.

Some of the key outputs obtained post-synthesis are synthesized netlist, SDC file, scandef file, area, and power consumption. The power consumption of the design post synthesis was observed to be 0.349 μ W.

VII. PHYSICAL DESIGN IMPLEMENTATION IN INNOVUS

The gate-level netlist obtained post-synthesis contains information pertaining to logic gates and the connections between them. The resultant netlist from synthesis in Genus was imported into Innovus along with the technology LEF files for physical design implementation. The multi-mode muti-corner (MMMC) file is another crucial file that contains post-synthesis SDC, RC corners and timing library information. It was imported to ensure accurate timing analysis and optimization.

A. Floorplanning

To create a floorplan for the design, a chip height-to-width ratio of 1 was used with a core area utilization of 72%. The core to die boundary was maintained at $2.5\mu m$. The subsequent steps are explained below.

1) *Powerplanning*: Power rings were added to carry VDD and VSS around the chip. VDD and VSS power rings were implemented around the core area using metal layer 11 for horizontal connections at the top and bottom of the core. Metal layer 10 was used for vertical connections on the left and right. The metal layer width was set $0.7\mu m$, and the spacing between adjacent power rings was set to $0.2\mu m$.

VDD and VSS power stripes were inserted using metal layer 10 in the vertical direction to carry power supply across the chip. The width of these stripes was set to $0.3\mu m$, with a spacing $0.4\mu m$. The distance between the stripes was maintained at $5\mu m$.

Global net connection was carried out to link the VDD and VSS nets to the standard cell pin names. Power rails were created with vias placed at the intersection of rails and stripes to ensure connectivity throughout the chip and power supply to the standard cells.

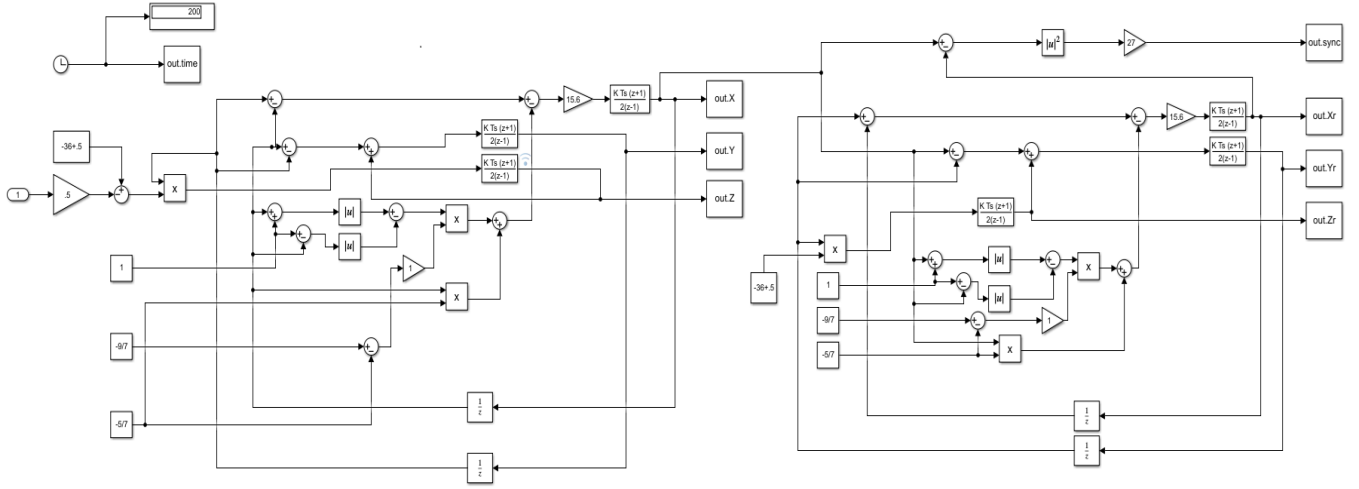


Fig. 2. Simulink model of the discrete-time security architecture with encryption and decryption blocks developed from Chua's equations

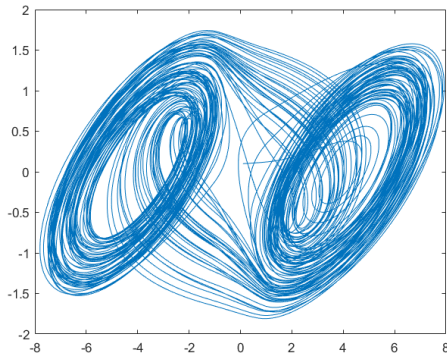


Fig. 3. *Out.X* vs *Out.Y* plot

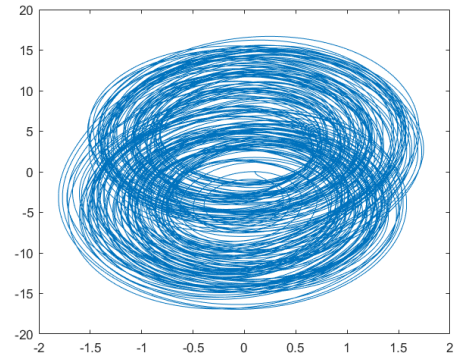


Fig. 5. *Out.Y* vs *Out.Z* vs plot

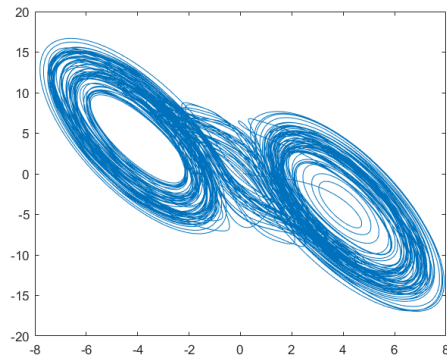


Fig. 4. *Out.X* vs *Out.Z* plot

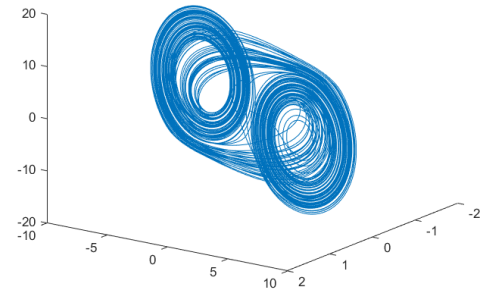


Fig. 6. *Out.X* vs *Out.Y* vs *Out.Z* plot

2) *I/O pin assignment*: The 39 I/O pins with a width of $0.08\mu m$ and depth of $0.25\mu m$ each, were placed across the four edges of the die area. The control signals are placed at the top edge with an offset of $27.5\mu m$ and spacing of $20\mu m$

to ensure effective clock distribution. The input bus $in[15 : 0]$, the scan input pin dft_sdi_1 and the mode selection pin SE are placed on the left edge with the individual pins placed evenly at a $4.5\mu m$ with an offset of $8\mu m$.

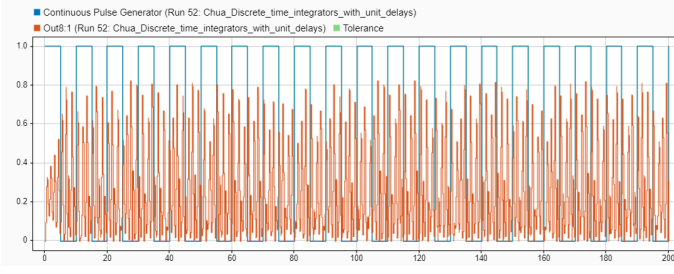


Fig. 7. Comparison of input pulse and encrypted output from transmitter block in the Simulink model presented in figure 2.

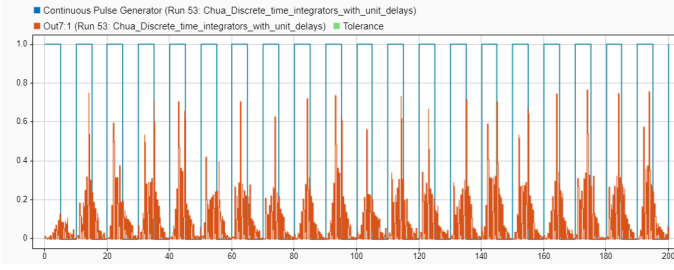


Fig. 8. Raw decrypted message signal obtained from the receiver block in the Simulink model presented in figure 2.

The output clock enable pin is placed at the bottom with an offset of $47\mu m$. The output bus $out[15:0]$ and the scan output pin dft_sdo_1 are placed on the right edge with an offset of $10\mu m$ and pin spacing of $4.2\mu m$. Table I summarizes the I/O pin assignment.

TABLE I
I/O PIN ASSIGNMENT FOR THE 16-BIT DESIGN

Pin name	Location	Layer
clk	Top	2
reset	Top	2
clk_enable	Top	2
in[15:0]	Left	3
SE	Left	3
dft_sdi_1	Left	3
ce_out	Bottom	2
out[15:0]	Right	3
dft_sdo_1	Right	3

3) *Addition of physical cells*: Endcap cells, also known as boundary cells were placed on the left and right ends of site rows to protect the standard cells at the edges from damage due to ion-scattering. Tap cells were placed in a checkerboard pattern throughout the chip with a spacing of $15\mu m$ to avoid CMOS latchup.

B. Placement

The scandef file was loaded to provided scan chain information. The standard cells were then placed in site rows within the defined core area. The design was checked for congestion post placement, and 0% vertical congestion and 0% horizontal congestion were observed. Spare cells were added. Early global routing was carried out to identify congestion following the placement of standard cells.

C. Clock Tree Synthesis

The process of distributing the input clock signal to all sequential elements of a chip is called clock tree synthesis with minimum skew and latency. The design uses a single clock port named clk . The skew for the primary clock group was calculated as 0.0066ns. The latency is 0.150 ns.

D. Routing

Routing is the process of introducing physical wire connections between the different elements of the integrated circuit like I/O pins and standard cells. NanoRoute was set up and carried out to address signal integrity and timing early in the routing process. Routing was carried out, followed by post-route optimization to mitigate DRC issues in the design.

E. Physical Verification

After routing, filler cells were added to maintain n-well and p-substrate continuity throughout the chip. Design Rules Checks (DRC) and Layout Versus Schematic (LVS) checks were carried out for the design in Pegasus with GDS, netlist and map files from Cadence's 45nm technology files. Layout issues like shorts and minimum spacing violations were resolved to obtain a clean layout with 0 DRC and LVS violations.

To summarize this section, we processed the physical design implementation using Innovus. After importing the gate-level netlist and necessary files, floorplanning and powerplanning were performed, including setting up power rings and stripes. I/O pins were assigned specific locations around the die, and endcap and tap cells were added for protection and to prevent latchup. Standard cells were placed and checked for congestion, followed by clock tree synthesis to ensure minimal skew and latency. Routing was completed with NanoRoute for signal integrity and optimization. Finally, physical verification was conducted, including DRC and LVS checks, to ensure a clean layout with no violations.

VIII. CONCLUSION

This research presents a novel approach to ASIC digital IC design by leveraging Simulink's HDL Coder to extract a functional RTL code for an on-chip data encryption module. The continuous-time model in [17] was converted to a discrete-time model from which the RTL code was obtained for the chaotic encryption architecture. The SDC file was composed to include clock frequency, and input/output pin delays. This RTL code was then synthesized in Genus with DFT inputs, SDC file, and 45nm library files to obtain the gate-level netlist for digital IC design. The physical design implementation from floorplanning through routing were carried out in Innovus followed by physical verification in Pegasus.

The design was implemented with at a frequency of 100KHz – within the desired frequency range for implantable and wearable medical devices. The initial core utilization at the floorplan stage was 76%, and the post-route density with filler cells is 89.29%. The system on chip uses an input voltage of 0.9V, consumes $0.005mm^2$ on-chip area and a total power of

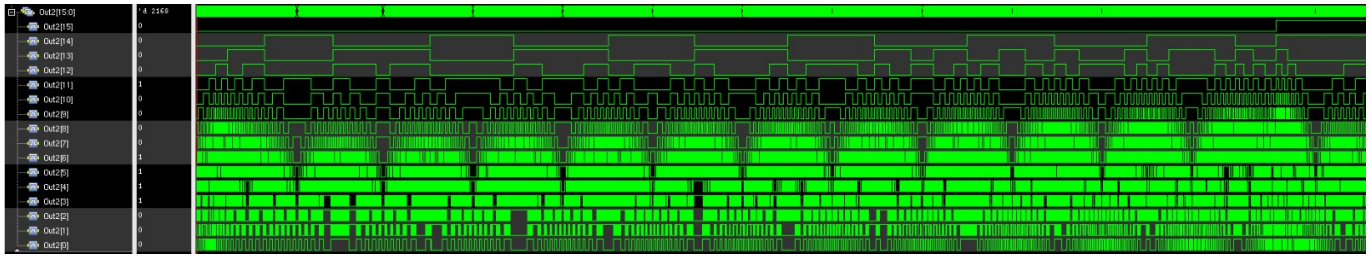


Fig. 9. Results from the RTL simulation of the verilog code for the encryption module along with the testbench for a 16-bit binary 0 input.

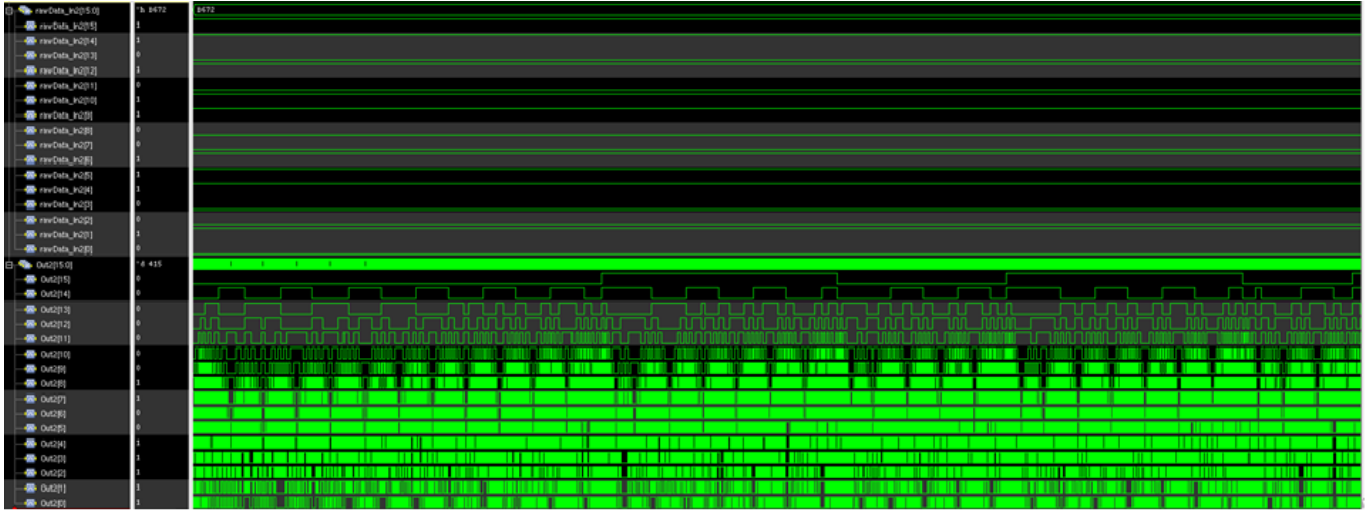


Fig. 10. Results from the RTL simulation of the Verilog code for the encryption module along with the testbench for a 16-bit binary input.

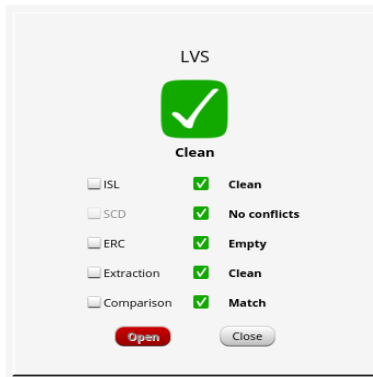


Fig. 11. Clean LVS observed in the Pegasus Results Viewer

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VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 46.000 86.450} 1 of 2
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {46.000 0.000 90.400 86.450} 2 of 2
VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.

Verification Complete : 0 Viols.

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Fig. 12. Clean DRC observed in Innovus terminal

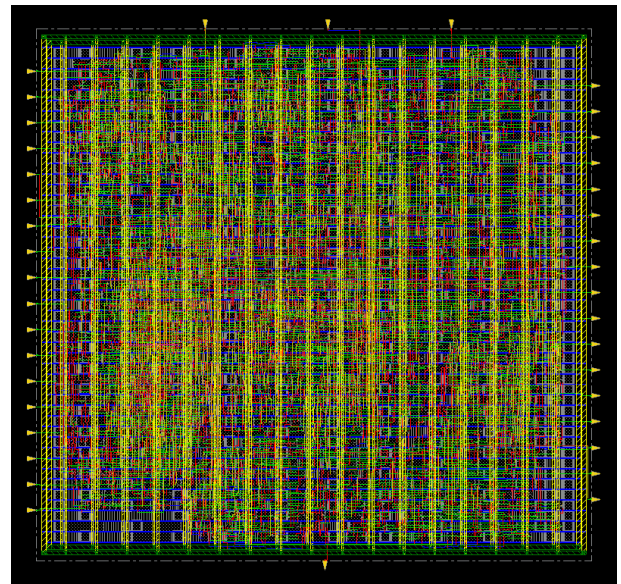


Fig. 13. Final Layout of the on-chip 16-bit encryption module

0.486 μ W of which 0.234 μ W (48.27 %) is the internal power, 0.143 μ W (29.5 %) is the switching power, and 0.108 μ W (22.22 %) is the leakage power. The resultant System On Chip is now ready for fabrication. A comparison of the state of the

TABLE II
COMPARISON TABLE WITH STATE OF ART CHAOTIC COMMUNICATION
ARCHITECTURES

Reference	Year	Design	Area	Supply	Power
[18]	2015	0.35 μ m	1.845mm ²	1.4V	360m W
[26]	2016	180nm	0.00045mm ²	0.6V	0.082 μ W
[23]	2016	0.13 μ m	11.75mm ²	1.2V	259.6 μ W
[27]	2019	0.18 μ m	28,000 μ m ²	1V	25 μ W
[28]	2019	65nm	0.556 μ m ²	5V	1.84 μ W
[29]	2020	0.18 μ m	1.5mm ²	1.8V	1.5mW
[24]	2021	65nm	0.024mm ²	1.2V	2.33mW
[24]	2021	65nm	0.132mm ²	1.2V	2.14mW
[19]	2021	180nm	4000 μ m ²	1.8V	70 μ W
[25]	2021	180nm	2mm ²	2V	4.5mW
[30]	2023	0.35 μ m	2mm ²	3.3V	1.7mW
[31]	2023	45nm	50 μ m ²	3V	5mW
This work	2024	45nm	0.005mm ²	0.9V	486.4 μ W*

art with our work is presented in table II.

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