IEEE Open Journal of
Power Electronics

Received 9 January 2024; accepted 24 January 2024. Date of publication 29 January 2024;
date of current version 9 February 2024. The review of this article was arranged by Associate Editor Telles Brunelli Lazzarin.

Digital Object Identifier 10.1109/OJPEL.2024.3359479

Design of a 2.5 kW Four-Level Interleaved Flying Capacitor Multilevel Totem-Pole PFC Converter With AC-Side Passive Volume Optimization

NAVEED ISHRAQ (Student Member, IEEE) AND AYAN MALLIK (Senior Member, IEEE)

Arizona State University, Mesa, AZ 85212 USA

CORRESPONDING AUTHOR: AYAN MALLIK (e-mail: ayan.mallik@asu.edu)

This work was supported by the National Science Foundation under Grant 2236846.

ABSTRACT In this article, a high-efficiency and high-density 2.5 kW four-level interleaved flying capacitor multilevel (FCML) totem-pole bridgeless power-factor-correction (PFC) rectifier with 200 V GaN devices is analyzed, designed, and tested. This 2.5 kW four-level continuous conduction mode (CCM) GaN totem pole PFC operates with three times inductor current ripple frequency than that of the switching frequency which significantly reduces the size of the inductors while also supporting switching loss reduction. This article compares the loss of the two-level CCM GaN totem-pole PFC, four-level non-interleaved FCML PFC and interleaved four-level FCML PFC with the same ripple frequency (300 kHz) and shows that the interleaved four-level CCM GaN PFC has much less device loss. In addition, this article discusses the detailed EMI spectrum analysis and derivation of the mathematical model for determining the attenuation requirement of the four-level interleaved FCML PFC converter followed by volumetric co-optimization of AC-side passives i.e., the boost inductor and differential mode (DM) EMI filter. A 2.5 kW four-level interleaved FCML GaN totem-pole PFC prototype with an optimized 94 kHz switching frequency is developed and tested in this article. The converter exhibits a peak efficiency of 99.14% with system power density reaching 89.47 W/inch^3.

INDEX TERMS Flying capacitor multilevel (FCML), gallium nitride (GaN), interleaved totem-pole, power factor correction (PFC).

I. INTRODUCTION

Numerous topologies and control schemes of PFC converters have been developed to achieve output voltage regulation with high efficiency and lower harmonic distortion in electrical vehicle charging and data center applications [1]. Improving the efficiency of the PFC rectifier is very critical to improve the power supply system efficiency. The bridgeless PFC topologies are receiving more interest due to their reduction of the diode-bridge conduction loss [2]. The dual-boost bridgeless PFC removes two line-frequency diodes, but it still has two low-frequency diodes in the circuit. Besides, since the two boost converters work alternatively, the utilization of the inductors and the devices in the dual-boost PFC are low [2], [3]. The GaN totem-pole bridgeless PFC is considered as a major solution recently, since the 650 V enhancement-mode GaN high electron mobility transistors (HEMTs) have no reverse recovery issue [4], [5], [6]. The switching frequency of the CCM GaN totem-pole PFC is normally under 100 kHz to reduce the switching loss. Compared with the traditional hard-switching boost PFC, the main inductor size of the GaN totem-pole PFC is not reduced due to their similar frequency range. The flying capacitor multilevel (FCML) converters can achieve much higher current ripple frequency with reduced voltage stress per device and lower switching losses. The current ripple frequency of a four-level FCML PFC converter is three times the switching frequency, thus offering a considerable shrinkage in the inductor volume. The non-interleaved FCML converters are traditionally used for medium voltage power electronics [7], [8], [9]. Recently, they have also been demonstrated with high efficiency and high density for

low-voltage grid-connected applications [10]. A 1.5 kW bridgeless seven-level FCML boost PFC is reported in [11]. With twelve 100 V GaN devices which work at 150 kHz, the peak efficiency is reported as 99.07%. However, in this topology, there are four line-frequency Si MOSFETs, while the totem-pole PFC has only two of them. Besides, the loss is not evenly distributed between the high-side devices and low-side devices as the boost PFC is not a symmetrical topology, which results in non-uniformity in thermal management performance of the power devices. The FCML totem-pole bridgeless PFC topology combines the FCML boost converter and the totem-pole PFC. It addresses the above issues of the FCML boost bridgeless PFC. A 200 W four-level FCML totem-pole PFC rectifier with 200 V Si MOSFETs is reported in [12]. However, due to the high switching loss and reverse recovery loss of 200 V Si MOSFETs, the efficiency is only around 98% at 150 kHz switching frequency. A 3 kW three-level FCML totem-pole PFC with two 150 V Si MOSFETs in series is implemented with 99% efficiency in [13] since the performance of 150 V Si MOSFETs is significantly improved compared with 200 V Si MOSFETs. However, due to its low switching frequency 70 kHz and the three-level operation, the main inductor size is still large [13], and not improved as significant compared with the two-level GaN totem-pole PFC. Besides, the voltage balance between the two series-connected 150 V MOSFETs is another major reliability issue. As the number of levels rises, the FCML boost inductor's volt-second falls squarely [14], [15], which aids in the inductor's contraction. To reduce the main inductor size while achieving 99% efficiency, a 2.5 kW CCM four-level interleaved FCML GaN totem-pole PFC rectifier is designed, analyzed, and implemented in this article. Due to the four-level operation, the device voltage stress is only one-third of the dc-link voltage, and the inductor current ripple frequency is three times the switching frequency. In this article, 200 V enhancement-mode (E-Mode) GaN devices are utilized, and the optimized switching frequency is designed to be 94 kHz, while the inductor current ripple frequency is 282 kHz. The inductor current ripple frequency of this four-level interleaved FCML GaN totem-pole PFC is significantly higher than that of the traditional CCM two-level GaN totem-pole PFC. Thus, the inductor size is dramatically reduced. In addition, the switching loss is very low due to scaled down voltage stress across each device. To reduce the conduction losses, interleaving technique is employed where a second FCML leg comprising high frequency switches operates exactly that of phase 1, except that the PWMs are shifted 60o with respect to phase 1. This has the effect of reducing the input ripple current [4], [16], [17]. Higher efficiency is realized since the input current is split across two paths and can substantially lower I^2R losses. In this article, to show the advantage of the four-level interleaved GaN totem-pole PFC, the device loss reduction of the four-level GaN PFC, compared with the two-level and four-level non-interleaved GaN PFC under the same ripple frequency is investigated in detail.

The key contributions of this article are as follows:

a) Our work is the first to demonstrate the superior efficiency and power density using 200 V GaN devices for the four-level interleaved FCML totem-pole PFC, yielding 3x effective frequency of inductor current, with cascaded benefits of current ripple cancellation through interleaving mechanism.
b) Comprehensive explanation of the waveform dynamics of individual phase currents and grid current under all operating modes of Interleaved FCML PFC converter and its control strategy for closed-loop regulation.
c) Extensive analysis of the input current Fast Fourier transform (FFT) model of the FCML PFC converter and interleaved FCML PFC converter for evaluation of switching harmonics amplitudes and hence conducted EMI spectrum quantification of inductor current, subsequently followed by volume co-optimization of DM EMI filter and boost inductor.
d) Multivariable lumped formulation of the EMI filter inductor, capacitor and boost inductor volume followed by its co-optimization using Lagrange multiplier method to minimize the total size of AC-side passive components.
e) Computation of total device loss and inductor power loss based on the individual phase current reconstruction, followed by a comparative loss evaluation performed against totem-pole PFC and FCML PFC counterparts.

This article is organized as follows. In Section II, the interleaved FCML topology and mode-derived operating principle is discussed. The input current EMI spectrum computation and boost inductor-EMI filter co-optimization are provided in Section III. Section IV compares the overall loss breakdown of the interleaved FCML PFC with the totem-pole PFC and single phase non-interleaved FCML PFC. Finally, the design and implementation of the hardware prototype and experimental results validating the steady state performance are illustrated in Section V and the conclusions are given in Section VI.

II. TOPOLOGY AND OPERATIONAL PRINCIPLE OF INTERLEAVED FCML TOTEM-POLE PFC

The four-level interleaved FCML GaN based totem-pole PFC circuit topology is illustrated in Fig. 1, which includes the high frequency switches Q1a-Q3b and M1a-M3b followed by a line frequency leg with switches S1 and S2 operating at 60 Hz line frequency. This topology essentially combines the fundamental structures of the FCML boost converter and the bridgeless totem-pole PFC. The totem-pole bridgeless topology is popular due to its control simplicity and lower switch count. However, to attain high efficiency and reduce the transistor switching loss, this topology imposes a limit on the maximum operable switching frequency. Consequently, the volume of the input inductor size becomes large which is a drawback in terms of power density. On the other hand, the non-interleaved FCML boost converter is used typically for medium voltage applications that utilize devices with reduced voltage ratings with superior loss performance [5].

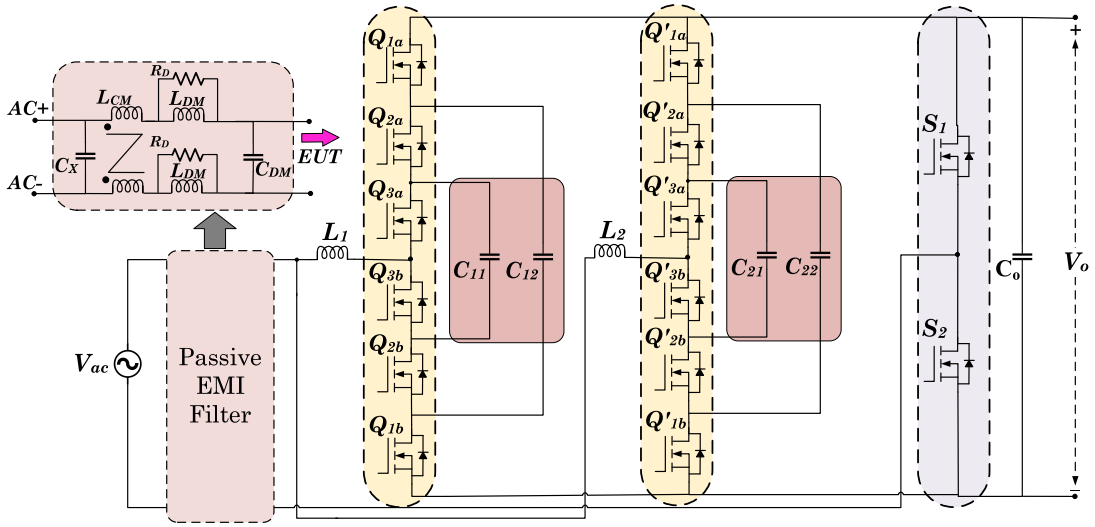

FIGURE 1. Circuit diagram of GaN based four-level interleaved FCML totem-pole PFC converter.

The work in [11] demonstrated a seven-level FCML boost PFC with 12 GaN switches, each of 100V voltage rating. The FCML totem-pole PFC converter gathers the positive attributes of both these converters to achieve high efficiency and power density. This section briefly discusses the operation principle of the FCML PFC converter.

A. OPERATING PRINCIPLE

As seen from Fig. 1, the converter comprises two high switching frequency legs with a relatively low voltage i.e., 200 V GaN FETs operating at 100 kHz and a line frequency leg with 650V GaN devices. During positive half-line cycle, S2 is always ON, and the equivalent circuit is a low side linked FCML boost converter. In this state, Q1b, Q2b, and Q3b are the active switches alternatively, while Q1a, Q2a, and Q3a act as synchronous rectifier (SR) switches. During negative half-line cycle, S1 is always ON, and Q1a, Q2a, and Q3a are the active switches alternatively, while Q1b, Q2b, and Q3b are SR switches. In both the positive and negative half-cycles, the converter operates as a four-level FCML Boost converter. The control signals for Q1a, Q2a, and Q3a share the same duty cycle profiles with a mutual phase-shift of 120^o angle apart. To implement this control strategy for driving the switches, the phase shift pulse width-modulation (PSPWM) is employed which has natural voltage balancing capability [19], [20], [21]. Similarly, the switching signals for Q1b, Q2b, and Q3b are obtained by negating the gate signals of Q1a, Q2a, and Q3a, respectively. Since a phase shift of 120^o is equivalent to a time shift of one third of the switching period, the four-level boost converter changes its switching sequence whenever the duty cycle (D) crosses the levels of 1/3 and 2/3, which is illustrated in Fig. 2. It can be inferred that each half-line cycle will get divided into three segments where duty cycle varies between 0 to 1/3, 1/3 to 2/3, and 2/3 to 1. Similarly, the 2nd high frequency leg switching devices are split into 3 pairs of switches including (Q ′ 1a, Q ′ 1b), (Q ′ 2a, Q ′ 2b), and (Q ′ 3a, Q ′ 3b). Each arrangement of paired switches is operated in a complementary manner. The low side switches Q ′ 1b, Q ′ 2b and Q ′ 3b share the same duty ratio D and switching frequency with 120^0 phase shift apart. However, the difference in driving pulses of the 2nd phase switches (Q ′ 1a to Q ′ 3b) with respect to the 1st phase switching devices (Q1a to Q3b) is that each of them are 60^0 phase-shift apart i.e., the rising edge of the gates signal Q ′ 1b will lag Q1b by one-sixth of the switching period. In a complete switching cycle of the two-stage interleaved four-level FCML PFC converter, there exists a maximum of 12 different switching states possible for the AC input current. The eight possible switching sequences that occur in each of the high frequency legs when the converter completes one-half of the line cycle are depicted in Table 1.

TABLE 1. Switching States of Interleaved FCML PFC

Q_{1b}/Q'_{1b}	Q_{2b}/Q'_{2b}	Q_{3b}/Q'_{3b}	C_1	C_2	$V_{SW1,2}$
0	0	0	NC	NC	V_o
0	0	1	-	NC	V_o- V_{c1}
0	1	0	+	-	V_o-V_{c2}+V_{c1}
1	0	0	NC	+	V_{c2}
1	0	1	-	+	V_{c2}-V_{c1}
1	1	0	+	NC	V_{c1}
0	1	1	NC	-	V_o-V_{c2}
1	1	1	NC	NC	0

Here '1' represents the device to be ON and '0' refers OFF state. The switching node voltage at the center of the high frequency legs V_{SW1} and V_{SW2} determine the slope of the AC input current i_{ac} flowing through the two inductors.

Here '1' represents the device to be ON and '0' refers OFF state. The switching node voltage at the center of the high frequency legs V_{SW1} and V_{SW2} determine the slope of the AC input current i_{ac} flowing through the two inductors.

$$\frac{d\,(i_{ac})}{dt} = \frac{2V_{ac} - (V_{SW1} + V_{SW2})}{L} \tag{1}$$

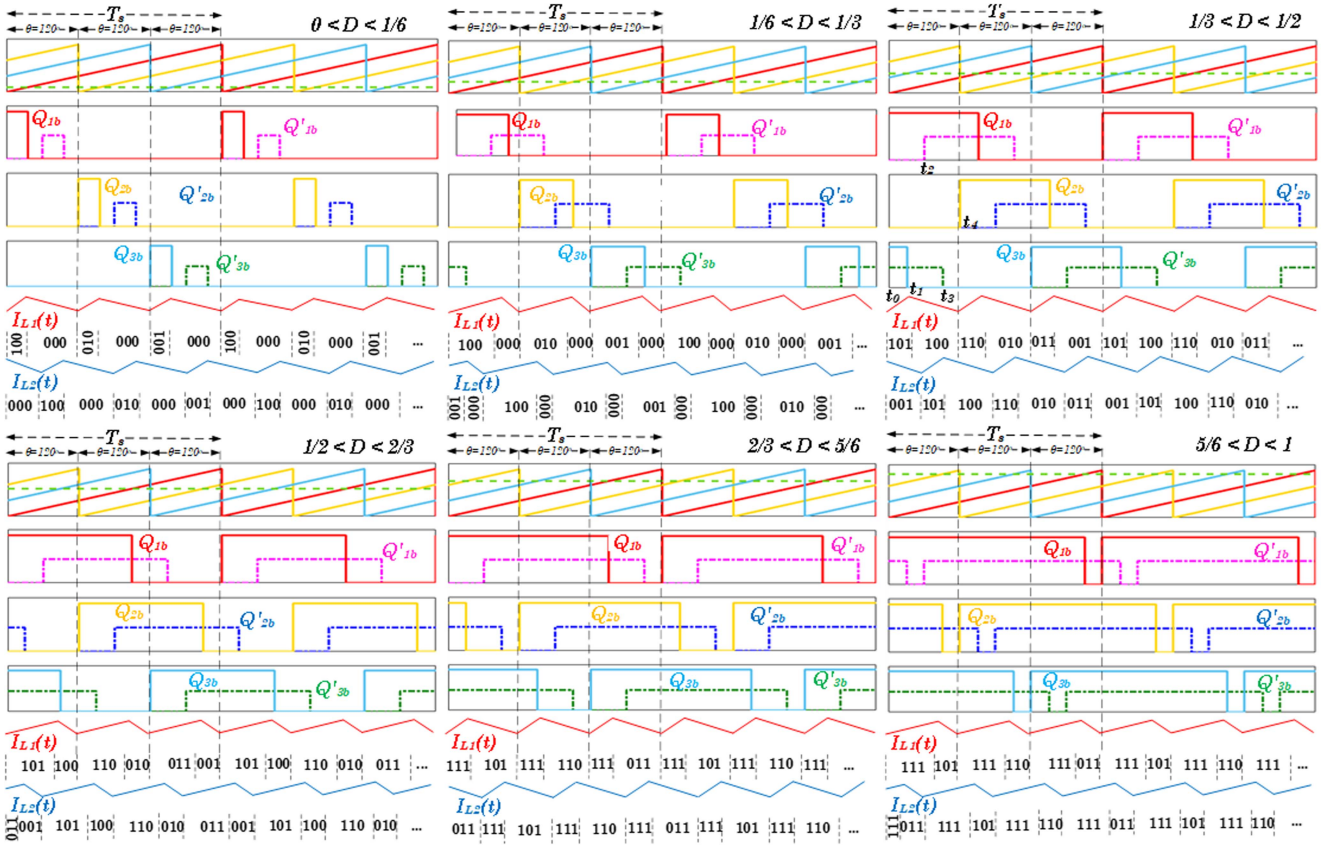

FIGURE 2. Four-level interleaved FCML PFC Gate signals and inductor current. (a) 0 < D < 1/6. (b) 1/6 < D < 1/3. (c) 1/3 < D < 1/2. (d) 1/2 < D < 2/3. (e) 2/3 < D < 5/6. (f) 5/6 < D < 1.

To elucidate the switching operation of the interleaved FCML PFC converter, the operating stages at duty cycle 1/3 < D < 1/2 for a duration of $T_s/3$ seconds are depicted in Fig. 3.

1) t_0 to t_1 [(Q_{1b} Q_{2b} Q_{3b}) = (101) and (M_{1b} M_{2b} M_{3b}) = (010)]: During this stage, the flying capacitors $\boldsymbol{C}_{11}$ and $\boldsymbol{C}_{22}$ discharge whereas capacitors $\boldsymbol{C}_{12}$ and $\boldsymbol{C}_{21}$ are charged through the path formed by the corresponding switching sequence. The slopes for current $\boldsymbol{I}_{L1}$ and $\boldsymbol{I}_{L2}$ are positive and negative, respectively, with a duration of $(\boldsymbol{D} - 1/3)\boldsymbol{T}_s$. The input current slope during this interval can be determined as,

$$\Delta i_{ac} = \frac{2V_{ac} - (V_{c12} - V_{c11} + V_o - V_{c22} + V_{c21})}{L} \times \left(D - \frac{1}{3}\right) T_s \tag{2}$$

2) t_1 to t_2 [(Q_{1b} Q_{2b} Q_{3b}) = (100) and (M_{1b} M_{2b} M_{3b}) = (010)]: During this stage, the flying capacitors $\boldsymbol{C}_{11}$ and $\boldsymbol{C}_{22}$ discharge whereas only capacitor $\boldsymbol{C}_{12}$ is charged through the path formed by the corresponding switching sequence. The slopes for both current $\boldsymbol{I}_{L1}$ and $\boldsymbol{I}_{L2}$ are negative with a duration of $(0.5 - \boldsymbol{D})\boldsymbol{T}_s$. The input current slope during this interval can be determined as,

$$\Delta i_{ac} = \frac{2V_{ac} - (V_{c12} + V_o - V_{c22} + V_{c21})}{L} (0.5 - D)\, T_s \tag{3}$$

3) t_2 to t_3 [(Q_{1b} Q_{2b} Q_{3b}) = (100) and (M_{1b} M_{2b} M_{3b}) = (011)]: During this stage, the flying capacitors $\boldsymbol{C}_{12}$ and $\boldsymbol{C}_{22}$ charges and discharges, respectively. The slopes for current $\boldsymbol{I}_{L1}$ and $\boldsymbol{I}_{L2}$ are negative and positive respectively with a duration of $(\boldsymbol{D} - 1/3)\boldsymbol{T}_s$. The input current slope during this interval can be determined as,

$$\Delta i_{ac} = \frac{2V_{ac} - (V_{c12} + V_o - V_{c22})}{L} \left(D - \frac{1}{3}\right) T_s \tag{4}$$

4) t_3 to t_4 [(Q_{1b} Q_{2b} Q_{3b}) = (100) and (M_{1b} M_{2b} M_{3b}) = (001)]: During this stage the flying capacitors $\boldsymbol{C}_{12}$ and $\boldsymbol{C}_{21}$ charges and discharges, respectively. The slopes for both current $\boldsymbol{I}_{L1}$ and $\boldsymbol{I}_{L2}$ are negative with a duration of $(0.5 - \boldsymbol{D})\boldsymbol{T}_s$. The input current slope during this interval can be determined as,

$$\Delta i_{ac} = \frac{2V_{ac} - (V_{c12} + V_o - V_{c21})}{L} (0.5 - D)\, T_s \tag{5}$$

B. CONTROL STRATEGY

The control block diagram of the interleaved FCML totem-pole PFC converter is shown in Fig. 4. It is made up of an

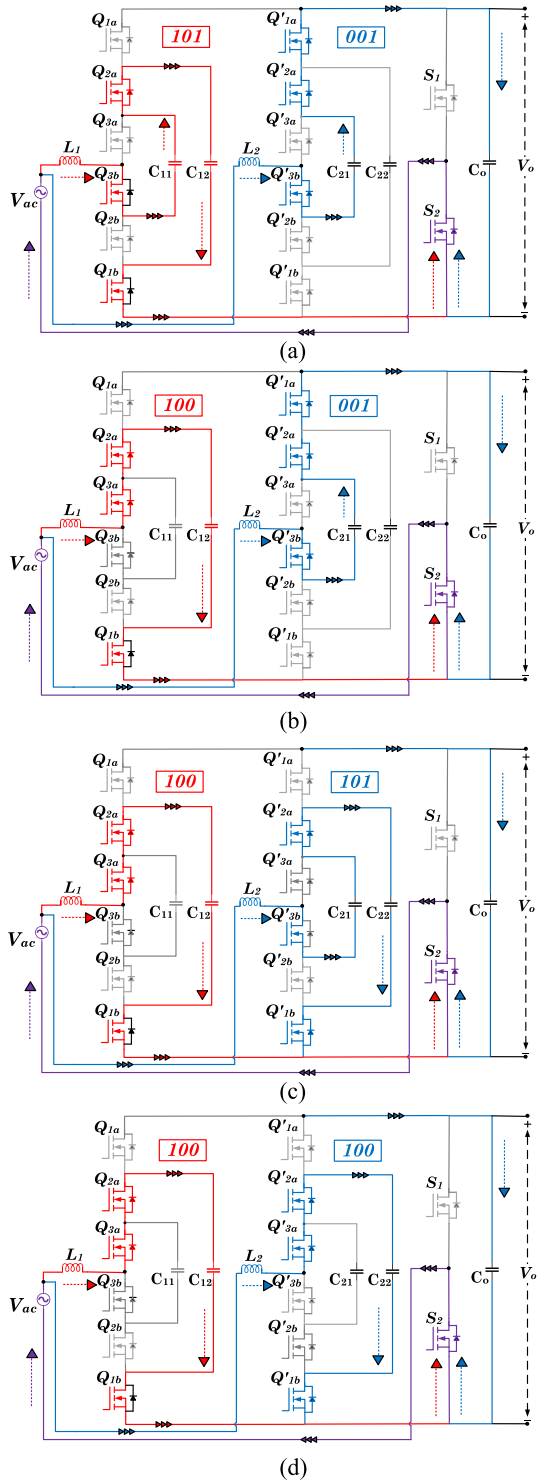

FIGURE 3. Operating stages two-stage interleaved FCML PFC converter. (a) $t_0 \sim t_1$, (b) $t_1 \sim t_2$, (c) $t_2 \sim t_3$, (d) $t_3 \sim t_4$.

outer DC link voltage loop, an inner inductor current loop, and a voltage feedforward control. The bandwidths of the voltage and current loops are set around three orders of magnitude apart to restrict their interaction so that the voltage loop perceives the current loop as an ideal current source. After sensing the input ac-line voltage V_{AC}, the phase-locked-loop (PLL) is employed to produce the sinusoidal ac-line current reference. The dc-link voltage (Vdc) sensor output is feed through a proportional integral (PI) controller to generate the magnitude of ac-line current reference. The inductor current of each interleaved phase (I_{L1} and I_{L2}) is individually sampled and controlled through a type-II current loop compensator to shape a sinusoidal inductor current. Here, the individual inductor currents, rather than the ac-line current, are regulated to ensure equal current sharing in two interleaved phases. The step change in the initial duty cycle D hampers the dynamic response of the input inductor current at zero crossing of the input voltage. Adding the feedforward term with the current compensator output facilitates the step change in the duty cycle during the zero crossing because such a control loop modification aids towards large signal stability. With this, the zero-crossing distortion of the inductor current can be improved leading to a near-unity power factor. Two duty cycle outputs are then used by the Phase-shift PWM block to generate the PWM signals of the FCML leg switches with 120^0 phase-shift. However, the triangular high frequency carrier signals in the PSPWM block for the 2nd interleaved phase have an additional 60^o phase shift to generate the gate signals Q'_{1a} to Q'_{3b}.

C. NATURAL VOLTAGE BALANCING CAPABILITY

By assuming the converter is operating in CCM with negligible voltage ripples across the capacitors, the DC analysis is done for D < 1/3 condition. The input voltage V_{ac} is considered constant over a switching cycle ($T_s \ll T_{\text{cycle}}$). Applying Voltage-second balance principle to the inductor gives,

$$\int_0^{T_s} (V_{ac} - V_{sw})\, dt = 0 \tag{6}$$

By substituting the switching node voltage V_{SW} value from Table 1, the above equation turns the following.

$$V_{sw} = DV_{c2} + 3\left(\frac{1}{3} - D\right)V_o + D\,(V_o - V_{c2} + V_{c1}) + D\,(V_o - V_{c1}) = V_o\,(1 - D) \tag{7}$$

Hence, the duty cycle D can be expressed as,

$$D = \begin{cases} 1 - \frac{V_{in}}{V_{out}} & V_{in} > 0 \\ \frac{V_{in}}{V_{out}} & V_{in} < 0 \end{cases} \tag{8}$$

From charge balance of flying capacitor C_{11}, $\int_0^{T_s} i_{c1}(t)dt = 0$. The inductor current charges the flying capacitor C_{11} during the '010' switching state and discharges it at '001' switching mode. Since the input voltage is assumed to be constant in a switching cycle, the inductor switching ripple depends upon the switching node voltage V_{SW}. For holding the capacitor charge balance equation, these ripples must be equal. Hence the V_{SW} at these two intervals are equal.

$$V_{c12} - V_{c11} = V_{c11} \tag{9}$$

$$V_o - 2V_{c12} + V_{c11} = 0 \tag{10}$$

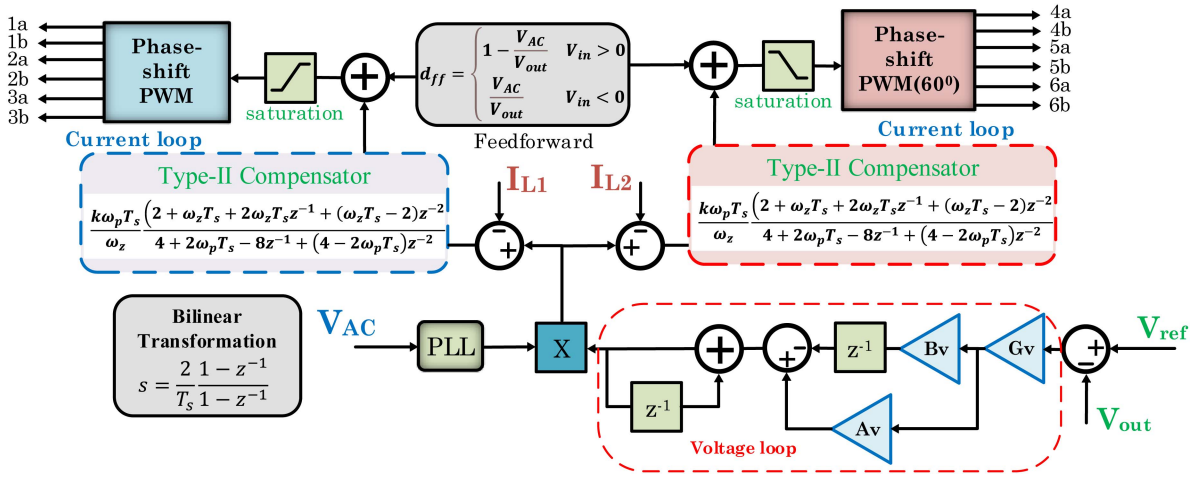

FIGURE 4. Control block diagram of GaN based two-stage interleaved FCML PFC converter.

Combining (9) and (10), the natural voltage balancing capability of the FCML converter can be verified, $V_{c11}=\frac{V_o}{3}$ and $V_{c12}=\frac{2V_o}{3}$. Similarly, the secondary leg flying capacitors C_{21} and C_{22} also maintain one-third and two-third of the output voltage due to natural voltage balancing capability. While the natural balancing capability of the flying capacitors are ensured by the PSPWM technique, a symmetrical layout is vital for this converter because the gate signal propagation delay mismatch in half-bridge gate drivers can lead to capacitor voltage imbalance [19]. Moreover, applications requiring fast start-up time may require additional control loops for regulating the flying capacitors voltages at desired levels. Nevertheless, once the converter achieves the steady state, the voltages across flying capacitors will become naturally balanced.

III. BOOST INDUCTOR-EMI FILTER CO-OPTIMIZATION AND ITS IMPACT ON EMI PERFORMANCE

In this section, the co-optimization of the EMI filter and boost inductor with respect to volume is evaluated considering the DM noise level complies with the FCC Class A EMI standards. The DM filter design for the PFC converters is dependent upon the selection of LC product to achieve the required attenuation level at a certain design frequency. In addition, the selection of the boost inductor determines the required attenuation level, and the attenuation requirement can be fulfilled by numerous other possible combinations of L_{DM} and C_{DM} having the same LC product. Hence, co-optimization of the boost inductor, DM filter inductor and capacitor is required to minimize the volume as the AC-side passive components contribute a major part of the volume of a PFC converter. This section focuses on the optimal design of the AC-side passive components based on the required attenuation level obtained from the input current FFT model of the PFC topologies.

A. GENERALIZED INPUT CURRENT FFT MODEL FOR CONSTANT SWITCHING FREQUENCY CCM PFC TOPOLOGIES

One common thing for the continuous conduction mode (CCM) totem-pole PFC, non-interleaved FCML PFC converter and interleaved FCML PFC is that the switching frequency remains fixed but the duty cycle changes depending upon the applied input voltage. The input current is not a perfect sinusoid and includes ripple current which has frequency components of the switching frequency and its multiples. During the k^{th} switching cycle with switching period T_s, the triangular inductor current $f_+(t)$ and $f_-(t)$ during time interval D_kT_s and $(1-D_k)T_s$, respectively. can be expressed as follows,

$$f_+(t)=\frac{\Delta i_{ripple,k}}{D_kT_s}t+\left(i_k-\frac{(k-1+D_k)}{D_k}\Delta i_{ripple,k}\right) \quad (11)$$

$$f_-(t)=-\frac{\Delta i_{ripple,k}}{(1-D_k)T_s}t+\left(i_k+\frac{(k-1+D_k)}{(1-D_k)}\Delta i_{ripple,k}\right) \quad (12)$$

where D_k and $\Delta i_{ripple,k}$ are the duty cycle and switching current ripple at the k^{th} switching cycle. The inductor current can be represented by the sum of triangular current waveform $f(t)$ at each switching cycle. The Fourier coefficients can be determined from the input inductor current from which the FFT of the input inductor current is developed.

$$a_n=\frac{4}{T}\sum_{k=1}^{T/T_s}\left[\int_{(k-1)T_s}^{(k-1+D_k)T_s}f_+(t)\cos(n\omega_o t)+\int_{(k-1+D_k)T_s}^{kT_s}f_-(t)\cos(n\omega_o t)\right] \quad (13)$$

$$b_n=\frac{4}{T}\sum_{k=1}^{T/T_s}\left[\int_{(k-1)T_s}^{(k-1+D_k)T_s}f_+(t)\sin(n\omega_o t)\right.$$

TABLE 2. Peak-to-Peak Input Current Ripple for PFC Topologies

Duty Cycle, D	Peak to peak Input Current Ripple, $\Delta I_{L,pk-pk}$		
	Totem-pole PFC	Non-interleaved 4-level FCML PFC	4-level FCML Interleaved PFC
$\frac{5}{6} < D < 1$	$\frac{V_{in} D T_s}{L}$	$\frac{V_{in}\left(D-\frac{2}{3}\right)T_s}{L}$	$\frac{2V_{in}\left(D-\frac{5}{6}\right)T_s}{L}$
$\frac{2}{3} < D < \frac{5}{6}$			$\frac{2\left(\frac{V_o}{3}-V_{in}\right)\left(\frac{5}{6}-D\right)T_s}{L}$
$\frac{1}{2} < D < \frac{2}{3}$		$\frac{\left(V_{in}-\frac{V_o}{3}\right)\left(D-\frac{1}{3}\right)T_s}{L}$	$\frac{2\left(V_{in}-\frac{V_o}{3}\right)\left(D-\frac{1}{2}\right)T_s}{L}$
$\frac{1}{3} < D < \frac{1}{2}$			$\frac{2\left(\frac{2V_o}{3}-V_{in}\right)\left(\frac{1}{2}-D\right)T_s}{L}$
$\frac{1}{6} < D < \frac{1}{3}$		$\frac{\left(V_{in}-\frac{2V_o}{3}\right)DT_s}{L}$	$\frac{2\left(V_{in}-\frac{2V_o}{3}\right)\left(D-\frac{1}{6}\right)T_s}{L}$
$0 < D < \frac{1}{6}$			$\frac{2(V_o-V_{in})\left(\frac{1}{6}-D\right)T_s}{L}$

$$+\int_{(k-1+D_k)T_s}^{kT_s} f_{-}(t)\sin(n\omega_o t)\Bigg] \tag{14}$$

These expressions can be further expanded to find the Fourier coefficients a_n and b_n as shown in (15) and (16) shown at the bottom of this page, where n is the harmonic order and T is the line period, the input current EMI spectrum of the PFC converters can be obtained. The magnitude of the EMI spectrum for each harmonic is obtained by, $c_n = \sqrt{a_n^2 + b_n^2}$.

B. INPUT CURRENT SPECTRUM ANALYSIS OF PFC CONVERTERS

In order to compute the input current FFT model for a particular PFC topology, the peak-to-peak ripple current over the line cycle is first determined. The current ripple frequency of the four-level GaN totem-pole PFC is three times the switching frequency. Thus, the inductor size of the four-level CCM GaN totem-pole PFC should be much smaller than the inductor size of the two-level GaN totem-pole PFC under the same switching frequency condition. On the other hand, due to two-stage interleaving, the interleaved FCML PFC input current ripple frequency is six times the switching frequency. Table 2 illustrates the peak-to-peak input current ripple of the above three topologies for various duty cycle range. It can be observed that the non-interleaved FCML current ripple goes down to zero at D = 1/3 and 2/3. However, the interleaved FCML PFC peak-to-peak ripple current becomes zero at D = 1/6, 1/3, 1/2, 2/3 and 5/6. Fig. 5 shows and compares the peak-to-peak current ripples of the totem-pole PFC, four level single phase FCML PFC and the four-level interleaved FCML PFC over a half-line-cycle. In this ripple comparison, the switching frequency of the four-level PFC is 100 kHz, while the ripple frequency is 300 kHz. The switching frequency of the four-level interleaved FCML PFC is also 100 kHz, while the grid current exhibits a ripple frequency of twice the phase current ripple frequency, i.e., 600 kHz. The test conditions include the ac voltage of 240 Vac, output voltage of 400 V dc, and the load power of 2500 W. As shown in Fig. 5, even though the inductance value of the two-level PFC is five times of that in an FCML PFC, the inductor current ripple value of the two-level PFC is still much higher than the inductor current ripple value of the four-level non-interleaved FCML PFC while the interleaved FCML has nearly half the ripple.

$$\begin{aligned} a_n = \frac{4}{T}\sum_{k=1}^{T/T_s}\Bigg[& \frac{\Delta i_{ripple,k}}{D_k T_s}\left(\frac{(k-1)T_s\sin((k-1)n\omega_o T_s)-((k-1+D_k)T_s)\sin(n\omega_o(k-1+D_k)T_s))}{n\omega_o}\right) \\ & +\frac{(\cos(n\omega_o(k-1+D_k)T_s)-\cos(n\omega_o(k-1)T_s)}{n^2\omega_o^2} - \left(i_k - \frac{(k-1+D_k)}{D_k}\Delta i_{ripple,k}\right)\left(\frac{\sin((k-1)n\omega_o T_s)-\sin(n\omega_o(k-1+D_k)T_s))}{n\omega_o}\right) - \frac{\Delta i_{ripple,k}}{(1-D_k)T_s} \\ & \times\left(\frac{(k-1+D_k)T_s\sin(n\omega_o(k-1+D_k)T_s)-kT_s\sin(n\omega_o kT_s)}{n\omega_o} + \frac{(\cos(n\omega_o kT_s)-\cos(n\omega_o(k-1+D_k)T_s)}{n^2\omega_o^2}\right) \\ & +\left(i_k + \frac{(k-1+D_k)}{1-D_k}\Delta i_{ripple,k}\right)\left(\frac{\sin(n\omega_o(k-1+D_k)T_s)-\sin(n\omega_o kT_s)}{n\omega_o}\right)\Bigg] \end{aligned} \tag{15}$$

$$\begin{aligned} b_n = \frac{4}{T}\sum_{k=1}^{T/T_s}\Bigg[& \frac{\Delta i_{ripple,k}}{D_k T_s}\left(\frac{(k-1)T_s\cos((k-1)n\omega_o T_s)-((k-1+D_k)T_s)\cos(n\omega_o(k-1+D_k)T_s))}{n\omega_o}\right) + \frac{(\sin(n\omega_o(k-1+D_k)T_s)-\sin(n\omega_o(k-1)T_s)}{n^2\omega_o^2} \\ & -\left(i_k - \frac{(k-1+D_k)}{D_k}\Delta i_{ripple,k}\right)\left(\frac{\cos((k-1)n\omega_o T_s)-\cos(n\omega_o(k-1+D_k)T_s))}{n\omega_o}\right) - \frac{\Delta i_{ripple,k}}{(1-D_k)T_s} \\ & \times\left(\frac{(k-1+D_k)T_s\cos(n\omega_o(k-1+D_k)T_s)-kT_s\cos(n\omega_o kT_s)}{n\omega_o} + \frac{(\sin(n\omega_o kT_s)-\sin(n\omega_o(k-1+D_k)T_s)}{n^2\omega_o^2}\right) \\ & +\left(i_k + \frac{(k-1+D_k)}{1-D_k}\Delta i_{ripple,k}\right)\left(\frac{\cos(n\omega_o(k-1+D_k)T_s)-\cos(n\omega_o kT_s)}{n\omega_o}\right)\Bigg] \end{aligned} \tag{16}$$

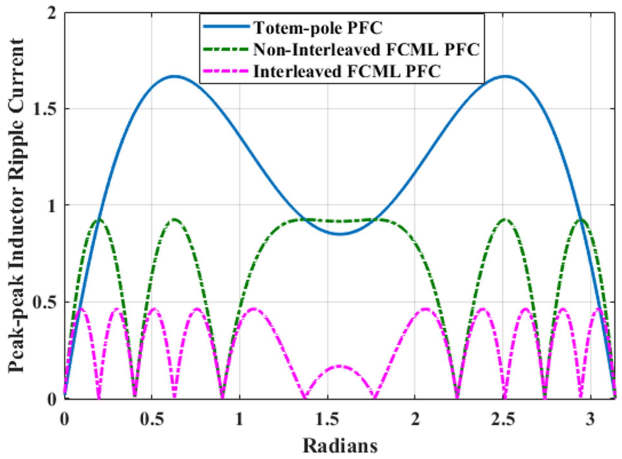

FIGURE 5. Comparison of peak-to-peak ripple current between totem-pole PFC, FCML PFC and Interleaved FCML PFC.

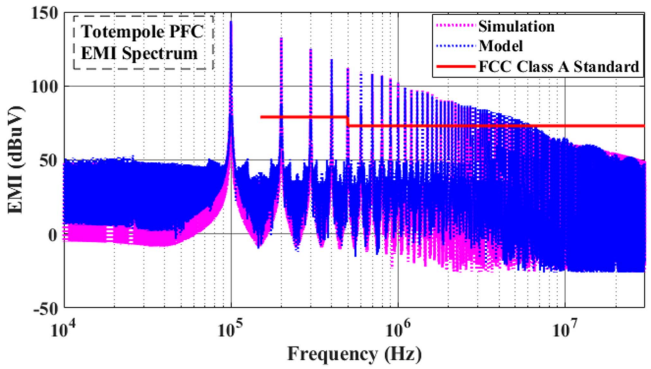

FIGURE 6. EMI spectrum for 500 uH boost inductor CCM Totem-pole PFC converter.

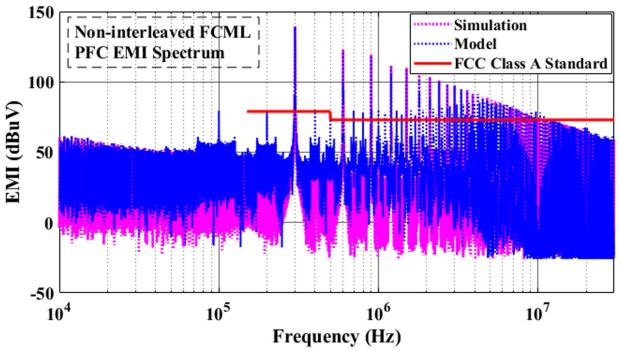

FIGURE 7. EMI spectrum for 100 uH boost inductor non-interleaved FCML PFC converter.

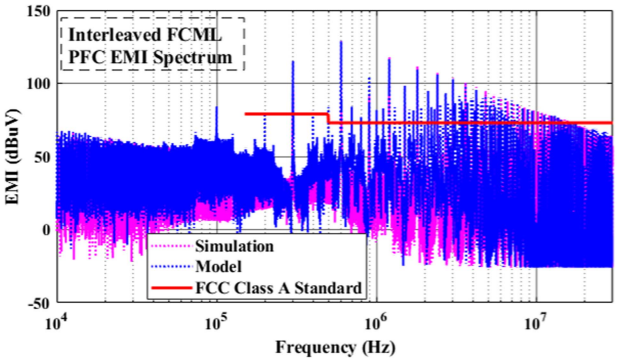

FIGURE 8. EMI spectrum for 100 uH boost inductor Interleaved FCML PFC converter.

To verify the accuracy of the EMI spectrum obtained from the model, the simulated EMI spectrum of the three topologies is compared against the model outcomes. The current spectrum for the CCM totem pole PFC converter has frequency components at fixed intervals due to its fixed frequency operation. The EMI spectrum of the input inductor current of the CCM totem-pole PFC converter operating at 100 kHz switching frequency is illustrated in Fig. 6. The input current constitutes of the line frequency component (60 Hz) and the switching frequency component and its multiple. Since the second switching harmonic component falls in the EMI spectrum, the attenuation requirement for designing the EMI filter is based upon the switching harmonic current amplitude at 200 kHz.

The EMI spectrums for the single phase FCML totem-pole PFC and interleaved FCML totem-pole PFC converter would vary due to the difference in peak-to-peak ripple frequency behavior over half the line cycle. The EMI spectrum of the input current of these converters operating at 100 kHz switching frequency is illustrated in Figs. 7 and 8. For the non-interleaved FCML PFC, the 3rd switching harmonic component falls in the EMI spectrum which implies the attenuation requirement designing the EMI filter is based upon the switching harmonic current amplitude at 300 kHz. Consequently, the interleaved FCML PFC input current EMI spectrum peaks at 600 kHz. The mathematical model of all the three topologies derived from the Fourier analysis (blue) closely match with the simulated EMI spectrum (pink) with almost no error in the spectrum peak amplitudes and frequencies. Moreover, relatively small EMI peaks also occur at 100 kHz and 300 kHz frequencies and their harmonics. The harmonics are present mainly due to the voltage ripples present in the flying capacitor and output capacitor due to 100 kHz switching frequency. To explain this phenomenon the input current slope near the peak, where the duty cycle ranges from 0 to 1/6 is shown in Table 3. It can be inferred that the switching state 1, 5 and 9 would have the same slope if the flying capacitor voltages (C_{11}, C_{21}) and (C_{12}, C_{22}) for the 4-level interleaved FCML PFC are exactly $V_{out}/3$ and $2V_{out}/3$ respectively. Due to the presence of the voltage ripple in these capacitors, slightly unequal input current slopes occur in these intervals that result in the 300 kHz component in the EMI spectrum. Similar phenomena also occur in other duty cycle ranges.

TABLE 3. Input Current Slopes During 0 < D < 1/6

Switching Interval/State	Input current slope
1 (100/000)	$\frac{(2V_{in}-V_{c2}-V_{out})}{L}$
2 (000/000)	$\frac{2(V_{in}-V_{out})}{L}$
3 (000/100)	$\frac{(2V_{in}-V_{c2}-V_{out})}{L}$
4 (000/000)	$\frac{2(V_{in}-V_{out})}{L}$
5 (010/000)	$\frac{(2V_{in}+V_{c2}-V_{c1}-2V_{out})}{L}$
6 (000/000)	$\frac{2(V_{in}-V_{out})}{L}$
7 (000/010)	$\frac{(2V_{in}+V_{c2}-V_{c1}-2V_{out})}{L}$
8 (000/000)	$\frac{2(V_{in}-V_{out})}{L}$
9 (001/000)	$\frac{(2V_{in}+V_{c1}-2V_{out})}{L}$
10 (000/000)	$\frac{2(V_{in}-V_{out})}{L}$
11 (000/001)	$\frac{(2V_{in}+V_{c1}-2V_{out})}{L}$
12 (000/000)	$\frac{2(V_{in}-V_{out})}{L}$

C. BOOST INDUCTOR-EMI FILTER VOLUME CO-OPTIMIZATION

In this section, the performance of the EMI filter with respect to volume is evaluated considering that the DM noise level complies with the EMI standards. The DM filter design for the PFC converter is based upon the selection of LC product to achieve the required attenuation level at a certain design frequency. But the attenuation requirement can be fulfilled by numerous other possible combinations of L_D and C_D having the same LC product. This section discusses the selection of optimum L_{DM} and C_{DM} values to minimize the DM filter volume as DM EMI filter contributes a major part of the volume of a PFC converter. For determining the total volume of the DM EMI filter, the individual DM inductor and capacitor volume need to be estimated. The filter capacitor volumetric cost function is developed using a regression model used in [22], [23] that utilize the rated voltage V, capacitance C and stored energy CV^2. The capacitor volume can be approximated as,

$$V_c = K_c C + K_c^{'} V + K_c^{''} C V^2 \tag{17}$$

The estimated capacitor volume is based on the X2 film capacitors datasheet. A second order regression model is developed to get the coefficients K_c, K_c' and K_c'' which can accurately fit the actual volume data points for a given capacitance and rated voltage. Similar to this, a model is also used to estimate the volume of inductors with toroidal cores. The filter inductor volume is proportional the stored inductive energy, $V_L \propto K_L L I^2$. Where K_L is the proportionality between the stored energy and the inductor volume. Manufacturer information for various inductor core dimensions, inductance values, and current ratings can be used to compute this factor. Thus, the filter inductor volume can be approximated as,

$$V_L = K_L L + K_L^{'} I + K_L^{''} L I^2 \tag{18}$$

As a result, the optimum DM EMI filter utilizing the filter inductor and capacitor coefficients can be obtained by minimizing the total volume of the DM filter expressed as,

$$V_{tot} = \underbrace{k_{C_{DM}} + k_{C_{DM}}^{'} V + k_{C_{DM}}^{''} V^2}_{V_{C_{DM}}} + \underbrace{k_{L_{DM}} + k_{L_{DM}}^{'} V + k_{L_{DM}}^{''} V^2}_{V_{L_{DM}}} + \underbrace{k_L + k_L^{'} V + k_L^{''} V^2}_{V_L} \tag{19}$$

where V_{CDM}, V_{LDM} and V_L are the volumes of C_{DM}, L_{DM} and L, respectively, which can be expressed similarly as done in (10) and (11). The DM filter design with N_f filter stages for the PFC converter is based upon the selection of LC product to achieve the required attenuation level at a certain design frequency f_D. Fig. 9 shows the attenuation requirement with respect to the boost inductor L. and switching frequency f_s for the three PFC topologies of interest. By using a multivariate non-linear regression model, the attenuation requirement as a function of L and f_s can be formulated. To attain minimum filter volume, V_{tot} is to be minimized with a constraint of the required level of attenuation as shown,

$$Att_{DM} = (2\pi f_D)^{2N_f} ((L_{DM} C_{DM})^{N_f} = b_1 + b_2 L + b_3 f_s + b_4 L f_s \tag{20}$$

Here, b_1, b_2, b_3, and b_4 denote the coefficients of the regression model and are determined by the principle of least squares. Here, boost inductor L and switching frequency f_s notations are replaced by x_1 and x_2 respectively. The least square estimates of $b_1 \sim b_4$ for n number of Att_{DM} measurements are then found by taking partial derivatives $\frac{\partial S}{\partial b_{1\sim4}}$ and equating them to zero, where

$$S = \sum_{i=1}^{n} (y_i - b_1 + b_2 x_{1i} + b_3 x_{2i} + b_4 x_{1i} x_{2i})^2.$$

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} n & \sum x_1 & \sum x_2 & \sum x_1 x_2 \\ \sum x_1 & \sum x_1^2 & \sum x_1 x_2 & \sum x_1^2 x_2 \\ \sum x_2 & \sum x_1 x_2 & \sum x_2^2 & \sum x_1 x_2^2 \\ \sum x_1 x_2 & \sum x_1^2 x_2 & \sum x_1 x_2^2 & \sum x_1^2 x_2^2 \end{bmatrix}^{-1} \times \begin{bmatrix} \sum y \\ \sum x_1 y \\ \sum x_2 y \\ \sum x_1 x_2 y \end{bmatrix} \tag{21}$$

From the device loss perspective, the switching frequency selection is crucial as it accounts for the switching loss and device CV^2 loss. Excluding the switching frequency in the objective function results in a lower AC-side passive volume as the switching frequency can be increased by any limit. But higher switching frequency causes the converter efficiency to degrade owing to higher switching losses. Hence, the objective function includes the volume of the AC-side passive components (L, L_{DM} and C_{DM}) as well as the switching frequency dependent losses. The optimization objective function consolidates the volume- and loss-related information in a

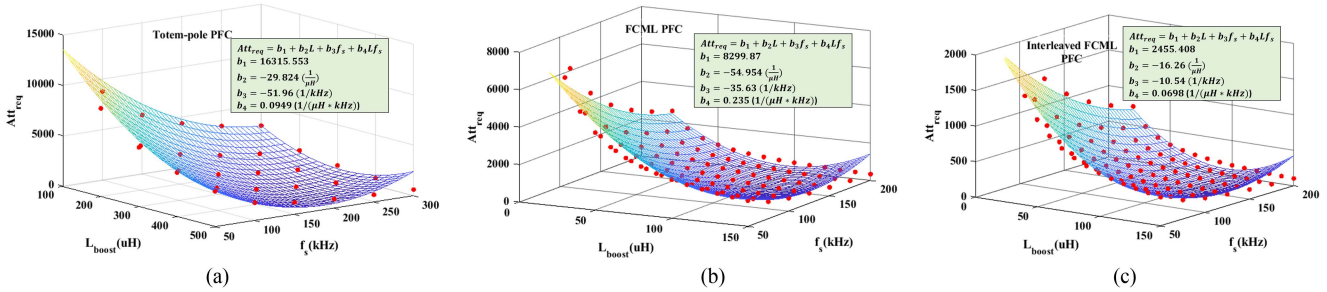

FIGURE 9. DM EMI filter attenuation requirement of (a) totem-pole PFC, (b) Non-interleaved FCML PFC and (c) Interleaved FCML PFC.

TABLE 4. Coefficients for Co-optimization of PFC Topologies

Topology	Coefficients for Att_{req}				Coefficients for Inductor Volume		Coefficients for Capacitor Volume	
	const	L	f_s	Lf_s				
Totem-pole PFC	16315.5	-29.824	-51.96	0.0949	K_L	$0.91 cm^3/mH$	K_C	$2.18\ cm^3/\mu F$
Non-interleaved FCML PFC	8299.87	-54.954	-35.63	0.235	K'_L	$0.38\ cm^3/A$	K'_C	3e-3 cm^3/V
FCML Interleaved PFC	2455.4	-16.26	-10.54	0.0698	K''_L	$0.237\ cm^3/(mH.A^2)$	K''_C	4.6e-5 $cm^3/(\mu F.V^2)$

unit-less representation through proper normalization, as follows in equation (22),

$$F = \frac{V_{tot}}{\alpha Vol} + \frac{\gamma f_s}{\beta P_{out}} \tag{22}$$

F is the sum of normalized filter volume and normalized switching frequency-related loss. The objective function F is constructed in a way that minimizing this would ensure a co-optimization of passives volume and converter efficiency. Both of the terms have been normalized and weighted equally to put equal emphasis on the AC-side passive volume and the switching frequency dependent losses.

The terms α and β are constants that represent the fraction of the total volume of the converter and fraction of the converter output power, respectively. α is a unit-less quantity, where αVol is the targeted fraction of the total volume of the power converter taken by the DM EMI filter and boost inductor. Since practical filter implementations typically comprises of ∼30% of the total volume of a power converter [24], $\alpha = 0.3$ was selected as a benchmark for all the three PFC topologies. In addition, β, which is also a unit-less quantity, is the fraction of the total converter output power, appearing as the switching frequency related loss. In this article, $\beta = 0.008$ is selected based upon two aspects, 1) use of GaN switches and 2) PFC topology operating in CCM mode at the rated voltage/power conversion (i.e., 240Vac to 400 V dc at 2.5 kW). It is important to note that, constant terms α and β are user defined parameters which can be altered depending upon the use of semiconductor technology, type of the converter, and test specifications to set the desired objective function. The term γfs in the numerator refers to the switching frequency related losses that are linearly proportional to the switching frequency. For minimizing (22) while satisfying the constraints given by (20), Lagrange multiplier method has been employed to find the optimized volume of the boost inductor, DM filter inductor and capacitor while keeping the switching loss under a desired level. Table 4 shows the necessary coefficients for solving the optimization function. The optimized AC-side passive parameters and switching frequency are formulated as,

$$f_s = \sqrt[3]{\frac{\frac{2(k_{L_{DM}} + k''_{L_{DM}} I^2)(k_{C_{DM}} + k''_{C_{DM}} V^2)}{\left(k_L + k''_L I^2\right)^2} \frac{b_2^2}{(2\pi)^2}}{b_3 - \frac{\gamma \alpha Vol\, b_2}{\beta P_{out}\left(k_L + k''_L I^2\right)}}} \tag{23}$$

$$C_{DM} = \frac{-b_2(k_{L_{DM}} + k''_{L_{DM}} I^2)}{\left(k_L + k''_L I^2\right)(2\pi f_s)^2} \tag{24}$$

$$L_{DM} = \frac{(k_{C_{DM}} + k''_{C_{DM}} V^2)}{(k_{L_{DM}} + k''_{L_{DM}} I^2)} C_{DM} \tag{25}$$

$$L = \frac{1}{b_2}\left[\frac{(k_{L_{DM}} + k''_{L_{DM}} I^2) \times (k_{C_{DM}} + k''_{C_{DM}} V^2)}{\left(k_L + k''_L I^2\right)^2} \frac{b_2^2}{(2\pi f_s)^2} - b_1 - b_3 f_s\right] \tag{26}$$

Fig. 10 illustrates the objective function F with respect to the DM filter parameters L_{DM} and C_{DM} for the three PFC topologies. It can be observed that the minimum objective function for the interleaved FCML PFC is the lowest with $F = 1.09$ (Fig. 10(c)). To elucidate the functionality of the co-optimization routine, the objective functions for three different switching frequencies (50 kHz, 94 kHz, and 150 kHz) are depicted and the switching frequency obtained from the (15) results in the minimum value of the objective function. The switching frequency candidates of 50 kHz and 150 kHz

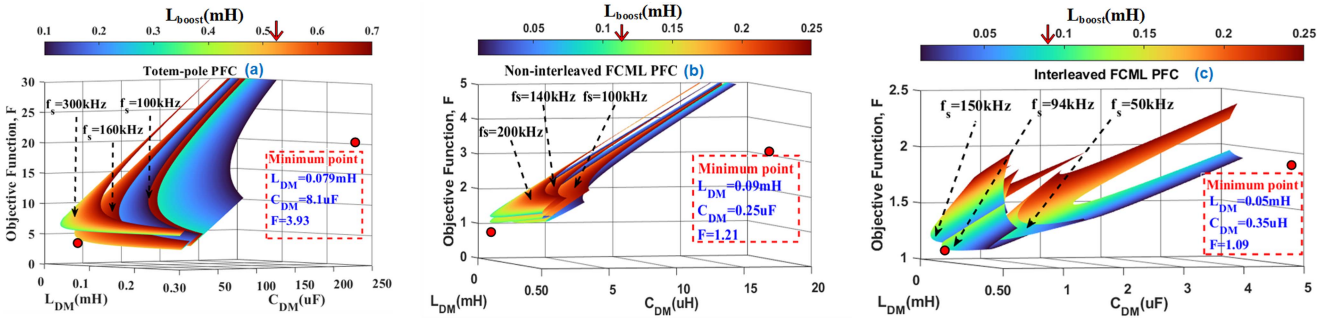

FIGURE 10. DM EMI filter volume and switching loss minimization of (a) totem-pole PFC, (b) non-interleaved FCML PFC, and (c) Interleaved FCML PFC.

TABLE 5. Co-optimized Parameters of PFC Topologies

Topology	L_{DM} μH	C_{DM} μF	L μH	f_s kHz	Total AC-side Passive volume (cm^3)	Switching related loss (W)
Totem-pole PFC	79	8.1	512	160	139.8	9.23
Non-interleaved FCML PFC	90	0.25	121	140	28.37	6.25
Interleaved FCML PFC	51.96	0.35	85	94	25.95	7.6

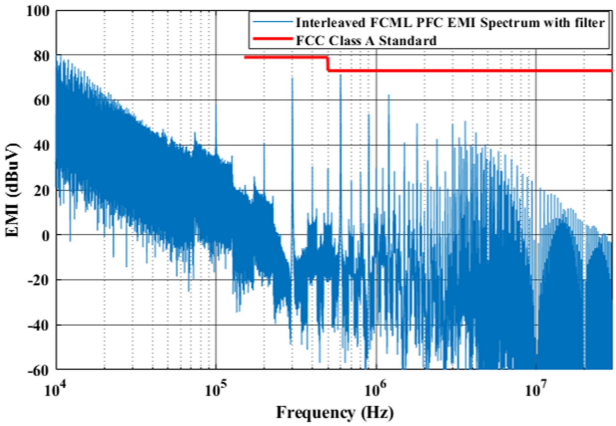

FIGURE 11. EMI spectrum of Interleaved FCML PFC converter with DM EMI filter.

TABLE 6. Co-optimized DM Filter Parameters of Interleaved FCML PFC for Multistage DM Filter.

No. of Stage	L_{DM} μH	C_{DM} μF	L μH	f_s kHz	Total AC-side Passive volume (cm^3)
N_f=1	51.96	0.35	85	94	25.95
N_f=2	22.13	0.11	73	147	29.7
N_f=3	13.67	0.05	66	170.3	35.63

are selected as benchmark for comparison since their third and first harmonics appear in the conducted EMI zone, while the second harmonic for the 94 kHz appears in the spectrum range. As can be seen in Fig. 10(a), the totem-pole PFC has the highest objective function value (F = 3.93) with the optimized switching frequency of 160 kHz. The adjacent plots for switching frequencies 100 kHz and 300 kHz are kept for comparison to illustrate that the optimum switching frequency results in the minimum value of *F*. The objective function for the non-interleaved FCML PFC falls between the two topologies discussed here with an optimized switching frequency of 140 kHz. Table 5 shows the optimized DM filter parameters, optimal boost inductance, and optimal switching frequency based on the Lagrange multiplier method applied on the three PFC topologies. Based on the results obtained from the optimization routine, it can be observed that even though the DM inductance for the totem-pole PFC is lower than that in other FCML topologies, the overall AC-side passive volume of the interleaved FCML PFC is the lowest.

The totem-pole PFC necessitates the highest boost inductor which results in the larger total passive volume. Since the effective boost inductor ripple frequency increases by three times and six times of the switching frequency in non-interleaved FCML PFC and two-phase interleaved FCML PFC converter respectively, the boost inductor size can be significantly reduced. Thus, the total volume of the AC-side passive components (boost inductor and DM EMI filter) can be minimized to satisfy the FCC Class A standard EMI spectrum requirements. The EMI spectrum of the interleaved FCML PFC with the optimal DM filter design is illustrated in Fig. 11.

To explore multistage DM EMI filters for interleaved FCML PFC, the L_{DM} and C_{DM} for the intermediate stages were considered equal and the attenuation requirement is shared equally by each individual stage. The optimization routine was again performed for $N_f = 2$ and $N_f = 3$ to determine the required filter parameters and boost inductor as depicted in Table 6. Because the objective function F includes both volume and switching-related losses, the increase in switching frequency is constrained to prevent excessive rises. As the design frequency of the interleaved FCML PFC converter is six times the switching frequency, the single stage filter can

achieve the required attenuation with smaller volume and simple structure. Furthermore, in practice, imperfect interleaving impacts the DM noise more significantly for multistage filters [25]. The filter corner frequency drops dramatically with the phase error for higher order filters which results in larger filter size. In addition, multistage filters are more likely to cause additional phase shift between the inductor current and grid current, worsening the power factor. Considering all these reasons, the single stage DM filter was used for this design.

IV. LOSS COMPARISON OF INTERLEAVED FCML PFC CONVERTER WITH OTHER PFC COUNTERPARTS

The CCM operated totem-pole PFC has a large inductor size which significantly reduces the system power density. The CCM two-level totem-pole PFC can be operated at several hundred kHz switching frequency to reduce the filter size; however, the efficiency will be compromised. Under the same ripple frequency condition, the switching frequency of the four-level totem-pole PFC is only one-third of the switching frequency of the two-level totem-pole PFC. In addition, the switching voltage for each power device of the four-level totem-pole PFC is also only one-third of the switching voltage of the two-level totem-pole PFC. These features significantly reduce the switching losses. Moreover, by the inclusion of interleaving technique, conduction losses can also be minimized by half for the same power level. To evaluate the efficiency advantage of the four-level totem-pole PFC, a detailed device loss comparison among the two-level GaN totem-pole PFC, four-level GaN totem-pole PFC and four-level interleaved FCML PFC with the same inductor current ripple frequency and the peak power is discussed in this section. In this comparison, the test conditions are kept as follows: the grid voltage of 240 Vac/60 Hz, the dc-link voltage of 400 V and the rated power of 2.5 kW. The four-level totem-pole PFC works at 100 kHz switching frequency, and the ripple frequency is 300 kHz. To reduce the inductor size of the two-level totem-pole PFC, the switching frequency of the two-level PFC is increased to 300 kHz, and the ripple frequency increases to 300 kHz as well. During the four-level single phase FCML operation, there are three devices in series under conduction, whereas six EPC2215 switches operate at a time during the interleaved FCML PFC operation with half the current. Therefore, the total equivalent R_{DSon} for the single phase four-level FCML and two-stage interleaved FCML operation is three and six times that of the single-device R_{DSon}. The GaN device loss includes the switching turn ON loss, switching turn OFF loss, charging, and discharging C_{oss} loss, and conduction loss. Since the enhancement-mode GaN devices do not have the reverse recovery issue, there is no zero reverse recovery loss associated. The switching turn on/off losses are the switching transition losses caused by the device current and voltage overlapping. The turn on/off overlapping time t_{on} and t_{off} can be calculated as,

$$t_{on} = \frac{R_{on} Q_{gtotal}}{V_{GS} - V_{plat}} \tag{27}$$

$$t_{off} = \frac{R_{off} Q_{gtotal}}{V_{plat}} \tag{28}$$

where V_{GS} is the gate driver voltage, V_{plat} is the GaN device plateau voltage, R_{on} is the gate resistance of the charging network, R_{off} is the gate resistance of the discharging network, and Q_{gtotal} is total gate charge. In this comparison for the three devices, V_{GS} is 5 V, R_{on} is 5Ω and R_{off} is 1Ω . The switching related loss includes the turn on, turn off and MOSFET C_{oss} loss components that are linearly proportional to the switching frequency. The turn ON/OFF losses (P_{on} and P_{off}) for both the two-level and four-level totem-pole PFC can be calculated as,

$$P_{on} = \frac{1}{2} V_{DC} \, |i_{ac}| \, t_{on} f_s \tag{29}$$

$$P_{off} = \frac{1}{2} V_{DC} \, |i_{ac}| \, t_{off} f_s \tag{30}$$

where the switching frequency f_s is 100 kHz for both the two-level PFC and four-level FCML PFC. During the hard switching transitions, charging and discharging the output capacitance C_{OSS} of the devices will cause extra losses which are not related to the turn ON or OFF speed. The charging and discharging C_{OSS} losses can be expressed as,

$$P_{cossTP} = \frac{1}{2} (2C_{oss}) V_{DC}^2 f_s \tag{31}$$

$$P_{cossFCML} = \frac{1}{2} (2C_{oss}) \left(\frac{V_{DC}}{3}\right)^2 (3f_s) = \frac{1}{3} P_{cossTP} \tag{32}$$

$$P_{cossFCML-2} = \frac{1}{2} (2C_{oss}) \left(\frac{V_{DC}}{3}\right)^2 (6f_s) = \frac{2}{3} P_{cossTP} \tag{33}$$

where V_{DC} is the output DC link voltage, P_{cossTP}, $P_{cossFCML}$ and $P_{cossFCML-2}$ are the C_{OSS} losses for totem-pole PFC, non-interleaved FCML PFC and interleaved FCML PFC, respectively. The conduction and copper(Cu) loss can be calculated as,

$$P_{condTP} = I_{rms}^2 (R_{DSon} + R_{Cu}) \tag{34}$$

$$P_{condFCML} = I_{rms}^2 (3R_{DSon} + R_{Cu}) \tag{35}$$

$$P_{condFCML-2} = 0.5 I_{rms}^2 (3R_{DSon} + R_{Cu}) \tag{36}$$

where R_{DSon} is the GaN FET device on-resistance and R_{Cu} is the total copper resistance of the converter that includes the transformer winding and PCB trace resistance components. On the other hand, the capacitor ESR loss for the FCML PFC includes output capacitor and flying capacitors ESR losses. The rms currents i.e., $I_{C_{out},rms}$ through output capacitor and $I_{C_{fly},rms}$ through flying capacitors can be formulated as

$$I_{C_{out},rms} = \sqrt{\frac{8\sqrt{2} P_{out}^2}{3\pi V_{ac,rms} V_{out}} - \frac{P_{out}^2}{V_{out}^2}} \tag{37}$$

Equation (38) shown at the bottom of the next page.

Here, $\xi = \frac{V_{out}}{V_{ac,peak}}$. The capacitor ESR losses for the 4-level interleaved FCML PFC topology can be computed as,

$$P_{Cout} = I_{C_{out},rms}^2 * ESR_{Cout} \tag{39}$$

$$P_{Cfly} = I_{C_{fly,rms}}^2 * ESR_{Cfly} \tag{40}$$

The inductor core loss is also an important factor while designing PFC front-end converters. A general form of the core loss can be determined from the improved Generalized Steinmetz equation [26] and expressed as follows, which is used in this design for inductor core loss formulation.

$$P_{core} = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{41}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{42}$$

where α, β and k are Steinmetz coefficients given by the inductor manufacturer datasheet. ΔB is the peak-to-peak magnetic flux density and f_s is the ripple frequency. If using the same inductor, the two-level PFC (of 300 kHz) will have much higher core loss compared with the four-level PFC (of 100 kHz) as a higher current ripple would cause a higher flux density swing i.e., ΔB.

$$\Delta B = \frac{L\Delta I}{nA} \tag{43}$$

Even after increasing the switching frequency of a two-level PFC to 300 kHz for keeping the same inductor current ripple frequency as other FCML counterparts, the corresponding inductor loss of the two-level PFC is yet found out to be much higher than those of the four-level PFC. This benefit of the four-level PFC is not only caused by increasing the ripple frequency to three times the switching frequency but also caused by the reduction of the voltage swing across the inductor. Based on the above-mentioned equations, the total power loss for the three PFC topologies at different load conditions is shown in Fig. 12. The interleaved FCML PFC topology results in the least power loss under all load conditions under study. The detailed loss distribution and comparison between the two-level GaN totem-pole PFC, FCML PFC and Interleaved FCML PFC at 10% and 90% load condition are illustrated in Fig. 13.

The 650V GS66516T GaN FETs are utilized for the totem-pole PFC power stage whereas both the single phase FCML and interleaved FCML PFC use 200V-rated EPC2215 switches to realize the high frequency switching leg. Although the 4-level non-interleaved FCML topology has three high frequency switches conducting at a time, the devices with lower voltage rating also possess lower device on-resistance (of 8mΩ) compared to 650V GaN devices in two-level PFC. Although the output capacitance C_{OSS} of the 650V device is lower than the EPC2215 switch, the CV^2 loss of the FCML topology is one-third of the totem-pole PFC as each device withstands one third of the output voltage.

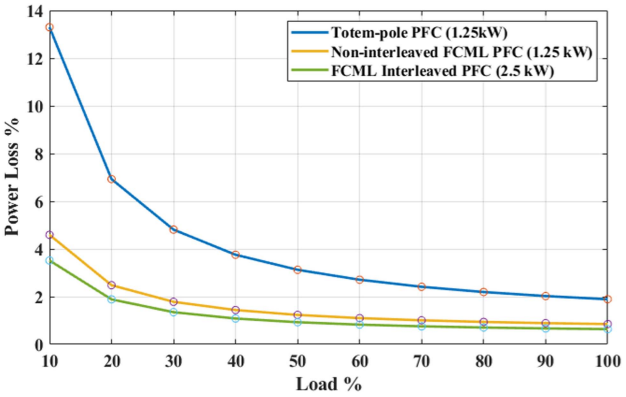

FIGURE 12. Device loss breakdown of the totem-pole PFC, single phase non-interleaved FCML PFC and interleaved FCML PFC.

V. HARDWARE PROTOTYPING AND EXPERIMENTAL RESULTS

In this article, a 2.5 kW hardware prototype of the four-level Interleaved FCML PFC converter is designed and tested. This section discusses the implementation of the hardware prototype followed by the steady state performance and EMI noise spectrum characterization of the FCML PFC converter.

A. HARDWARE PROTOTYPE

To verify the Interleaved Flying Capacitor Multilevel totem-pole PFC operation and control, a 2.5 kW-rated hardware prototype is designed and fabricated according to the list of converter specifications, mentioned in Table 7. The hardware prototype with an on-board EMI filter is shown in Fig. 14 which has a modular architecture having separate daughter-cards for the two FCML high switching frequency legs and the line frequency leg. The list of key components used in hardware prototype is shown in Table 8. To implement the current and voltage loop compensator structures as discussed in Section II, TMS320F28379D (from Texas Instruments), which is a dual-core digital microcontroller with 200 MHz clock has been used. The duty cycle computed from the control output is then used to generate the 12 phase-shifted PWM signals, being fed to the FCML leg high frequency switches. For the line frequency switches, the gate pulses are generated based on checking the polarities of the sensed input voltage

$$I_{Cfly,rms} = \frac{\sqrt{2}I_{AC,peak}}{\sqrt{\pi}}\sqrt{\frac{1}{2}\sin^{-1}\frac{\xi}{3} - \frac{\xi}{6}\sqrt{1-\frac{\xi^2}{9}} + \frac{1}{\xi}\sqrt{1-\frac{\xi^2}{9}}\left(\frac{2}{3}+\frac{\xi^2}{27}\right) + \frac{1}{6}\left[\sin^{-1}\frac{2\xi}{3} - \sin^{-1}\frac{\xi}{3} - \frac{\xi}{3}\left(2\sqrt{1-\frac{4\xi^2}{9}} - \sqrt{1-\frac{\xi^2}{9}}\right)\right] + \frac{1}{\xi}\sqrt{1-\frac{4\xi^2}{9}}\left(\frac{2}{3}+\frac{4\xi^2}{27}\right)} \tag{38}$$

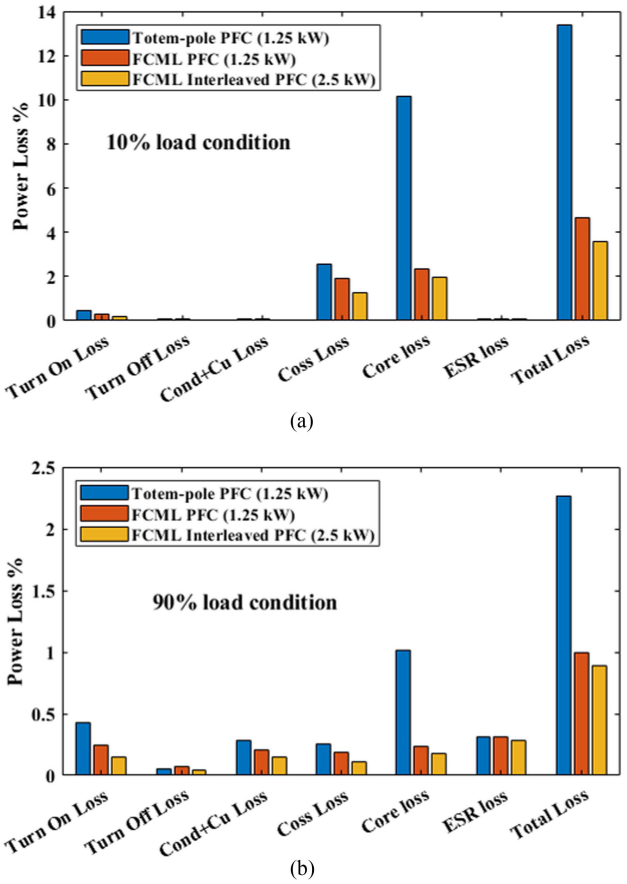

FIGURE 13. Total loss breakdown of the totem-pole PFC, single phase non-interleaved FCML PFC and interleaved FCML PFC. (a) 10% load condition, (b) 90% load condition.

TABLE 7. Specifications of the Interleaved FCML PFC Hardware Prototype

Parameters	Value
Input Voltage, V_{ac}	240 Vac rms
Output Voltage, V_{out}	400 Vdc
Output Power, P_o	2.5 kW
Switching Frequency, f_s	94 kHz
Effective Switching node frequency	300 kHz
Input Line Inductor, L_1 L_2	85.2 μH, 85.13 μH
Flying Capacitor, C_{11} C_{12} C_{21} C_{22}	11 μF
Output DC link Capacitor, C_o	660 μF

ADC signals. The FCML totem-pole PFC converter operation is largely dependent on the voltage balancing of the flying capacitors [27]. Hence, during the layout design process, high frequency decoupling capacitors are placed in close proximity to the EPC GaN FETs to lower the stray inductance and provide low impedance path to the output terminal. By ensuring the voltage levels to be balanced, it is safely assumed that each four-level FCML leg switch withstands 133.3V (V_o/3) and

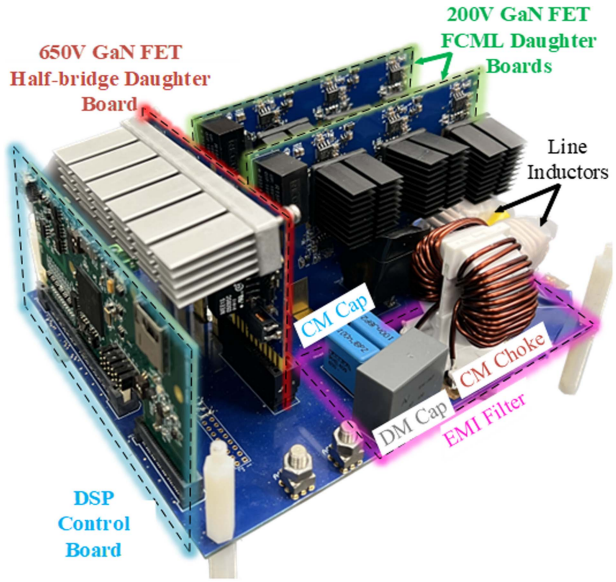

FIGURE 14. Hardware prototype of the interleaved FCML totem-pole PFC.

TABLE 8. Key Components of FCML PFC Hardware Prototype

Component	Part Number	Parameters
FCML GaN FETs	EPC2215	200 V, 8 mΩ
Line frequency GaN FETs	GS66516T	650 V, 25 mΩ
Gate Driver	SI8271GBD-IS	4 A, 2.5 kV
Bootstrap LDO	TPS71550DCKR	5 V, 50 mA
Bootstrap diode	VS-2EFH02HM3/I	200 V, 2 A
Inductor	0077930A7	A_L=157 nH/T^2
Flying Capacitor	C5750X6S2W225K250KA	450 V, 2.2 μF
Output DC link Capacitor	450HXW220MEFR18X45	450 V, 220 μF
DM Capacitor	B32672Z4334K000	450 V, 0.33 μF
CM Choke	SC-15-10J	1 mH, 15 A
DSP Controller	TMS320F28379D	Dual core 32 bit, 200 MHz clock
Heat Sink	UB22-20B	4.2 °C at 0.5 ms^{-1}

is hence realized using six 200V EPC2215 GaN FETs with sufficient safety voltage margins.

B. STEADY STATE EXPERIMENTAL RESULTS

The key experimental waveforms for an input voltage of 240Vac rms to achieve an output DC link voltage of 400 V at 2.5 kW resistive load condition are illustrated in Figs. 15 and 16. The inductor current I_{AC} of 10.35 A rms and with a THD of 4.33% is found to be in phase with the input voltage V_{AC} which exhibits the verified steady-state functionalities of the current loop compensator, yielding unity power factor. The output voltage is well regulated at 400Vdc with less than 5% voltage ripple. Fig. 17 depicts the boost inductor currents I_{L1}

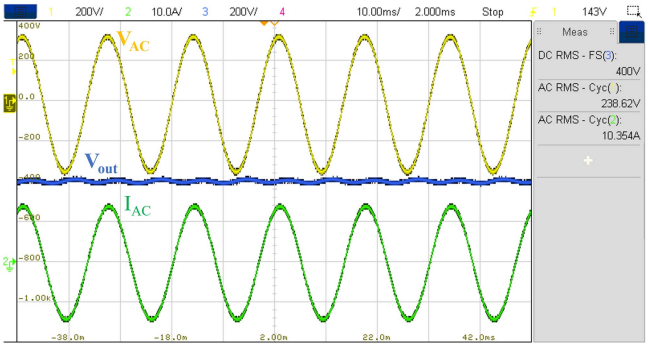

FIGURE 15. Experimental waveforms showing input voltage, input current and output DC link voltage at 2.5 kW steady state operation.

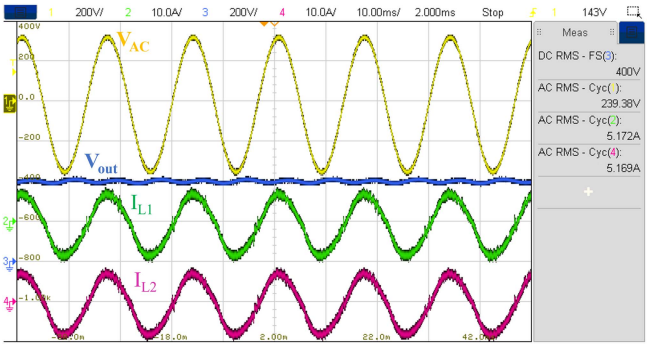

FIGURE 16. Experimental waveforms showing input voltage, boost inductor currents of two phases, and output DC link voltage at full load operation.

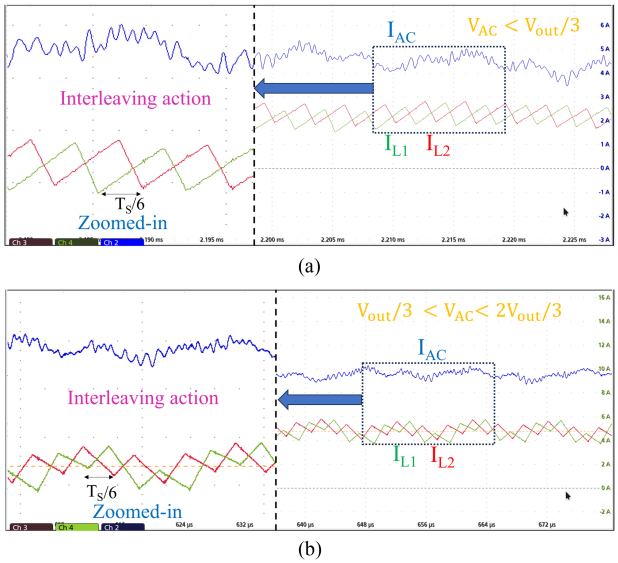

FIGURE 17. Waveforms showing input voltage, input current and boost inductor currents. (a) $V_{in} < V_{out}/3$. (b) $V_{out}/3 < V_{in} < 2V_{out}/3$.

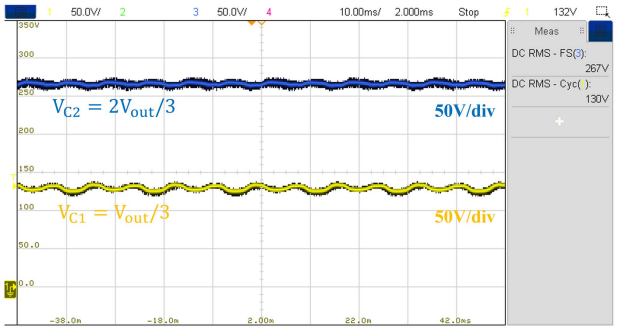

FIGURE 18. Experimental waveforms of the flying capacitor voltages at 2.5 kW steady state operation.

and I_{L2} having 5.172A rms and 5.169A rms with 300 kHz ripple frequency. The zoomed in waveforms of input current $I_{AC,}$ boost inductor currents I_{L1} and I_{L2} at different intervals of the line cycle are illustrated in Fig. 16. It can be observed that the inductor current I_{L2} lags I_{L1} by $T_s/6$ seconds, while the sum of these currents counteracts each other to result in the grid current with much lower current ripple content as discussed in Section II. Also, as evident from Fig. 18, the flying capacitor voltages V_{C1} and V_{C2} are naturally balanced at $V_{out}/3$ and $2V_{out}/3$ voltages, respectively, with a maximum ripple of 11V i.e., ±8.5%. To suppress the EMI noise and to comply with the required standard, a DM EMI filter with the values of its elements obtained from the mathematical models developed earlier, is designed and implemented at the front end of the converter. The experimentally obtained EMI spectrum of the input current for the filter-integrated interleaved FCML PFC is given in Fig. 19 (zoomed) for a span of 1 MHz, which when compared with the FCC class A EMI standard shows that the input current spectrum complies with the required standard limit all throughout the conducted EMI zone. The zoomed in figure includes the EMI spectrum with a span of 1 MHz to illustrate the EMI peak occurring at 600 kHz. The EMI spectrum of the model with the optimum DM EMI filter ($L_{DM} = 51.96\ \mu$H and $C_{DM} = 0.35\ \mu$F) is depicted in Fig. 11. The experimental EMI noise peaks at 600 kHz with 73.5 dB μV which closely match with the mathematical model showing 72 dB μV for the respective peak.

The efficiency of hardware prototype is measured using HIOKI PW3337 power meters and compared with the analytically computed efficiency derived from the loss analysis done in Section IV and depicted in Fig. 20. The error margin of the efficiency measurement with the PW3337 power meter is restricted within ±0.1%. The measured peak efficiency of the converter is 99.14% at 1750 W load, while the full load efficiency reaches 99.06%. Moreover, the maximum deviation of the analytically derived efficiency from the experimental measurements is 0.3%. Fig. 21 depicts the thermal image of the converter operating at 2.5 kW for an input voltage of 240Vac rms using a FLIR E6-XT infrared thermal camera. The maximum temperature of the converter during operation settles at 62.5 °C without the use of any external fans at an ambient of 22 °C. It is mainly the power devices that attain a steady temperature of ∼60 °C, while the boost inductors stay much cooler at about 35 °C. The thermal picture of

TABLE 9. Comparison of PFC Topologies

Topology	Power Density (W/inch^3)	Maximum Efficiency	Total AC-side passive volume (cm^3) to rated power ratio [cm^3/kW]	Remarks
Boost PFC [28]	36	98.6%	138*	Simple design, Significant diode-bridge loss
Totem-pole PFC [29]	78	99%	75.28*	Zero reverse recovery loss, Large inductor size, Limited switching frequency
Interleaved CRM TP PFC [4]	200**	98.8%	46.2*	Soft-switching capability, Higher switching frequency, Larger EMI Filter
Non-interleaved FCML PFC [15]	104	99.25%	48.39*	Higher power density and efficiency, Reduced inductor size, Lower switching loss
FCML Interleaved PFC [this work]	89.47	99.04%	43.9	Requires lower EMI attenuation, Higher number of components

*AC-side passive volume estimated from the given part numbers. ** Not including EMI filter, DC link capacitor and controller.

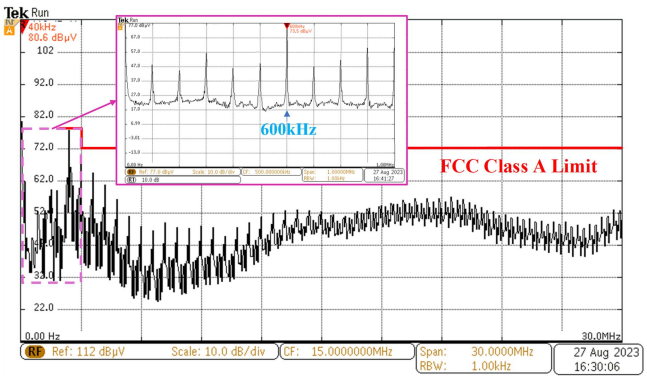

FIGURE 19. Input current EMI spectrum after implementation of the EMI filter at the front end of the Interleaved FCML PFC converter.

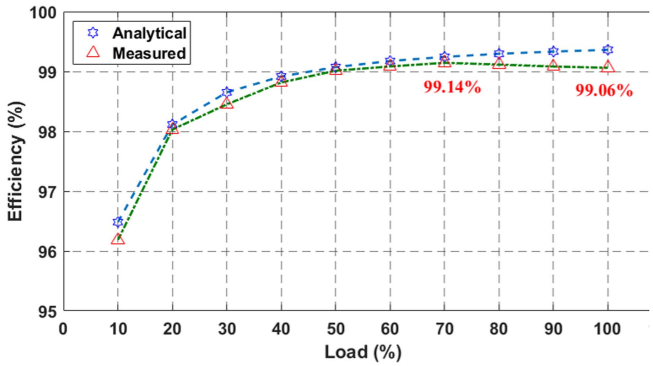

FIGURE 20. Measured efficiency of the Interleaved FCML PFC hardware prototype.

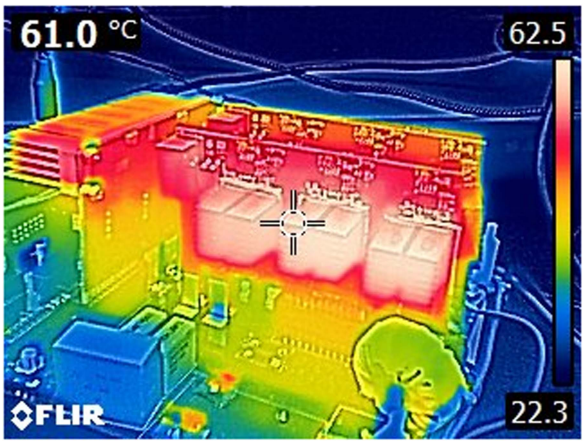

FIGURE 21. Thermal image of the converter operating at 2.5 kW for input voltage V_{AC} = 240Vac rms.

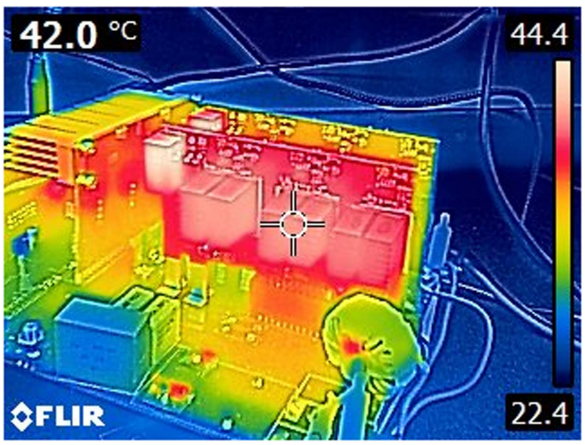

FIGURE 22. Thermal image of the converter operating at 1.25kW for input voltage V_{AC} = 120Vac rms.

the converter operating at 1.25 kW for 120Vac(rms) is also illustrated in Fig. 22 where the maximum temperature attains 44.4 °C with similar setup. Table 9 shows the performance comparison along with the respective salient features of this work with state-of-the-art PFC topologies in the literature and commercial PFC front-end products in terms of power density, efficiency, and total AC-side passives volume-to-power ratio (in cm^3/kW). The passive components employed for the interleaved FCML PFC converter are based on the optimization routine performed in Section III-C. The interleaved FCML PFC converter shows 9.3% lower cm^3/kW ratio compared to the non-interleaved FCML PFC [15], while also exhibiting 14.7% higher power density than totem-pole PFC converter [29]. Table 10 depicts the transient performance comparison of this work with other control algorithms available in the literature. The comparison is made mainly against the totem-pole boost PFC candidates because the transient performance of FCML PFC is not available in literature. Moreover, to enhance the efficiency of the FCML PFC converter, critical

TABLE 10. Comparison of Control Performance

Reference/Topology	Load Transient	Output Voltage Overshoot (%)	Settling Time	Type of Control
Jain et al. [30] Boost PFC	1 kW to 160 W	22	580 m	Non-linear control
Rao et al. [31] Boost PFC	1 kW to 160 W	20	55 m	Lead-Lag
Mallik et al. [32] TP PFC	500 W to 400 W	5	80 m	Sliding mode Control
This work	1 kW to 500 W	11	200 m	Type II Control
Chu et al. [33] Boost PFC	108 W to 38 W	-	20 m	Feedback linearization

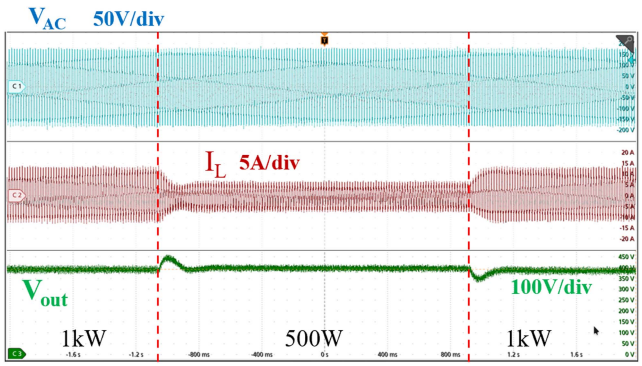

FIGURE 23. Experimental waveforms of the system during load change from 1 kW to 500 W and again back to 1 kW.

conduction mode (CrCM) mode control is a viable option that allows the GaN FETs to achieve soft switching resulting in nulling the turn-on switching loss. This will also allow the optimum switching frequency to increase and further reduce the AC-side passive volume. However, the soft switching techniques (i.e., Zero Voltage Switching (ZVS) capability) of FCML candidates have not been reported in the literature yet. The proposed multilevel interleaved PFC converters blended with CrCM-enabled soft-switching would therefore have great potential in terms of improving the efficiency and power density. Fig. 23 illustrates the experimental waveforms of the system when a load transient from 1 kW to 500 W is applied and then increased back to the previous 1 kW load condition. It can be observed that the controller takes only 200 milli-seconds to settle the input inductor current to 4.2 A rms which corresponds to the 500 W load. The output DC link V_{out} experiences an overshoot of 11.11%.

VI. CONCLUSION

This article presents the design and control of a 2.5 kW interleaved FCML totem-pole PFC converter. The four-level interleaved FCML GaN totem-pole PFC has the following benefits: utilization of the low-voltage GaN devices, reduced switching voltage stress, reduced voltage swing on the inductor, and raising the equivalent ripple frequency of the inductor. This work is the first to demonstrate enhanced efficiency and power density employing 200 V GaN devices for the four-level interleaved FCML totem-pole PFC, producing 3x effective frequency of inductor current and cascaded benefits of current ripple elimination by means of the interleaving mechanism. It discusses the detailed explanation of the Interleaved FCML PFC converter's control approach for closed-loop regulation as well as the waveform dynamics of individual phase currents and grid current in all working modes. This article also presents an extensive mathematical modelling of the input current FFT model and AC-side passive volume co-optimization of the TPFC, non-interleaved FCML PFC and Interleaved FCML PFC converter. Based on the comparison, the four-level interleaved FCML totem-pole PFC is found to be exhibiting 9.3% lower cm^3/kW ratio compared to the non-interleaved FCML PFC and 14.7% higher power density than totem-pole PFC converter, as indicated in Table 9. The interleaved FCML PFC prototype achieved a power density of 89.47 W/in^3 while the peak efficiency is reported as 99.14%. Finally, we demonstrate that the viability of the interleaved FCML configuration in PFC applications can bring significant improvements in terms of efficiency and lower AC-side passive volume.

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NAVEED ISHRAQ (Student Member, IEEE) received the B.S. degree in electrical engineering from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 2021. He is currently working toward the Ph.D. degree with the Power Electronics and Control Engineering Laboratory, Arizona State University, Tempe, AZ, USA. His research interests include wide bandgap semiconductor device applications in high-power density multilevel converters, isolated DC-DC resonant converters, and bridgeless PFC rectifiers for electric vehicle applications.

AYAN MALLIK (Senior Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, MD, USA, in 2018 and 2019, respectively. In 2019, he joined Arizona State University, Tempe, AZ, USA, as an Assistant Professor. He is an author or co-author or co-inventor of more than 90 peer-reviewed publications and four pending/issued U.S. Patents. His research interests include the modeling, control, and multi-objective optimization of multi-order power converters. Dr. Mallik was the recipient of NSF CAREER award (2023) and IEEE TPEL second place Prize Paper Award (2023).