INVITED PAPER

Doubling Down on Wireless Capacity: A Review of Integrated Circuits, Systems, and Networks for Full Duplex

This article presents a comprehensive review of in-band full-duplex wireless systems with a focus on hardware design and implementation.

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ABSTRACT | The relentless demand for data in our society has driven the continuous evolution of wireless technologies to enhance network capacity. While current deployments of 5G have made strides in this direction using massive multiple-input–multiple-output (MIMO) and millimeter-wave (mmWave) bands, all existing wireless systems operate in a half-duplex (HD) mode. Full-duplex (FD) wireless communication, on the other hand, enables simultaneous transmission and reception (STAR) of signals at the same frequency, offering advantages such as enhanced spectrum efficiency, improved data rates, and reduced latency. This article presents a comprehensive review of FD wireless systems, with a focus on hardware design, implementation, cross-layered considerations, and applications. The major bottleneck in achieving FD communication is the presence of self-interference (SI) signals from the transmitter (TX) to the receiver, and achieving SI cancellation (SIC) with real-time adaption is critical for FD deployment. The review starts by establishing a system-level understanding of FD wireless systems, followed by a review of the architectures of antenna interfaces and integrated RF and baseband (BB) SI cancellers, which show promise in enabling low-cost, small-form-factor, portable FD systems. We then discuss digital cancellation techniques, including digital signal processing (DSP)- and learning-based algorithms. The challenges presented by FD phased-array and MIMO systems are discussed, followed by system-level aspects, including optimization algorithms, opportunities in the higher layers of the networking protocol stack, and testbed integration. Finally, the relevance of FD systems in applications such as next-generation (xG)

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wireless, mmWave repeaters, radars, and noncommunication domains is highlighted. Overall, this comprehensive review provides valuable insights into the design, implementation, and applications of FD wireless systems while opening up new directions for future research.

KEYWORDS | Antenna interface; baseband (BB) cancelers; digital cancellation; full-duplex (FD) wireless; integrated circuit (IC); RF cancelers; self-interference (SI) cancellation; testbeds.

I. INTRODUCTION

Every new generation of wireless technology seeks to significantly enhance the network capacity beyond the previous generations to support our society's insatiable need for data. For instance, current 5G deployments are exploiting massive multiple-input–multiple-output (MIMO) in the sub-6-GHz bands and new millimeter-wave (mmWave) bands, to enhance capacity. However, all wireless communication systems today, including unlicensed Wi-Fi and licensed cellular networks, function in a half-duplex (HD) mode. This means that the radios involved in the communication process transmit and receive signals in separate time slots [known as time-division duplexing (TDD)] or in different frequency bands [known as frequency-division duplexing (FDD)]. Over the past decade, there has been significant interest in full-duplex (FD) wireless [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], which is an emerging communication paradigm enabling simultaneous transmission and reception (STAR) of radio signals at the same frequency. The adoption of FD wireless technology offers several advantages, including enhanced spectrum efficiency, improved data rates, and reduced communication latency.

However, a significant obstacle in achieving FD wireless communication is the presence of strong self-interference (SI) signals from the transmitter (TX) to the receiver (RX), potentially desensitizing the RX. This SI: 1) is typically 90–120 dB larger than the desired signal, requiring very high levels of SI suppression; 2) undergoes substantial frequency dispersion, due to long delay spreads in the SI channel; and 3) is subject to changes in the electromagnetic environment, requiring adaptive cancellation. Fortunately, unlike unknown blockers, the knowledge of the TX SI enables cancellation architectures where a portion of the TX signal is coupled and used to cancel the SI at RX. As depicted in Fig. 1, the required large SI cancellation (SIC) levels necessitate cancellation across multiple domains, starting from the initial antenna interface through antenna pair isolation [8], [19], reciprocal hybrids [20], [21], [22], [23], [24], [25], [26], [27] and circulators [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43]; then through analog RF/baseband (BB) cancellation [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55]; and finally digital cancellation [6], [7], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66].

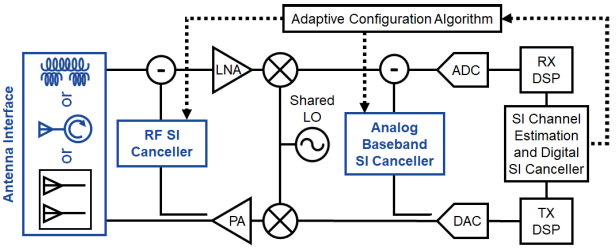


Fig. 1. ***Block diagram of a typical FD transceiver employing multidomain SIC.***

This review article provides a comprehensive exploration of FD wireless systems, including aspects of their hardware design and implementation, performance optimization, and testbed integration. We focus primarily on the design of SIC techniques tailored for small-form-factor/integrated circuit (IC) implementations, some of which have been addressed over the past decade within the Columbia FlexICoN project [18]. We follow up with discussion on the cross-layer challenges stemming from these designs, which influence the overall benefit FD that can have to networks of devices. The organization of this article is given as follows. In Section II, a system-level understanding of FD wireless systems is established by offering an overview of the typical FD system architectures and their link budget, considering factors such as signal strength, interference, and noise. Section III reviews the design of antenna interfaces for FD wireless, including dual antenna schemes, passive hybrids, and integrated circulators. For a quantitative and fair comparison, we define two figures of merit (FOMs): 1) the *antenna interface efficiency* and 2) the *isolation fractional-bandwidth (FBW) product*. In Section IV, research progress on RF and analog-BB SIC circuits is reviewed by providing an in-depth analysis of various circuit techniques, including phase-based cancellers, time-domain cancellers, and frequency-domain cancellers. We provide two FOMs for SI cancellers for fair comparison and performance evaluation: 1) the *canceller efficiency* and 2) the *SIC-FBW product*. Section V reviews digital SIC techniques such as digital signal processing (DSP)-based techniques and learning-based techniques. In Section VI, the challenges and opportunities presented by FD phased-array and MIMO systems are discussed. Following that, Section VII addresses the configuration of several examples of FD hardware introduced in the earlier parts of this article, an important step toward a full system-level integration of an FD radio. Section VIII discusses the cascading impact of FD at higher layers of the networking stack, including the development of effective medium access control (MAC) algorithms and potential benefits at the transport layer. We also discuss open-access FD hardware integrated in the ORBIT and NSF PAWR COSMOS testbeds [66], [67], [68]. Section IX focuses on the relevance of FD systems in various applications such as next-G wireless, mmWave repeaters, radars, and other

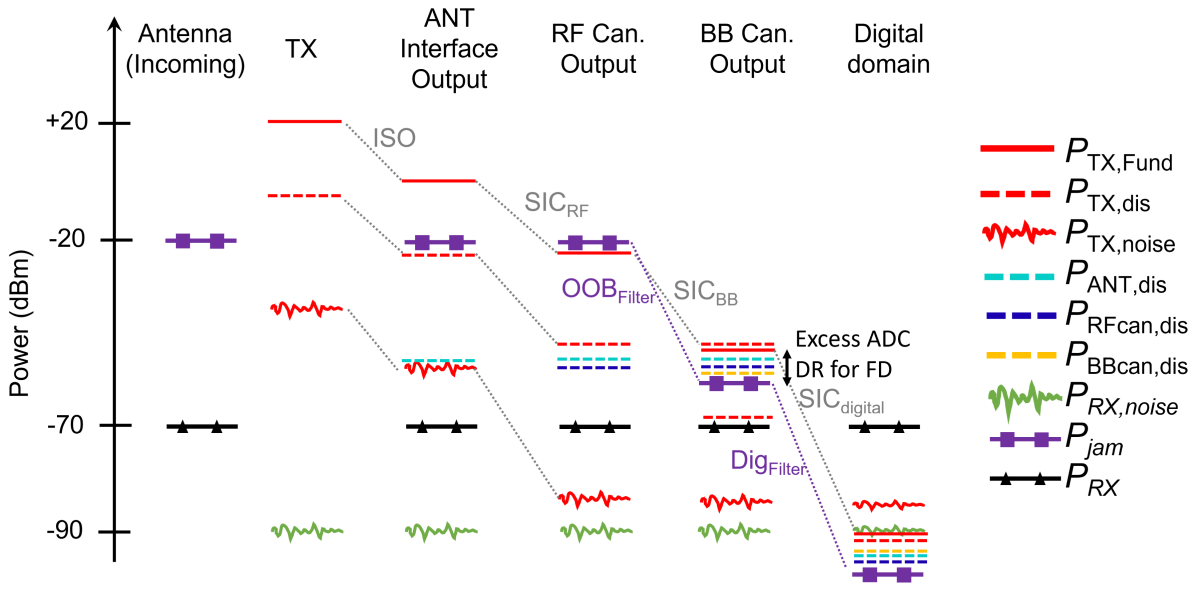


Fig. 2. ***Typical signal levels in FD radios across cancellation stages.***

noncommunication applications. Finally, Section X concludes this article. For a detailed review of physical layer approaches, network design, and large-scale deployed network design, readers are directed to the review articles in [69], [70], and [71], respectively.

II. SYSTEM-LEVEL UNDERSTANDING OF FD WIRELESS SYSTEMS

Various power levels in an FD transceiver across the stages are depicted in Fig. 2. The receiver must receive a small signal in the presence of an out-of-band jammer and the TX leakage signal. Therefore, at the input of an FD receiver, one may expect various signals: 1) the received signal (P_{RX}); 2) the leakage of the TX signal from the power amplifier (PA) output ($P_{\text{TX,Fund}}$); 3) the leakage of the TX nonlinear distortion ($P_{\text{TX,dis}}$) and TX noise ($P_{\text{TX,noise}}$); and 4) an out-of-band jammer (P_{jam}). Various contributions of the TX signal (fundamental, nonlinearity, and noise) that originate at the PA output leak to the receiver input through the antenna interface due to finite TX-to-RX isolation (ISO). If the antenna interface exhibits nonlinear distortion and/or adds noise, as electrical balanced duplexers (EBDs) and active or time-varying circulators do, then those components also appear at the RX input. These SI signals should be canceled to a level close to/below the receiver noise floor, to achieve a successful RX reception without degrading sensitivity. The signal-to-noise ratio (SNR) degradation in the RX link can be quantified as $+10\log_{10}(1+R)$ dB, where R depicts the ratio of the SI power after all cancellation domains and the noise floor of the receiver.

As an example, let us assume an IEEE 802.11ac Wi-Fi [72] signal with $P_{\text{TX,Fund}}$ of +20 dBm at the TX output, 80-MHz RX bandwidth (BW), and 8-dB RX noise figure (NF, NF_{RX}). To achieve a receive link with +3-dB SNR degradation (i.e., $R = 1$ and SI power after the cancellation = noise floor of the receiver), a total SIC of 20 dBm (−174 dBm/Hz + 8 dB + 79 dBHz) = 107 dB is required. Achieving such a significant level of isolation and cancellation necessitates combined suppression across the antenna isolation (ISO), RF (SIC_{RF}), BB (SIC_{BB}), and digital domains (SIC_{Dig}). When using a real-world RF channel, a typical ISO of 20–30 dB [39], SIC_{RF} of 20–25 dB [54], [55], [73], SIC_{BB} of 15–25 dB [54], [55], and SIC_{Dig} of 35–45 dB [6], [7] can be achieved.

The first line of defense to protect the RX from compression is the isolation from the antenna interface. The key metrics of the importance of the antenna interface are: 1) TX-to-RX isolation (ISO); 2) ANT-to-RX loss (L_{ANT}); and 3) TX-to-RX IIP3 ($\text{IIP3}_{\text{ANT,TX–RX}}$) defined as TX power level at which the power levels of TX leakage to the RX port and the nonlinearity generated by the antenna interface at the RX port are equal. Therefore, the signals at the RX port can be expressed as follows: 1) P_{RX}–L_{ANT}; 2) P_{jam}–L_{ANT}; 3) $P_{\text{TX,Fund}}$ − ISO; 4) $P_{\text{TX,dis}}$ − ISO; 5) $P_{\text{TX,noise}}$ − ISO; and 6) $P_{\text{ANT,dis}} = P_{\text{TX,Fund}} - 0.5 \times \text{IIP3}_{\text{Ant,TX–RX}}$, as depicted in Fig. 2. Here, we are assuming that while the antenna interface might introduce nonlinear distortion, it does not produce any excess random noise.

Next, the RF cancellers tap the PA output and cancel the SI at the RX front end, effectively canceling TX fundamental signal, TX nonlinear distortion, and TX noise, while the antenna interface distortion, desired receive signal, and the jammer remain unaffected. In addition, the RF canceller may introduce its own nonlinear distortion ($P_{\text{RFCan,dis}}$). Therefore, the signals at the output of the RF canceller can be expressed as follows: 1) P_{RX}–L_{ANT};

2) P_{jam}–L_{ANT}; 3) $P_{\text{TX,Fund}} - \text{ISO} - \text{SIC}_{\text{RF}}$; 4) $P_{\text{TX,dis}} - \text{ISO} - \text{SIC}_{\text{RF}}$; 5) $P_{\text{TX,noise}} - \text{ISO} - \text{SIC}_{\text{RF}}$; 6) $P_{\text{ANT,dis}}$; and 7) $P_{\text{RFCan,dis}}$, as depicted in Fig. 2.

Further downstream, the TX terms are additionally canceled by the BB SI canceller, which may add its own nonlinearity terms $P_{\text{BBCan,dis}}$. It is important to highlight that when BB cancellers tap from the TX BB, the tapped signal does not include the components related to PA nonlinearity and PA noise. As a result, the BB canceller does not suppress these components, as illustrated in Fig. 2. To overcome this limitation, alternative BB cancellers have been investigated in previous studies, which involve downconverting the PA output [42], [55]. Despite increasing the BB canceller complexity, this architecture offers benefits by reducing the design requirements for PA noise, PA nonlinearity, and nonlinear digital cancellation. Finally, the fundamental TX and the nonlinear terms are canceled to the noise floor by the digital canceller. The nonlinear terms generated by the antenna interface and the RF canceller are predictable and can also eventually be canceled in the digital domain [74], [75], [76]. Assuming a similar level of digital SIC for the fundamental and nonlinear terms, the nonlinear terms generated by the antenna interface, RF canceller, and the BB cancellers should be $<(P_{\text{TX}} - \text{ISO} - \text{SIC}_{\text{RF}} - \text{SIC}_{\text{BB}}) = -52$ to -42 dBm, which sets the linearity requirement on the antenna interface and the RF/BB cancellers. However, unpredictable effects of SI, including RX gain compression of the desired signal, NF increase due to the gain compression, and interaction between the SI (or other nonlinear distortion terms) and the unknown incoming jammer, cannot be canceled in the digital domain. Therefore, the RX in an FD system should be designed with sufficient linearity to handle these impairments.

III. DESIGN OF ANTENNA INTERFACES

The antenna interface of FD wireless systems can be split into two main categories: 1) dual-antenna schemes and 2) single-antenna interfaces such as EBDs and circulators. The antenna or propagation domain is the first SIC domain within an FD system. Achieving higher amounts of SIC in this domain is crucial for relaxing the dynamic range requirements of the rest of the receiver chain.

A. Dual-Antenna Schemes

If the size of the FD system is not limited, a dual-antenna interface with physical separation between the antennas may be used, which is often referred to as bistatic simultaneous transmit and receive antenna systems [8], [19]. By increasing the distance between the antennas (typically by a few wavelengths), a high level of RF isolation can be achieved. In such a configuration, the power couples between the TX and RX antennas in two main ways: 1) through the spatial domain consisting of antenna-to-antenna coupling and reflections from nearby objects and 2) through the ground plane and antenna feed networks. Additional spacing between the antennas and using different antenna polarizations, therefore, can help reduce the overall coupling between the TX and the RX. Various decoupling techniques have been proposed to further increase the isolation between TX and RX in a bistatic antenna system such as using absorbers, reactive impedance surfaces, and wavetraps [19]. Bistatic configurations can achieve large BWs and high isolation and are robust to fabrication mismatches in aperture geometry since the isolation is mainly dictated by the physical distance of the antennas. Furthermore, directional antennas can also be used to achieve more isolation by choosing the direction appropriately to reduce the gain from the TX antenna to RX antenna [77]. This approach helps reduce the significant line-of-sight component of the SI from the TX to RX. However, the biggest drawback of bistatic configurations is the increased size of the overall system, which is prohibitive, especially for handheld devices operating in the sub-6-GHz frequency bands. Furthermore, usage of two antennas or two polarizations may require sacrificing MIMO or polarization multiplexing, which can also double the data rate, similar to the FD operation.

B. Single-Antenna Interfaces

As discussed previously, single-antenna interfaces are more desirable for compact FD implementations. In addition, they ensure channel reciprocity and can ease the translation of the FD concept to phased-array and MIMO systems.

To enable single-antenna operation, a three-port device is needed that routes the outgoing TX signal to the ANT port, while the incoming signal from the antenna is delivered to the RX port. This function can be achieved using reciprocal or nonreciprocal components as discussed next.

1) Reciprocal Single-Antenna Interfaces: EBDs are a class of reciprocal components that operate based on balancing signals in a 180° or 90° hybrid coupler through a balance impedance to provide isolation between TX and RX [refer to Fig. 3(a)]. Various EBD implementations have reported operation ranges from low-RF all the way to mmWave frequencies [20], [21], [22], [23], [24], [25], [26], [27]. It is known that reciprocal matched three-port networks cannot be lossless, and hence, EBDs that use a symmetrical hybrid feature a theoretical 3-dB loss in the TX–ANT and ANT–RX transmission paths [82]. In practice, implementation nonidealities, such as additional ohmic loss producing finite Q in the transformer, increase the losses by an additional 0.5–1 dB. Using an asymmetrical hybrid can allow to favor either TX–ANT loss or RX NF performance [20]. EBDs can be integrated on-chip, and hence, they are suitable for low-cost small-form-factor devices. They offer additional benefits such as high linearity without any dc power consumption and dynamic adaptive isolation through the use of reconfigurable balance networks. Their linearity is typically limited by the switches used in the balance network.

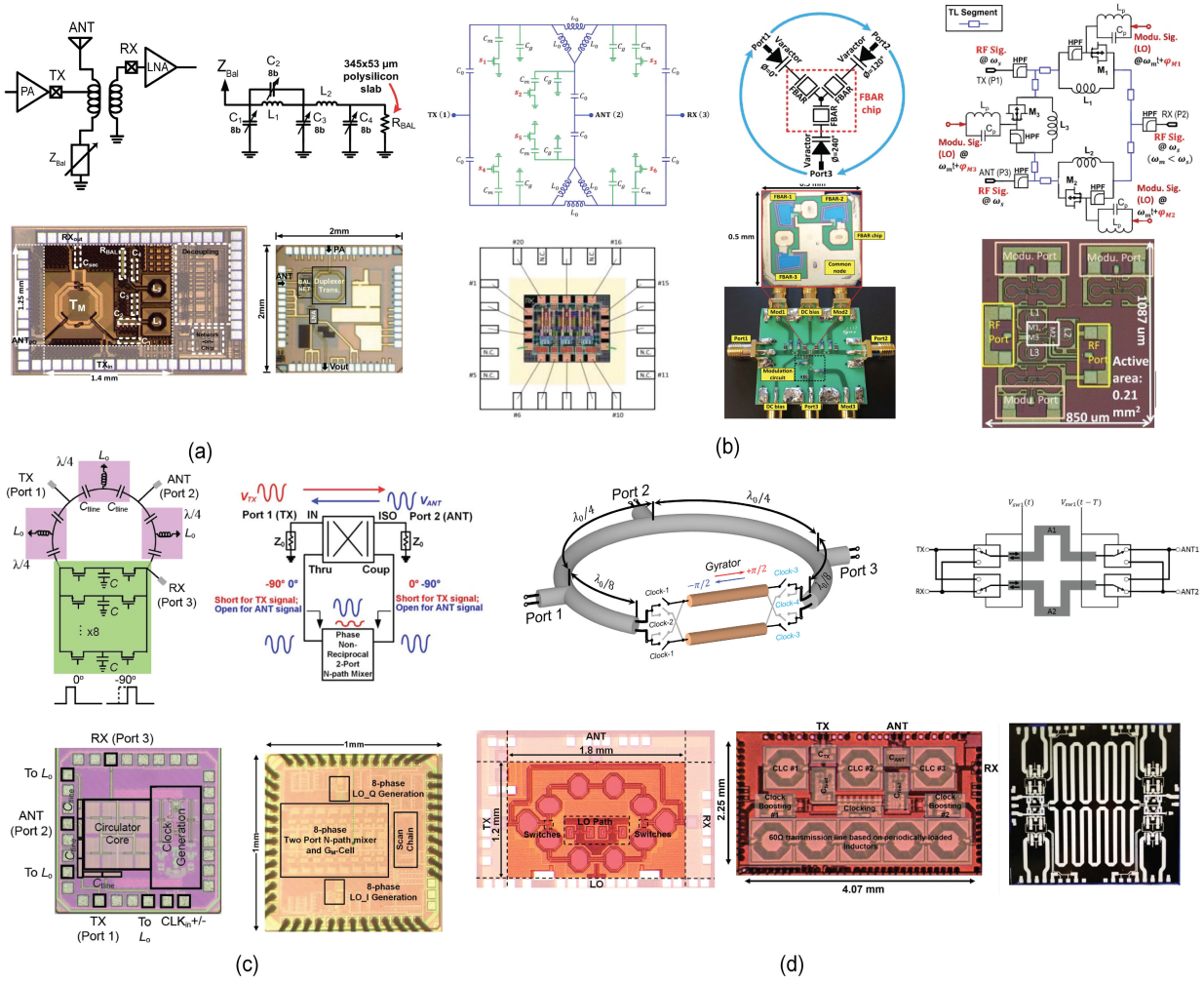


Fig. 3. ***Various shared antenna interfaces for FD systems. (a) EBDs. Top left: structure of an EBD with a single-ended LNA configuration. Top right: highly linear balance network used in [23]. Bottom: chip photographs of EBDs implemented in [22] and [23]. (b) Circulators based on angular momentum biasing. Left: schematic and chip photograph of the circulator implemented in [38]. Middle: schematic and implementation photograph of the FBAR circulator implemented in [78]. Right: schematic and chip photograph of the circulator implemented in [37]. (c) N-path-filter-based circulators. Left: schematic and chip photograph of first on-chip magnetic-free circulator [29] and [79]. Right: schematic and chip photograph of [80]. (d) Transmission-line-based circulators. Left: general circuit diagram and chip photographs of transmission-line-based circulators implemented in [31] and [42]. Right: schematic and chip photograph of the circulator implemented in [81].***

State-of-the-art integrated EBDs have demonstrated up to +70-dBm TX–ANT IIP3 and +30-dBm TX power handling (+27 dBm at the ANT port) [23] by stacking four silicon-on-insulator (SOI) SOI CMOS transistors to reduce the voltage swing across individual devices.

Since antenna impedance can vary across the operation frequency and due to environmental reflections such as user interaction, the balancing impedance should be synthesized to cover the full range of antenna impedance variability. Higher order passive LC ladders as shown in [24] can be incorporated to provide tunability across antenna voltage standing wave ratio (VSWR); however, such methods come with the cost of large area (due to the need for multiple inductors) and complex tuning algorithms for dynamic adaptation. Elkholy et al. [22] report a multiband EBD that achieves >40-dB isolation across 180-MHz BW using an RC balance network and can support antenna impedances with VSWRs of up to 1.5. The work presented in [23] and [83] uses an RLC network with four 8-bit tunable capacitors to achieve >50-dB isolation across 300-MHz BW and supports antenna impedances with VSWRs of up to 1.5. In [25], an EBD implementation is demonstrated at 120 GHz using an on-chip antenna which achieves >30-dB isolation across 14-GHz BW.

Furthermore, active balancing techniques have been proposed and implemented in [84] that use an additional TX to generate a cancellation signal, which is injected into the EBD through the balance port. However, such an approach is inherently limited by the noise and distortion of the auxiliary TX path.

2) Nonreciprocal Single-Antenna Interfaces: Nonreciprocal devices, such as circulators, are another option for the antenna interface of FD systems. A circulator is a three-port

component that routes the signals in a single direction from TX to ANT and ANT to RX while isolating the TX and RX. Ideal circulators also route any incoming signal from the RX port to the TX, although this is not of importance in FD systems since the RX is typically designed to be matched to avoid reflections. Another type of nonreciprocal device, namely, *quasi-circulators*, only provides TX–ANT and ANT–RX transmission while still isolating the TX and RX [85].

Conventional circulators are built based on the concept of Faraday rotation in a magnetized ferrite material. Off-the-shelf ferrite circulators achieve very low loss (as low as 0.5 dB) and impressive power handling (beyond 1 kW) [86] but are bulky and expensive for size- and cost-constrained FD systems (e.g., systems with handheld devices). There have been efforts to integrate ferrite-based components into semiconductor manufacturing processes in recent years, but these require nontrivial postprocessing [87], [88]. These prototypes while promising still occupy a significant area compared to nonmagnetic approaches that are discussed next since the size of the devices is proportional to the wavelength of the operation frequency.

Another alternative to build nonreciprocal components is by using nonmagnetic approaches that can be integrated into chip-scale semiconductor ICs. Incorporating time variance in the form of permittivity and conductivity modulation has shown promising results in enabling nonmagnetic nonreciprocal devices with compact form factors that can be suitable for FD applications [30], [35], [38], [39], [42], [43], [80], [89], [90], [91]. In principle, using time variance to break reciprocity can enable highly linear implementations that do not add additional noise. However, in practice, implementing the modulation adds additional loss and nonlinearity, and the modulation signal's phase noise can degrade the NF.

To perform permittivity modulation in the RF domain, a varactor or a switched-capacitor bank can be modulated using a pump signal to vary its capacitance. Inspired by how ferrite circulators operate, a nonreciprocal response can be achieved using angular momentum biasing within a loop consisting of three individual LC tanks [refer to Fig. 3(b)]. Each LC tank is modulated using a pump signal with a different phase [0, $(T_m/3)$ and $(2T_m/3)$], where T_m is the modulation period, to create a preferred sense of rotation within the loop. The loop can be formed using various architectures, such as delta or wye, as well as using single-ended or differential topologies [38], [89], [92], [93], [94], [95]. The use of resonators based on lumped inductors and capacitors miniaturizes the size of the ring in these works and allows for strong nonreciprocal response in subwavelength dimensions. Kord et al. [38] report an angular momentum-based circulator implemented in 180-nm CMOS operating at 0.91 GHz, which achieves a $>$20-dB isolation BW of 22 MHz. This technique has also been explored at mmWave frequencies to implement a circulator in CMOS [37]. Alternatively, SAW, MEMS, and FBAR resonators can be used in conjunction with varactors to create hybrid electronic–acoustic approaches [78], [96], [97], [98]. Kord et al. [40] provide a very detailed overview of all such implementations.

While using permittivity modulation to enable nonreciprocal behavior is very promising, the high-Q nature of the resonant tanks leads to lower BWs when compared with nonresonant structures. In addition, varactors provide a low modulation index (the ratio of the maximum and minimum capacitance) compared to the conductivity modulation approach discussed next.

Turning a transistor switch ON and OFF using a modulation signal enables another form of time variance, this time changing the conductance of the medium. The first implementations of a nonmagnetic circulator using conductance modulation have been shown in [29], [34], [79], [90], and [110] using N-path filters [refer to Fig. 3(c)]. An N-path filter is a network of "N" capacitors that are connected to the input and output ports through two sets of switches, where each set of switches is driven with nonoverlapping clocks and has a duty cycle of $(1/N)$. By staggering the modulation signal driving the switches within each path (i.e., imparting a phase shift between the input and output clocks), the N-path filter can achieve phase nonreciprocity that can be used to create a gyrator ($+90°/-90°$ in the forward/reverse direction). Such an architecture has been used in combination with a $3\lambda/4$ transmission line to realize a three-port circulator where the TX, ANT, and RX ports are connected on the transmission line with a $\lambda/4$ spacing [29], [79], [90]. By placing the RX port right at the gyrator, the voltage swing across the gyrator switches can be minimized for a TX excitation, resulting in an improved linearity with respect to TX–ANT propagation. This idea has been implemented in a 65-nm CMOS process and achieves $>$20-dB isolation over 12-MHz BW with a center frequency of 750 MHz using an off-chip antenna tuner to maximize isolation. In addition, the BB signal can be directly extracted from the capacitor voltages of the N-path filter to create a circulator–receiver architecture as shown in [34] and [110]. A similar approach has been taken in [80], by using a similar gyrator and replacing the transmission line with a hybrid coupler to create a circulator–receiver with enhanced BW. The prototype demonstrated in [80] provides $>$30-dB isolation across 190-MHz BW centered around 820 MHz for antenna impedances with VSWRs of up to 1.35 without any on-chip balancing network and is implemented in 65-nm CMOS.

The N-path-filter-based gyrators demonstrated in these works require narrow duty-cycled clocks (such as 12.5% to reduce the transmission losses of the circulator), which complicates the clock generation circuitry and increases its power consumption. Narrow duty-cycled clocks are also challenging to generate at higher frequencies. To adapt the previous technique to mmWave frequencies, an alternate approach of switching transmission lines using clocks with 50% duty cycle has been proposed in [30], [31], and [106]. By switching across transmission lines that provide 90° phase shift at a subharmonic of the modulation

frequency, the clock requirement can be relaxed to push the operating frequency to higher values. A 25-GHz 45-nm SOI CMOS implementation has been shown in [30], [31], and [106], which is clocked at 8.3 GHz and uses C–L–C sections to implement the switched transmission lines [refer to Fig. 3(c)]. This work achieves >18-dB isolation across 4.5-GHz BW with a 50-Ω ANT impedance. By swapping the switched transmission lines with bandpass filters (BPFs) that absorb additional switch parasitics, the operation frequency can be further increased. Nagulu and Krishnaswamy [35] show another circulator prototype implemented in 45-nm SOI CMOS that operates at 53.4 GHz (with a switching frequency of 8.6 GHz) and achieves >20-dB isolation across 6.8-GHz BW.

Furthermore, using a switched transmission line approach with subharmonic clocks and 50% duty cycle can enable the use of less-advanced CMOS nodes with thicker gate oxides that have lower speed but higher power handling. By exploiting this approach and incorporating additional linearity enhancement techniques such as device stacking and optimal switch biasing, an integrated circulator has been demonstrated in 180-nm SOI CMOS [39], [104] that achieves a TX power handling of >1 W (>30 dBm) at 1-GHz operation frequency. In addition, a low-loss inductor-free antenna impedance balancing technique is proposed in this work that enables >25-dB isolation across 160-MHz BW for antenna impedances with VSWRs of up to 1.85.

The highest TX power handling in a CMOS implementation has been achieved in [42] and [99], in which additional improvements in the clock path have been implemented. By incorporating switched-capacitor clock boosting within the clock path, the power handling of such switched transmission line approaches has been enhanced up to 2.5 W. Furthermore, in this work, the chip area and power consumption of the circulator have been reduced by exploiting lower characteristic impedance for the transmission lines and using periodically loaded inductors in their implementation. This work achieves >40-dB isolation across 92-MHz BW for a 1-GHz center frequency and for antenna impedances with VSWRs of up to 2.33.

Many of the previous implementations have limited frequency tuning capability given the limited tuning BW of transmission lines. More recently, transmission-line-free approaches have been investigated that enable ultracompact widely tunable [91] and ultrawideband [43] circulators on-chip. For example, Reiskarimian et al. [91] demonstrate an N-path Shekel circulator implemented in 65-nm CMOS that can be tuned from 0.28 to 1.15 GHz. This work achieves a >20-dB isolation BW of >230 MHz at a 620-MHz operating frequency. Nagulu et al. [43] report an ultrawideband circulator implemented in 65-nm CMOS covering dc–1 GHz with >18-dB isolation across the entire BW. These works report the smallest form factors among on-chip integrated antenna interfaces since no inductors or transmission lines are required in these architectures. However, their power-handling capability is still relatively low (in the order of 1–5 dBm). Other works have also explored switched transmission line architectures using off-the-shelf components [32] and gallium nitride (GaN) technologies [81] to realize ultrawideband circulators. For example, Biedka et al. [81] report the operation from 0.1 to 1 GHz with >16-dB isolation across the band.

3) Antenna Interface FOMs: In [2], two FOMs are reported to compare various antenna interfaces available for FD systems. These FOMs provide a quantitative summary of the various performance metrics of different state-of-the-art antenna interfaces. The first, *antenna interface efficiency*, evaluates the degradation of the PA efficiency in the presence of the antenna interface circuitry needed to enable single-antenna FD possible. This metric takes into account the power consumption of the antenna interface as well as its TX–ANT loss and ANT–RX NF. Intuitively, the lower the antenna interface's power consumption, TX–ANT loss, and ANT–RX NF, the less impact it will have on the PA efficiency.

The antenna interface efficiency FOM, η_{ANT}, can be calculated using the following equation:

$$\eta_{\text{ANT}} = \frac{P_{\text{out,PA}} \times L_{\text{TX–ANT}}/\text{NF}_{\text{ANT-INT}}}{P_{\text{out,PA}}/\eta_{\text{PA}} + P_{\text{dc,ANT-INT}}} \times \frac{1}{\eta_{\text{PA}}} \times 100\% \quad (1)$$

where $P_{\text{out,PA}}$ and η_{PA} are the total output power and drain efficiency of the PA, respectively; and $L_{\text{TX–ANT}}$ and $\text{NF}_{\text{ANT-INT}}$ are the TX-ANT loss and RX NF of the antenna interface with a power consumption of $P_{\text{dc,ANT-INT}}$, respectively. More details related to the derivation of (1) can be found in [2].

Among various approaches listed above, dual-antenna schemes have the potential to achieve high antenna interface efficiency due to the absence of additional circuitry consuming power and adding additional TX–ANT loss and RX noise. This benefit comes at the cost of additional area as was previously discussed. Using orthogonal polarizations for TX and RX within the same antenna footprint is another approach that yields high antenna interface efficiency. For example, in [30], 54.7% antenna interface efficiency has been achieved by using a dual-polarized antenna where the TX and the RX are connected at different physical locations on the same antenna. However, this approach limits the choice of the antenna, and in general, dual-antenna/polarization-based approaches sacrifice MIMO/polarization-multiplexing degrees of freedom (DoFs).

Among single-antenna interfaces, ferrite circulators are the best reported to date (60%–90% η_{ANT}) [2]. The highest η_{ANT} achieved in an integrated nonreciprocal single-antenna interface (27.6%) is reported in [42].

The second FOM defined in [2] is an isolation FBW product and is defined as

$$\text{ISO-FBW} = \text{ISO} \times \frac{\text{BW}}{f_c} \quad (2)$$

Table 1 Summary and Comparison of IC-Based Antenna Interface Implementations

Work	Category	Operating Frequency	TX-RX Isolation	Power Consumption	ANT-RX Noise Figure	TX-ANT Loss	TX Power Handling	Technology/ Area	Efficiency	ISO-FBW Product
ISSCC'20 [99], JSSC'20 [42]	Circulator	0.914–1.086 GHz	>40 dB/92 MHz, >25 dB/172 MHz @1 GHz	39 mW	2.5 dB	−2.07 dB	34 dBm	180 nm/ 9 mm^2	27.6%	>29.6 dB
JSSC'20 [100]	Circulator	5.6–7.4 GHz	>18 dB/1.82 GHz @6.5 GHz	2.5 mW	2.4–3.4 dB	-2.2 dB	N/A	40 nm/ 0.45 mm^2	N/C	12.5 dB
RFIC'20 [101]	Circulator	DC–1 GHz	>18 dB/1 GHz @0.5 GHz	20 mW	3.1–4.1 dB	−3.1 dB	1.4 dBm	65 nm/ 0.19 mm^2	3.6%	>21.0 dB
IMS'20 [102]	EBD	1.5–2 GHz	30 dB/500 MHz @1.75 GHz	0 mW, passive	6 dB	−5.0 dB	10 dBm	65 nm/ 1.5 mm^2	6.3%	24.6 dB
ISSCC'19 [35]	Circulator	50–56.8 GHz	>20 dB/6.8 GHz, >40 dB/1.3 GHz @53.4 GHz	24.14 mW	3.2 dB	−3.6 dB	19.65 dBm	45 nm/ 1.72 mm^2	15.4%	>23.9 dB
ISSCC'19 [103], JSSC'19 [53]	Circulator	2.2 GHz	15 dB/40 MHz @2.2 GHz	156 mW	N/A	−3.7 dB	14 dBm	65 nm/ 2.2 mm^2 per element	8.4%	-2.4 dB
JSSC'19 [37]	Circulator	90/100/105 GHz	46–47 dB/1.5 GHz @100 GHz	17.3–18.6 mW @100 GHz	5.2 dB	−5.6 dB	11.4 dBm	65 nm/ 0.21 mm^2	4.2%	28.8 dB
TMTT'19 [38]	Circulator	0.91 GHz	>20 dB/20 MHz @0.91 GHz	64 mW	5.2 dB	−4.8 dB	N/A	65 nm/ 36 mm^2	N/C	>3.4 dB
IMS'19 [81]	Circulator	0.1–1 GHz	>18 dB/900 MHz @0.55 GHz	4.1 W	3.0 dB	−3.0 dB	N/A	0.2 μm GaN/ 18.5 mm^2	N/C	20.1 dB
ISSCC'18 [80]	Circulator	0.55–0.9 GHz	40 dB/56 MHz, >30 dB/190 MHz @0.8 GHz	24 mW	2.7 dB	−2.6 dB	5.5 dBm	65 nm/ 38.6 mm^2	7.7%	>23.8 dB
ISSCC'18 [48]	EBD	1.6–1.9 GHz	39 dB/200 MHz @1.85 GHz	0 mW, passive	5.6 dB	N/A	N/A	40 nm/ 4 mm^2	N/C	29.6 dB
RFIC'18 [104], JSSC'19 [39]	Circulator	0.86–1.08 GHz	>25 dB/161 MHz @1 GHz	170 mW	3.1 dB	−2.1 dB	30.66 dBm	180 nm/ 16.5 mm^2	23.0%	>17.2 dB
CICC'18 [105]	EBD	1.1–2.5 GHz	31 dB/40 MHz @1.8 GHz	0 mW, passive	N/A	N/A	15 dBm	45 nm/ 1.4 mm^2	N/C	14.5 dB
ISSCC'17 [106], JSSC'17 [30]	Circulator	25 GHz	>18.5 dB/4.5 GHz @ 25 GHz	78.4 mW	3.3–4.4 dB	−3.3 dB	21.5 dBm	40 nm/ 2.16 mm^2	14.9%	>11.1 dB
ESSCIRC'17 [25], JSSC'16 [107]	EBD	120 GHz	>30 dB/14 GHz @ 120 GHz	0 mW, passive	<12 dB[(i)]	−11.0 dB	N/A	40 nm/ 0.015 mm^2	N/C	>10.7 dB
ISSCC'16 [79], JSSC'17 [90]	Circulator	610–850 MHz	20 dB/12 MHz @730 MHz	59 mW	4.3 dB	−1.7 dB	7 dBm	65 nm/ 1.4 mm^2	4.4%	2.2 dB
ISSCC'15 [83], TMTT'16 [23]	EBD	1.9–2.2 GHz	>50 dB/>200 MHz @1.95 GHz	0 mW, passive	<3.7 dB[(i)]	−3.7 dB	27 dBm	180 nm/ 1.75 mm^2	14.5%	>39.9 dB
TMTT'14 [108]	Circulator	62–75 GHz	18 dB/13 GHz @68.5 GHz	N/A	N/A	−7.4 dB	N/A	45 nm/ 1.24 mm^2	N/C	10.8 dB
CICC'14 [109], TMTT'16 [22]	EBD	1.6–2.2 GHz	>40 dB/180 MHz @1.9 GHz	0 mW, passive	N/A	−3.2 dB	22 dBm	180 nm/ 0.35 mm^2	N/C	>29.8 dB

[(i)] Obtained from the ANT-RX insertion loss of the antenna interface.
[(ii)] Distributed PA architectures have lower efficiency which is not being considered here.
[(iii)] NF: Noise Figure; ISO-FBW Product: Isolation-Fractional Bandwidth (FBW) Product (see (2) in Section III-B2)
[(iv)] N/A: Not Available/Applicable, i.e., metric was not reported in the specific implementation. N/C: Not Computable.

where ISO-FBW is the isolation FBW product, ISO is the TX-to-RX isolation of the antenna interface, and BW/f_c is the FBW or the ratio of the isolation BW of the antenna interface to its center frequency.

Table 1 provides a summary of some of the recent works on antenna interfaces. We refer the reader to [2] for a more comprehensive comparison. Fig. 4(a) and (b) shows the performance of various recent antenna interface implementations in terms of isolation obtained as a function of the BW and FBW, respectively. Fig. 4(c) captures the tradeoffs between the canceller efficiency and ISO-FBW product in these recent implementations.

IV. RF AND ANALOG-BB SIC CIRCUITS

A. Introduction to SIC Circuits

As illustrated in Fig. 1, in order to further reduce the effects of SI, a reference signal is extracted from the TX (at the RF and BB), fed through the RF and BB SI cancellers, and SIC is performed at the RF and BB domains of the RX. This article provides a comprehensive overview of three distinct types of SI cancellers that employ different approaches. These include: 1) phase-based SI cancellers; 2) time-domain cancellers with parallel delay taps in the RF and/or analog-BB domains; and 3) frequency-domain cancellers in the RF domain that utilize parallel RF BPF taps. To ensure a quantitative and equitable comparison, akin to the integrated antenna interfaces, we introduce two FOMs for integrated cancellers: 1) the canceller efficiency and 2) the SIC-FBW product.

B. Phase-Based SI Cancellers

Phase-based SI cancellers are the most basic form of a canceller in which a copy of the SI is generated by tapping the TX signal and scaling its amplitude and phase such that it matches the SI channel's response [45], [50], [52], [57], [111]. In Section VII, we will discuss algorithms that adaptively configure phase-based SI cancellers. However, such frequency-flat cancellers can only emulate the amplitude and phase of the SI channel at a single-frequency point. Wireless environments are usually very complex and the SI channel is not frequency-flat due to the effect of multipath fading. Thus, phase-based cancellers are limited to low cancellation BWs. To tackle this issue, the canceler's frequency response should match that of the SI channel

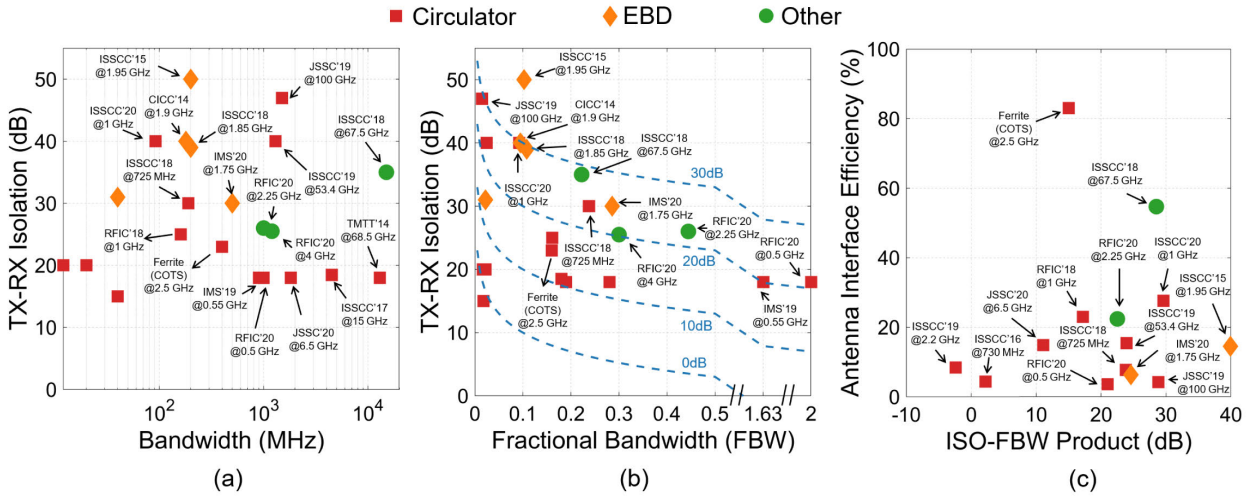


Fig. 4. *Achieved TX-to-RX isolation of different integrated shared antenna interfaces is presented as a function of (a) isolation BW and (b) FBW, where constant isolation FBW products are indicated by contour lines. (c) Antenna interface efficiency achieved by various integrated shared antenna interfaces is depicted as a function of the isolation FBW product.*

across the entire desired BW. This is typically done using: 1) time-domain cancelers, which use the multiple delay to create a tunable finite impulse response (FIR) filter whose taps are tuned to resemble the SI channel, or 2) frequency-domain cancelers, which uses a bank of parallel tunable BPFs to provide different amplitude and phase responses at different center frequencies. Thus, we require the use of time- or frequency-domain cancelers to obtain wideband cancellation.

C. Time-Domain SI Cancellers

Time-domain cancellers tap a portion of the TX signal, which is subsequently passed through multiple taps, each imparting a distinct amount of delay to the signal. These taps generate multiple parallel outputs that are then subjected to distinct weights (e.g., amplification/attenuation) and phase shifts. By recombining these parallel outputs, an FIR filter is realized in the RF or analog domain [refer to Fig. 5(a)]. The tap weights and phase shifts are chosen to ensure that the FIR filter closely resembles the frequency response of the SI channel across the desired wide BW. The resulting output from the FIR filter is injected into the RX path, where RF or analog baseband SIC is achieved.

Several methods have been proposed for implementing integrated time-domain RF cancellers using different techniques to incorporate true time delays in ICs [47], [48], [51], [53], [54], [55]. Fundamentally, wideband true time delays can be achieved through the utilization of transmission lines [Fig. 5(c)]. The amount of delay obtained through transmission lines is proportional to the length of the line. Nanosecond-level delays are necessary to effectively accomplish RF SIC across a broad frequency range for typical wireless antenna interfaces. However, implementing transmission lines with nanosecond-scale delays, especially in cases involving multiple delay taps, requires a considerably large area, making it impractical for compact IC designs. For instance, achieving a nanosecond delay in silicon typically demands a delay line measuring approximately 15 cm in length. Printed circuit board (PCB) implementation of such delays has been shown [6] but is impractical to be realized on-chip due to the large form factor. Such PCB-based passive implementations have high linearity due to their entirely passive nature and can be utilized in base stations (BSs) as the large form factor can be accommodated in BSs.

Techniques to implement miniaturized delay lines to realize integrated compact time-domain SI cancellers have been extensively investigated. Miniaturized delay lines enable implementing a wideband size- and cost-constrained FD systems (e.g., systems with handheld devices). One approach for achieving approximate true time delays on ICs is through the use of first-order RC–CR all-pass filters (APFs) [47], [48] [Fig. 5(e)]. These passive RF canceller implementations offer advantages such as low power consumption, high linearity, and compact form factor due to the absence of inductors. However, these filters produce delays that are inversely proportional to the operating frequency, making it challenging to achieve large delays at higher frequencies, such as 1 GHz. For example, previous studies have realized RC–CR filters with nominal delays of up to 65 ps [47], and by cascading multiple delay elements, delays of up to 250–300 ps have been implemented in five-tap FIR filters. These cancellers have achieved 50-dB cancellation across a 42-MHz BW at a 1.9-GHz operating frequency with a 50-Ω termination at the antenna port [48]. Furthermore, Gm-C-based APFs have also been used to generate delays for BB frequencies as RC–CR filters require a large form factor for lower frequencies [Fig. 5(d)].

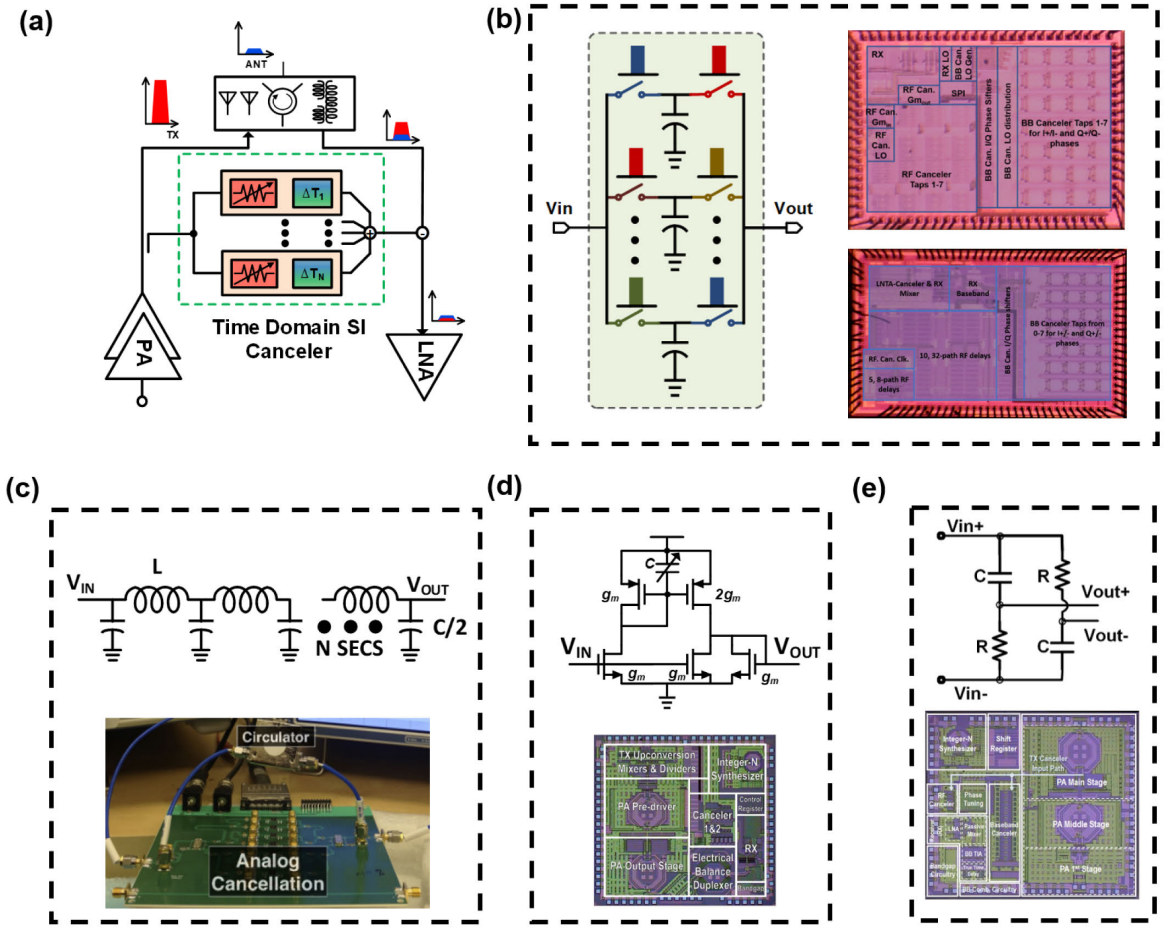


Fig. 5. *(a) Time-domain implementation of an SI canceller. (b) Delay generation using N-path-based switched-capacitor circuits [54], [55] and the chip photographs of the implemented cancelers. (c) Delay generation using passive delay lines with the implemented PCB prototype to demonstrate the technique [6]. (d) Delay generation using Gm-C APFs and the chip photograph of the implemented canceler [48]. (e) Delay generation using RC–RC APFs and the chip photograph of the implemented canceller [47].*

Another technique for achieving large true time delays with small form factors involves the sample-hold-and-release principle in switched-capacitor circuits [Fig. 5(b)]. By periodically sampling the input signal onto a capacitor and sensing the voltage across the capacitor using a switch controlled by a delayed clock, a true time delay can be applied to the input. The BW of this circuit is proportional to the clocking frequency, and the maximum delay is proportional to the clocking period. To overcome the tradeoff between BW and maximum delay, nonoverlapping layers of switched-capacitor structures can be used. By using N parallel nonoverlapping layers, the delay–BW product can be enhanced N times, allowing for larger delays with the same BW or vice versa [54], [55]. Using 32-path filter taps clocked at 125 MHz, delays up to 7.75 ns are achieved [55].

Furthermore, downconverting the RF signal into BB, applying delays in BB, and then upconverting the delayed signal back to the RF domain is another technique for obtaining RF delays. This approach enables complex-valued weighting of the RF canceller taps by utilizing I/Q paths in the BB. In previous studies, delays in BB were implemented using RC low-pass filters, and FIR filters with two taps achieved 23-dB SIC across an 80-MHz BW at a 900-MHz operating frequency [112]. Another implementation utilized delays generated in BB within a passive mixer-first architecture, achieving a total RF SIC of 28 dB across a 100-MHz BW at a 2.7-GHz operating frequency, in conjunction with an explicit analog-BB canceller [51].

In Section VII, we will discuss algorithms that adaptively configure time-domain SI cancellers.

D. Frequency-Domain SI Cancellers

Frequency-domain equalization (FDE)-based SI cancellers use multiple frequency-separated BPFs in parallel that span the desired BW for cancellation. A portion of the TX signal is tapped and passed through a bank of reconfigurable RF BPFs. The SI channel is recreated in the frequency domain by summing the individual filter tap responses and RF SIC is performed at RF [refer to Fig. 6(a)]. A second-order BPF has four DoFs, namely,

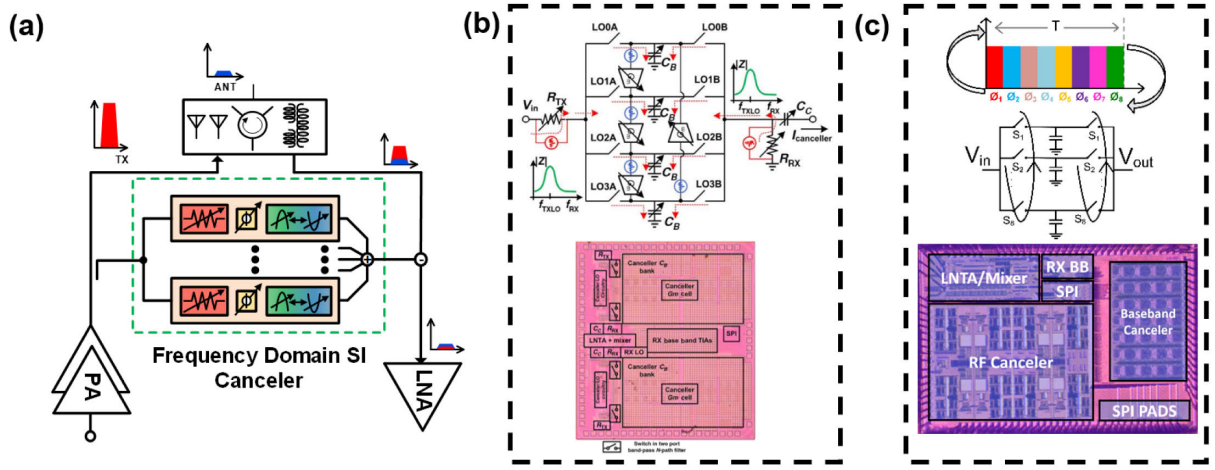


Fig. 6. *(a) Frequency-domain implementation of an SI canceller. (b) Implemented BPFs based on Gm-C frequency shifted N-path filters [44] and the chip photograph of the implemented canceler. (c) Implemented BPFs based on rotary clocking N-path filters [73] and the chip photograph of the implemented canceler.*

gain, phase, quality factor, and the center frequency of the filter, in contrast to time-domain equalization-based filter taps typically showing two or three DoFs (delay, gain, and possibly phase). This ensures that the SI channel can be emulated not only in amplitude and phase but also in the slope of the amplitude and the slope of the phase (i.e., group delay). A BPF tap can viewed as a narrowband delay response introducing a tunable delay to the signal using a tunable quality factor.

LC-based implementations of filters [113] are quite bulky, especially when reconfigurability is required, and therefore are impractical for CMOS implementations. Similar to time-domain cancellers, PCB implementations such as [113] can be utilized in BSs but are not amenable for applications requiring small form factors. N-path filters are an emerging solution to building compact, tunable, high-Q, and high linearity BPFs on chip. The quality factor and phase of a two-port N-path filter can be easily tuned by varying the path capacitance and the delay between the input and output switches. Variable attenuation can be introduced through resistive dividers [44]. The frequency is programmable by varying the clock frequency, but it is undesirable to have separate clock synthesizers for each frequency tap due to the increased power consumption and coupling between the synthesizer PLLs resulting in spurs. The FDE-based RF canceller in [44] utilizes the active Gm-C approach introduced in [114] to frequency-shift the N-path BPFs by inducing current injection between different paths in either the clockwise or counterclockwise direction [Fig. 6(b)]. Active transconductors are used to induce current, and the frequency offset produced is proportional to the ratio of transconductance to the path capacitance. This leads to higher power consumption when targeting larger cancellation BWs along with large quality factors (narrowband delays) while also adding noise. Using two frequency-shifted N-path BPFs, Zhou et al. [44] could achieve 20-dB RF SIC across 25-MHz BW at 1.37-GHz operating frequency (with 30-dB initial isolation achieved by an antenna pair) while having a dc power consumption of ∼90–180 mW. Improved versions of this RF SI canceller are implemented in the COSMOS testbed [66] and will be further discussed in Section VIII-D. Algorithms for adaptive configuration of this RF SI canceller will be discussed in Section VII.

A fully passive approach to frequency shift N-path filters has been introduced in [115] using rotary clocking. The proposed technique periodically rotates the clock phases driving the various path switches in an N-path filter in a clockwise or anti-clockwise manner, creating a staircase approximation of a phase ramp or, equivalently, a frequency shift. Specifically, rotating P phase units (a single phase unit is equal to $360^\circ/N$ in an N-path filter), every Q clock cycles in a clockwise or anti-clockwise manner would produce a frequency shift of $\pm Pf_c/QN$ (where f_c is the clocking frequency). This enables very large frequency shifts (up to 25% of the clocking frequency) with fine resolution and very low power consumption. Further power reduction and spur mitigation techniques were introduced in [73] [Fig. 6(c)]. An RF SI canceller using eight rotary-clocked eight-path filters with 20 different center frequencies, 3-bit phase and 9-bit quality factor programmability is reported. A closed-loop algorithm optimizing RF SIC achieved 23 dB of RF SIC over 160-MHz BW at 720-MHz operating frequency, consuming 7.2 mW per RF canceller tap while handling SI powers up to −12 dBm at the RX input. Large frequency shifts enabled placing filters across a broader spectrum resulting in very large fractional cancellation BWs (22.2% FBW).

E. Requirements and Methods for Tunability and Calibration

As the wireless environment is constantly changing, the frequency response of the SI channel changes in real

Table 2 Summary and Comparison of IC-Based RF/Analog-BB Canceller Implementations

Work	Category	Operating Frequency	SIC/ Bandwidth @Frequency	Canceller Power Consumption	Rx NF (NF degradation with canceller)	SI Power Handling	Technology/ Area	Canceller Efficiency	SIC-FBW Product
RFIC'23 [73]	Freq.-domain	0.1–1.0 GHz	31 dB/120 MHz @740 MHz	43.6 mW (RF and BB)	4.1 dB (5.2 dB)	−12 dBm	65 nm/ 10.9 mm^2	13.7%	23.1 dB
ISSCC'21 [55]	Time-domain	0.1–1.0 GHz	42 dB/40 MHz @800 MHz	44.8 mW (RF and BB)	3.7 dB (0.8 dB)	−12 dBm	65 nm/ 7.2 mm^2	43.5%	29.0 dB
JSSC' 22 [148]	Amp. & Phase-based	28/37 GHz	25 dB/100 MHz @28 GHz	N/A (Rx total: 98.75 mW)	7.9 dB (N/A)	N/A	65 nm/ 1.05 mm^2	N/C	0.5 dB
RFIC'20 [54]	Time-domain	0.1–1.0 GHz	30 dB/20 MHz @738 MHz	32 mW (RF and BB)	5.3 dB (1.9 dB)	−13 dBm	65 nm/ 5.15 mm^2	31.4%	14.3 dB
JSSC'19 [53]	Time-domain	1 (BB)	SIC: 30 dB/20 MHz, 2×2 CT-SIC: 23 dB/20 MHz @2.2 GHz	25 mW, per element	11.2 dB (1.7 dB)	−1 dBm	65 nm/ 2.8 mm^2, per element	21.0%	9.6 dB
JSSC'20 [52]	Amp. & Phase-based	28/37/39 GHz	26 dB/500 MHz @28 GHz	N/A (Rx total: 37.6 mW)	6.2 dB (N/A)	N/A	65 nm/ 0.48 mm^2	N/C	18.5 dB
JSSC'20 [51]	Amp. & Phase-based	0.5–2.5 GHz	SIC: 29 dB/20 MHz, 2×2 CT-SIC: 24 dB/20 MHz @900 MHz	16–62 mW, per element	3.1 dB (1.3 dB)	−5 dBm	65 nm/ 3 mm^2	60.3%	12.5 dB
RFIC'19 [50]	Amp. & Phase-based	0.5–3.5 GHz	35 dB/10 MHz @2 GHz	4–12 mW	3.3 dB (2 dB)	−25 dBm	65 nm/ 1.5 mm^2	16.3%	12.0 dB
JSSC'18 [49]	Amp. & Phase-based	60–75 GHz	25 dB/2 GHz @65 GHz	0 mW, passive	4.8 dB (<0.1 dB)	−24.5 dBm	45 nm/ 7.3 mm^2	86.9%	9.9 dB
ISSCC'18 [48]	Time-domain	1.6–1.9 GHz	31 dB/40 MHz @1.77 GHz	14.3 mW	2.5 dB (1.6 dB)	N/A	40 nm/ 4.0 mm^2	N/C	14.6 dB
JSSC'18 [47]	Time-domain	1.7–2.2 GHz	50 dB/42 MHz @1.9 GHz	3.5 mW (RF), 8 mW (BB)	4 dB (1.55 dB)	−13 dBm	40 nm/ 3.5 mm^2	48.0%	33.4 dB
TCAS-I'18 [46]	Time-domain	0.9 GHz	23 dB/80 MHz @900 MHz	13 mW	9.6 dB (1.4 dB)	N/A	130 nm/ 0.72 mm^2	N/C	12.5 dB
JSSC'18 [45]	Amp. & Phase-based	1–3 GHz	20 dB/15 MHz @2.3 GHz	0 mW, passive	4 dB (0.4 dB)	−5 dBm	28 nm/ 0.5 mm^2	71.7%	−1.9 dB
JSSC'15 [44]	Freq.-domain	0.8–1.4 GHz	20 dB/25 MHz @1.37 GHz	44–91 mW, per tap	4.8 dB (1.3 dB)	−8 dBm	65 nm/ 4.0 mm^2	32.5%	2.6 dB

(i) NF: Noise Figure; SIC-FBW Product: SIC-Fractional Bandwidth (FBW) Product (see (4) in Section IV-F).
(ii) N/A: Not Available/Applicable, i.e., metric was not reported in the specific implementation. N/C: Not Computable.

time, and it is necessary for the canceller to have the ability to adjust its parameters in response to changes in the channel. In phase-based cancellers, the only possible DoFs are amplitude and phase. These are usually achieved through tunable passive attenuators and phase shifters. The tunable range of the attenuator should be sufficient to span the desired level of isolation to be canceled, and the resolution of tunability determines the peak cancellation achieved.

In time-domain cancellers, the DoFs usually include the gains associated with each of the delay taps. This is usually realized by either tunable attenuators [6] or active variable gain amplifiers (VGAs) [47], [48], [54], [55]. Additional DoFs include tunable delays, which can either be realized by having tunable capacitors in passive implementations or introducing delay in the clock path for switched-capacitor implementations [55]. Furthermore, introducing an additional phase shift in each time-domain tap, which effectively realizes a complex gain for the taps, can be utilized to obtain more DoFs to better adapt to the varying SI channel.

Frequency-domain cancellers typically use four DoFs as mentioned earlier: 1) the gain of the BPF at the center frequency; 2) the phase shift at the center frequency; 3) the quality factor of the filter; and 4) the center frequency of the filter [44], [73]. Passive implementations of LC-BPFs usually use attenuators and phase shifters after the BPF to obtain the first two DoFs and incorporate tunable inductors and capacitors to realize the remaining two DoFs [113]. N-path filter-based implementations have phase shifting built into the filter itself [116]. The quality factor can be independently tuned by varying the path capacitance of these filters. Center frequency shifting is accomplished by inducing current between different paths [44], [114] or by modifications in the clock path to effectively realize a clock at a different frequency [73], [115]. The gain tunability is usually realized independently by VGAs similar to time-domain implementations or embedding resistive attenuators.

F. Performance Evaluation of SIC Circuits

An effective canceller should provide sufficient SIC across the desired BW at a specific center frequency while also handling a high power level of the SI signal. In addition, it should introduce minimal degradation to the receiver's NF. However, these metrics tend to trade off with each other in realistic IC designs. To provide a quantitative summary of the performance of these cancellers, we use two FOMs for SI cancellers based on [2] and describe different state-of-the-art cancellers based on these metrics in Table 2.

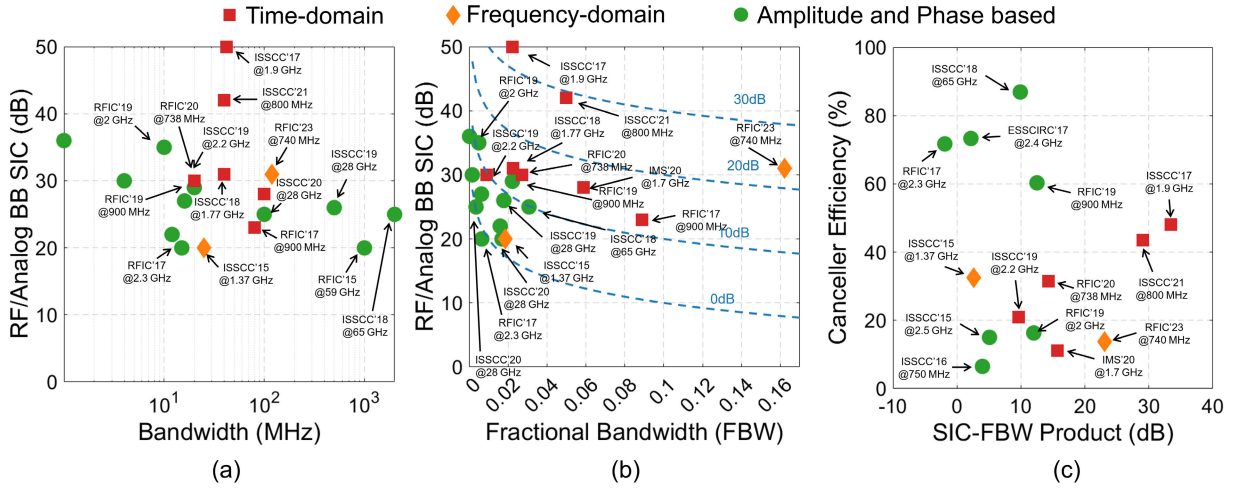


Fig. 7. *SIC achieved by various integrated cancellers in RF and/or analog-BB domains as a function of (a) SIC BW and (b) FBW (with contours indicating constant SIC FBW product). (c) Canceller efficiency achieved by various integrated cancellers as a function of the SIC FBW product.*

1) Canceller Efficiency: The efficiency of the canceller (η_{CANC}) quantifies the reduction in PA efficiency caused by incorporating additional circuitry to enable FD communication with a shared antenna. We consider an FD radio that comprises a PA producing a total output power $P_{\text{out,PA}}$, with a drain efficiency of η_{PA}, and a canceller with an added TX–ANT loss of $L_{\text{TX–ANT,Canc}}$, NF degradation of NF_{Canc}, and dc power consumption of $P_{\text{dc,Canc}}$. For a fair comparison, it is assumed that a -10-dB coupler is used to inject TX power into the canceler, which leads to the added TX–ANT loss ($L_{\text{TX–ANT,Canc}}$). Table 2 assumes a nominal $\eta_{\text{PA}} = 30\%$. The effective transmitted power of the wireless link, compared to the case without any additional loss or NF penalty, can be represented as

$$\eta_{\text{CANC}} = \frac{P_{\text{out,PA}} \times L_{\text{TX–ANT,Canc}}/\text{NF}_{\text{Canc}}}{P_{\text{out,PA}}/\eta_{\text{PA}} + P_{\text{dc,Canc}}} \times \frac{1}{\eta_{\text{PA}}} \times 100\%. \quad (3)$$

2) Isolation FBW Product: The isolation FBW product is obtained by multiplying the amount of SIC and the FBW over which the cancellation is achieved. Ideally, we would prefer to define the FBW as a performance metric for the canceller at a fixed target cancellation level. However, since different studies often report varying cancellation levels, we have chosen to define the FOM as the product of the amount of SIC and FBW. The equation that represents this is

$$\text{SIC-FBW} = \text{SIC} \times \frac{\text{BW}}{f_c} \quad (4)$$

where SIC-FBW represents the isolation FBW product for an antenna interface that provides an isolation of SIC over a BW of BW centered at a frequency of f_c.

Fig. 7(a) and (b) shows the performance of various recent SI canceller implementations in terms of SIC obtained as a function of the BW and FBW, respectively. Fig. 7(c) captures the tradeoffs between the canceller efficiency and SIC-FBW product in these recent implementations.

V. DIGITAL SIC TECHNIQUES

The goal of digital SIC is to remove any residual SI remaining after the antenna interface isolation and analog cancellation stages. As discussed in Sections III and IV, the isolation and analog cancellation stages are crucial in order to avoid saturation at the RX, which would result in desired signal desensitization. A system solely reliant on digital SIC would require an analog-to-digital converter (ADC) with a significantly large dynamic range capable of handling the SI; assuming an SI approximately 90 dB larger than the desired signal, the effective number of bits (ENoB) required by an ideal ADC would be

$$\text{ENoB} \approx \frac{\text{DR} - 1.76}{6.02} \approx 15 \text{ bits}. \quad (5)$$

By initially reducing the SI power by isolation and analog cancellation methods, the resolution requirements of the ADC can likewise be eased.

As each FD radio has perfect knowledge of its intended TX signal's digital representation, removing it from the SI signal is theoretically straightforward. This is done by passing the ideal TX signal through an SI channel model and subtracting the result from the measured RX signal in the digital domain, thereby completing the final cancellation stage and obtaining the desired signal. However, the presence of nonlinearities and nonidealities complicate this task, especially as transmission power increases and these effects become more prominent in both TX and receiver components [7], [8]. Many different digital cancellation approaches have been proposed to address this challenge,

several of which are based on DSP methods and others, especially in recent years, attempting machine learning (ML) and deep learning (DL) solutions.

A. DSP-Based Approaches

Traditionally, DSP principles have been employed to analyze and model the SI channel's linear and nonlinear components. These principles have extended to modeling individual components of the TX and RX signal processing chains, including both intended and nonideal behavior at each stage of the chains. In this section, we will introduce some of the major linear, nonlinear, and hardware modeling approaches that have been utilized for digital SIC.

1) Linear Approaches: A low-complexity approach is to utilize the least-squares (LS) algorithm to estimate the SI channel in the frequency domain [56]. This is well suited for orthogonal frequency-division multiplexing (OFDM) systems such as that implemented in [6], as predefined training symbols are intrinsically defined on individual subcarriers. The training symbols are transmitted during designated "quiet times," ensuring that there is no desired received signal from another wireless TX, thereby isolating the SI channel.

Specifically, let $\mathbf{X} = (X[0], \ldots, X[N-1])$ be the vector of training symbols across N subcarriers for a single OFDM symbol and M be the total number of OFDM symbols. Let $Y^{(m)}, m = 1, \ldots, M$, be the corresponding received signal. Then, the LS estimate of the SI channel $\hat{H}_{\mathrm{SI}}$ at subcarrier k is

$$\hat{H}_{\mathrm{SI}}[k] = \frac{1}{M}\left[\frac{1}{X[k]}\left(\sum_{m=1}^{M} Y^{(m)}[k]\right)\right]. \tag{6}$$

The estimated SI channel can thus be used to define an FIR filter, to be used in the same fashion as the analog RF cancellers; the transmitted signal is fed through the filter and subtracted from the received signal to perform cancellation. As implemented with radio hardware in [56], the LS approach achieved about 30 dB of digital cancellation across a 10-MHz BW. Other linear channel estimators include the maximum-likelihood [117] and minimum mean squared error (MMSE) [118] estimators.

The LS approach has been extended to widely linear channel models [7], which model direct-conversion architectures with the potential for in-phase/quadrature (IQ) mixer-generated image components and imbalances in phase and amplitude. To account for these effects, a complex conjugate of the transmitted signal is fed through a second linear FIR filter and combined with the output of the first, recreating the image effect in addition to the primary SI path. In simulations, the widely linear LS approach was shown to give a performance boost of almost 50 dB across a 12.5-MHz BW over traditional linear approaches at low TX power. At higher TX powers, the performance boost drops to approximately 15 dB.

Adaptive filtration approaches build on the linear channel estimators to improve nonlinearity handling and to provide the additional capacity to address evolving environmental conditions. Such approaches include using the least-mean-square (LMS) algorithm [74], the recursive LS (RLS) algorithm [119], and Kalman filtering [59]. The LMS approach provides between 25 and 35 dB of digital cancellation, and the RLS and Kalman filter approaches both indicate improved performance in simulation compared to the traditional nonadaptive LS approach.

2) Nonlinear Approaches: They generally consider a subset of hardware nonlinearities and have shown better performance (by approximately 25–30 dB) than traditional linear approaches alone, especially at higher transmit powers. Primary nonlinear approaches include polynomial models [60], the Volterra series [75], the Hammerstein model [76], the Wiener–Hammerstein model [120], and Itô–Hermite polynomials [121]. These methods, though effective, suffer from high implementation complexity, due to the necessarily high number of estimated parameters, especially as the nonlinearity order grows. Principal component analysis (PCA) methods have been proposed to reduce the complexity by focusing on the most significant nonlinearity terms with minimal impact on cancellation performance [122], but they require costly transformation matrix multiplies and reruns whenever the SI channel changes significantly.

3) Hardware Modeling Approaches: Much work has been performed in modeling the effects of nonlinearities at each stage of the transmit and receive chains. PA nonlinearities, at varying output power levels, were modeled in [7], [123], [124], and [125]. IQ imbalance effects were modeled in [7] and [124]. ADC and digital-to-analog converter (DAC) nonlinearities were modeled in [124]. Phase noise effects were modeled in [126], [127], and [128]. A comprehensive model for single-antenna, direct-conversion FD systems is presented in [129] and considers the nonlinearities of RF components, IQ imbalances, phase noise effects, and receiver NF.

B. Machine Learning-Based Approaches

Recently, the integration of ML and DL into physical layer communication systems has been studied [65]. In the same vein, these approaches have been applied to FD communications as a means of providing strong digital SIC with lower computational complexity, faster convergence speed, and improved steady-state performance compared to traditional nonlinear SIC methods [64], [130].

A multilinear regression model is proposed in [130], with complex-valued weights and biases learned iteratively, using the transmitted data as a training source, via gradient descent in real time, achieving 50 dB of digital SIC against self-interfering tones. A Gaussian mixture model is used in [131] to detect received signals without any direct digital SIC by expectation–maximization (EM) clustering

and cluster labeling, thereby achieving 2× throughput in simulation. Linear and nonlinear support vector machine (SVM) regression was studied as a cancellation approach in [132]. ML has similarly been used to model hardware nonlinearities, as in [133], which characterized commercial PA behavior using methods such as decision trees, random forests, gradient boosting, and k-nearest neighbors, trained and tested on 300 000 measured data samples from two BS PAs at a single output power level and two BWs (60 and 100 MHz). However, the authors report that most of these approaches (with the exception of gradient boosting) performed worse than the nonlinear memory polynomial approach. As with DSP-based hardware modeling approaches, ML-developed models can likewise be used in conjunction with other digital SIC approaches.

1) Neural Network Approaches: Neural networks (NNs) and DL approaches have been widely studied as ways to model and compensate for nonlinearities in wireless communications [134], [135], to reduce training time and resource demand in end-to-end systems [65], and to facilitate channel estimation and signal detection [136]. Due to their powerful nonlinear modeling capabilities, these approaches have been adapted for digital SIC and have proved to provide a good tradeoff between computational complexity and cancellation performance [137].

A simple feedforward NN (FFNN) canceller is proposed in [64] and implemented in hardware — both FPGA and ASIC — in [138]. The FFNN was trained using OFDM frames consisting of approximately 20 000 BB samples, of which 90% were used for training and 10% for computing the SIC. This canceller was shown to achieve similar cancellation levels (−45 dB across a 10-MHz BW) as the polynomial-based nonlinear canceller of [125] (with an equivalent training scheme) with lower resource utilization (0.47× the number of required DSP slices) and 81% higher hardware efficiency. More advanced NN architectures, such as recurrent NNs (RNNs) and complex-valued NNs (CVNNs), were studied in [139] in comparison to FFNN cancellers and traditional polynomial models, with the conclusion that — at equivalent cancellations of −45 dB across a 10-MHz BW — deep CVNNs require the least amount of floating-point operations and parameters compared to other models. Two novel NN architectures, ladder-wise grid structures (LWGSs) and moving-window grid structures (MWGSs), were proposed in [140] with the goal of modeling the memory effect of SI channels in addition to other nonlinearities. LWGSs and MWGSs showed complexity reductions of −49.9% and −34.2%, respectively, in terms of floating-point operations for equivalent cancellations of −45 dB across a 10-MHz BW. Time-varying channels are addressed in [141], which proposes a deep NN (DNN) that decouples the reconstruction of nonlinear SI components from the estimation of the SI propagation channel in order to eliminate the need for online training.

VI. OPPORTUNITIES IN MULTIANTENNA SYSTEMS

Multiple-antenna phased-array technologies are widely used in 5G systems due to their ability to increase link range and reject spatial interference through beamforming. In addition, MIMO technology can significantly improve the capacity and reliability of wireless networks and is an integral part of current and future wireless communication systems. Combining the benefits of FD with multiantenna technologies has been investigated in the recent past. In the following, we briefly review some of these works.

A. FD Phased Array

Phased arrays can substantially enhance the range in FD links that are challenged from a TX power handling and RX noise perspective. However, combining FD operation with phased-array beamforming is a significant challenge because, aside from the SI from each TX to its own RX, there exists crosstalk SI (CTSI) between every TX–RX pair.

In [142], a 730-MHz four-element phased-array FD receiver IC with on-chip circulators is implemented in a 65-nm CMOS technology that achieves SIC through repurposing beamforming DoFs (namely, the amplitude and phase of weights applied to each element) within the TX and RX without the need to incorporate separate cancellers. FD phased-array measurements were performed in a 2 × 4 array using two ICs tiled on a PCB. By configuring the beamforming DoFs within this structure, up to 50-dB array SIC has been demonstrated over a 16.25-MHz BW at the cost of 3-dB lower array gain for TX and RX. In addition, by using nonlinear digital SIC, a total of 100-dB total array SIC has been reported. Building on top of this result, we further investigated the design of adaptive beamforming algorithms scalable to larger phased arrays in [143].

Furthermore, an integrated 4 × 4 array of interconnected circulators (referred to as a Floquet topological insulator) in combination with off-the-shelf transceivers was implemented in [144] and shown to enable 4 × 4 FD phased-array beam-steering capability and demonstrated up to 44-dB SIC across 20-MHz BW.

B. FD MIMO

The main challenge associated with FD MIMO radios is simultaneous SI and CTSI suppression. The problem of CTSI suppression is even more challenging compared to the phased-array case since multiple streams of data can be received by the FD MIMO receiver all at once. In an MIMO FD radio, CTSI exists between every pair of antennas, causing the number of required cancellers to grow quadratically.

In [145], an FD MIMO radio has been reported that exploits the correlation between SI and CTSI to share cancellation delay taps and reduce canceller complexity. Using off-the-shelf components, Bharadia and Katti [145]

achieve 68–70 dB of SI and crosstalk interference cancellation. Digital beamforming can also be used to achieve SIC in many-antenna FD radios as demonstrated in [146]. However, since this work offers no SIC or CTSIC prior to the digital domain, the RF front end requires extremely high dynamic range to avoid saturation. A PCB implementation of a 2 × 2 FD MIMO was presented in [147] using dual antennas for each TRX. The implementation in this work is bulky due to the lack of a shared antenna interface, significant canceller complexity, and large delay lines.

More recently, Dastjerdi et al. [53] reported the first RF FD 2 × 2 MIMO IC with on-chip circulators that feature area- and power-efficient passive RF and active BB cancellers with shared delay elements. This work has achieved up to 35/45 dB of SI and 42/53 dB of CTSI cancellation across 40-/20-MHz BW with 2-dB degradation in receiver NF across an antenna VSWR of 2:1. Cao and Zhou [51] have also reported an RF 2 × 2 MIMO FD receiver that implements self-adaptive RF SIC using an LMS algorithm.

FD MIMO receivers have also been implemented on-chip at mmWave frequencies as reported in [52] and [148]. In [52], a multiband 28-/37-/39-GHz MIMO receiver with hybrid beamforming is proposed for FD applications that achieves a peak RF SIC of 36 dB and 500-MHz BW with >26-dB SIC. The high BWs used at mmWave, for example, up to 400 MHz for 5G NR FR2, with even larger aggregated BWs [149], pose a system-level challenge to achieve FD capability. Not only must the circuit-level design be capable of handing such BWs but also the digital SIC methods outlined in Section V. Machine learning-based approaches, while promising for handling complex channel effects, are not currently able to handle the wide BWs used in mmWave 5G systems.

VII. SYSTEM CONFIGURATION ALGORITHMS

In this section, we describe the algorithms utilized to configure the programmable ICs discussed in Section IV. Fig. 1 illustrates an adaptive configuration algorithm that can be utilized to configure both an RF SI canceller and an analog-BB SI canceller. We start by introducing some notation and describing the mathematical framework for the system configuration algorithm. Then, we describe the specific algorithms utilized to configure: 1) the phase-based SI canceller from Section IV-B; 2) the multistage time-domain SI canceller from Section IV-C; and 3) the FDE-based SI canceller from Section IV-D.

A. Mathematical Framework

Let B be the BW of interest for wireless communication. We divide B into K nonoverlapping subchannels indexed by $k \in \{1, 2, \ldots, K\}$ and denote the central frequency of subchannel k by f_k. The frequency response of the *SI channel* at f_k is represented by the complex number $H_{\text{SI}}(f_k)$, with an amplitude of $|H_{\text{SI}}(f_k)|$ and phase of $\angle H_{\text{SI}}(f_k)$. The frequency response of the *SI canceller, configured with parameters* $\boldsymbol{\theta} \in \Theta$, is given by $H_{\text{canc}}(f_k, \boldsymbol{\theta})$, where Θ is the *admissible configuration space* containing every parameter combination allowed by the SI canceller. Naturally, the structure of the admissible configuration space Θ can be different for different SI cancellers.

In general, the goal of the configuration algorithms is to find the optimal canceller parameter $\boldsymbol{\theta}^\star \in \Theta$ which maximizes SIC, namely

$$\boldsymbol{\theta}^\star := \arg\min_{\boldsymbol{\theta}\in\Theta} \sum_{k=1}^{K} |H_{\text{SI}}(f_k) - H_{\text{canc}}(f_k, \boldsymbol{\theta})|^2. \tag{7}$$

The configuration algorithms described next attempt to solve this optimization problem for specific SI canceller implementations.

B. Configuration of the Phase-Based Canceller

As described in Section IV-B, we demonstrated the implementation of a phase-based SI canceller [57], [61] based on the RFIC that we developed in [150], whose modeling and optimization were presented in [151] and [152]. Specifically, for a phased-based canceller with a single tap, the goal is to match the frequency response of the canceller to that of the SI channel *at a single frequency*. This is achieved by tuning the amplitude of the canceller to match with that of the SI channel at a selected frequency and then adjusting the phase such that the SI is suppressed to the minimum level. As a result, this phased-based canceller has a limited cancellation BW, as we demonstrated in [57], [61], and [68].

C. Configuration of the Multistage Time-Domain Canceller

As described in Section IV-C, the *integrated* time-domain canceller developed in [55] is composed of 16 *RF taps*, each with a programmable gain $\alpha_n^{\text{RF}} \in [0, 1], \forall n \in \{0, 1, \ldots, 15\}$ and a programmable delay $\tau_n^{\text{RF}} \in \{0, 0.25, \ldots, 7.75\}$ ns, and eight *BB taps*, each with a programmable complex-valued gain $\beta_m^{\text{BB}} + j\gamma_m^{\text{BB}}$ with $\beta_m^{\text{BB}}, \gamma_m^{\text{BB}} \in [-1, 1], \forall m \in \{0, 1, \ldots, 7\}$, and fixed delay $\tau_m^{\text{BB}} = m \times 10$ ns. The ideal frequency response of the nth RF tap is

$$H_n^{\text{RF}}\left(f_k, \theta_n^{\text{RF}}\right) = \alpha_n^{\text{RF}} \cdot e^{-j2\pi f_k \cdot \tau_n^{\text{RF}}} \tag{8}$$

where $\theta_n^{\text{RF}} = (\alpha_n^{\text{RF}}, \tau_n^{\text{RF}})$. Similarly, the ideal frequency response of the mth BB tap is

$$H_m^{\text{BB}}\left(f_k, \theta_m^{\text{BB}}\right) = \left(\beta_m^{\text{BB}} + j\gamma_m^{\text{BB}}\right) \cdot e^{-j2\pi f_k \cdot \tau_m^{\text{BB}}} \tag{9}$$

where $\theta_m^{\text{BB}} = (\beta_m^{\text{BB}}, \gamma_m^{\text{BB}})$. Therefore, the complete set of canceller parameters for a multistage time-domain canceller is

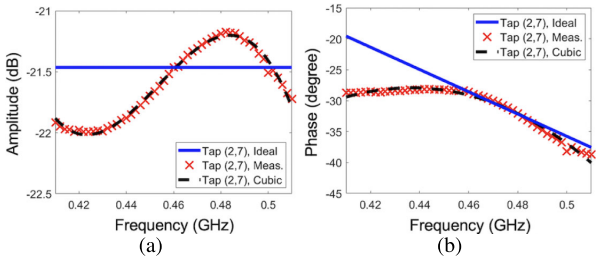


Fig. 8. ***Comparison of the measured frequency response of the 7th RF tap with gain $\alpha_7 = 1$ and delay $\tau_7 = 2 \times 0.25$ ns with both the ideal model and the cubic polynomial regression fit [55]. (a) and (b) Amplitude and phase of the frequency response, respectively.***

given by

$$\left[\left\{\theta_n^{\mathrm{RF}}\right\}_{n=0}^{15}, \left\{\theta_m^{\mathrm{BB}}\right\}_{m=0}^{7}\right] \in \Theta. \tag{10}$$

There are two main challenges associated with optimizing the configuration of the time-domain canceller. First, the admissible configuration space Θ is exponentially large, and is composed of more than 10^{19} possible parameter combinations $(\{\theta_n^{\mathrm{RF}}\}_{n=0}^{15}, \{\theta_m^{\mathrm{BB}}\}_{m=0}^{7})$ that is impossible to enumerate through. Second, the fact that, in practical IC implementations, the actual tap responses may deviate from the ideal analytical models. In Fig. 8, we compare the ideal frequency response of a single RF tap with its actual measurement using a VNA.

To address these challenges, in [55], we proposed and implemented a joint canceller modeling and optimization process that efficiently solves for the configuration parameters. The process begins with an *offline modeling* of the individual taps. Specifically, we use a cubic polynomial regression fit to model the frequency response of each individual tap with unit gain and fixed delay. Let $\hat{H}_n^{\mathrm{RF,cubic}}(f_k, \tau_n^{\mathrm{RF}})$ and $\hat{H}_m^{\mathrm{BB,cubic}}(f_k)$ represent the unit gain cubic models of the nth RF tap with delay τ_n^{RF} and the mth BB tap, respectively. In Fig. 8, we see how closely the unit gain cubic model $\hat{H}_7^{\mathrm{RF,cubic}}(f_k, \tau_7^{\mathrm{RF}})$ matches the corresponding VNA measurements. Compared with storing VNA measurements of every individual taps, storing only the coefficients of the cubic model can reduce the memory space by up to 100× [55].

Leveraging the cubic model, the optimization of the time-domain canceller parameters can be written as

$$\min_{\theta \in \Theta} \sum_{k=1}^{K} \left| H_{\mathrm{SI}}(f_k) - \left[\sum_{n=0}^{15} \alpha_n^{\mathrm{RF}} \cdot \hat{H}_n^{\mathrm{RF,cubic}}\left(f_k, \tau_n^{\mathrm{RF}}\right) + \sum_{m=0}^{7} \left(\beta_m^{\mathrm{BB}} + j\gamma_m^{\mathrm{BB}}\right) \cdot \hat{H}_m^{\mathrm{BB,cubic}}(f_k) \right] \right|^2 \tag{11}$$

subject to the constraints on $\alpha_n^{\mathrm{RF}}, \tau_n^{\mathrm{RF}}, \beta_m^{\mathrm{BB}}$, and γ_m^{BB}. To solve for the configuration parameters, Nagulu et al. [55] use a greedy-like algorithm that iteratively selects the RF tap delays τ_n^{RF} that yields the largest SIC improvement. Notice that, given the set of RF tap delays $\{\tau_0^{\mathrm{RF}}, \tau_1^{\mathrm{RF}}, \ldots, \tau_{15}^{\mathrm{RF}}\}$, the gain optimization procedure can be performed by utilizing the constrained least-square method. For a BW of 40 MHz, the time-domain canceller provides an SIC of 42 dB [55].

D. Configuration of the Frequency-Domain Canceller

As described in Section IV-D, the *integrated* frequency-domain canceller developed in [44] is composed of two parallel 2nd-order BPF taps, each with programmable complex-valued gain $\beta_n^{\mathrm{BPF}} + j\gamma_n^{\mathrm{BPF}}$, center frequency $f_{c,n}^{\mathrm{BPF}}$, and quality factor Q_n^{BPF}. In the RFIC canceller [44], $f_{c,n}^{\mathrm{BPF}}$ and Q_n^{BPF} are adjusted through a reconfigurable BB capacitor and transconductors, respectively. The ideal frequency response of the nth BPF tap is given by

$$H_n^{\mathrm{BPF}}\left(f_k, \theta_n^{\mathrm{BPF}}\right) = \frac{\beta_n^{\mathrm{BPF}} + j\gamma_n^{\mathrm{BPF}}}{1 - jQ_n^{\mathrm{BPF}}\left(f_{c,n}^{\mathrm{BPF}}/f_k - f_k/f_{c,n}^{\mathrm{BPF}}\right)} \tag{12}$$

where $\theta_n^{\mathrm{BPF}} = (\beta_n^{\mathrm{BPF}}, \gamma_n^{\mathrm{BPF}}, f_{c,n}^{\mathrm{BPF}}, Q_n^{\mathrm{BPF}})$. The ideal responses of the 2nd-order BPF taps closely matches the VNA measurements, as shown in [44].

The optimization of the frequency-domain canceller parameters can be written as

$$\min_{\theta \in \Theta} \sum_{k=1}^{K} \left| H_{\mathrm{SI}}(f_k) - \sum_{n=0}^{1} H_n^{\mathrm{BPF}}\left(f_k, \theta_n^{\mathrm{BPF}}\right) \right|^2 \tag{13}$$

subject to the constraints on β_n^{BPF}, γ_n^{BPF}, $f_{c,n}^{\mathrm{BPF}}$, and Q_n^{BPF}. To solve for the configuration parameters, Zhou et al. [44] use a heuristic iterative successive cancellation algorithm. Specifically, the algorithm optimizes the parameters the BPFs, one at a time, e.g., $\theta_0^{\mathrm{BPF}}, \theta_1^{\mathrm{BPF}}, \theta_0^{\mathrm{BPF}}, \ldots$

In [113], we designed and implemented a frequency-domain canceller using discrete components on a PCB. This PCB SI canceller emulates its RFIC counterpart [44]. We developed and evaluated an adaptive configuration algorithm customized for the PCB SI canceller. Our experiments showed that the PCB SI canceller achieves 52 dB across 20-MHz BW. The integration of the PCB SI canceller into the COSMOS testbed is discussed in Section VIII-D.

VIII. CONSIDERATIONS AT THE HIGHER LAYERS

While the benefits of FD wireless are clear at the PHY layer and have been shown to provide up to 2× throughput in a link between two devices [68], [113], benefits to higher layers of the networking protocol stack are less well understood. While the general structure of the networking stack, such as logically separate PHY, MAC, transport layers, and so on, will likely remain the same, the FD operation at the PHY layer has cascading effects up the remainder of the stack as the HD heuristic for typical network controls

algorithms is now broken. In this section, we describe design considerations for higher layer protocols intended for use with FD-capable devices. At the end of this section, we describe an open-access FD-capable testbed, which has been integrated into the COSMOS testbed [66], [67], [153], consisting of several FD nodes and thus designed for experimentation at the higher layers.

A. FD Medium Access Control

In principle, the FD operation at the PHY layer allows more than one radio to transmit at a given time within a network operating on a certain carrier frequency. Under certain conditions, this leads to interference conditions not typically experienced in networks with only HD radios.

Consider a simple access network with a single access point (AP) and two users, U_1 and U_2. Should the AP be FD-capable, U_1 may transmit to the AP at the same time as the AP transmits to U_2. At a simple level, this presents a 2× rate gain and reduced latency over an HD network where the transmissions would be separated by time. However, this scenario exhibits interuser interference (IUI) between U_1 and U_2, which may limit the feasibility of such a transmission scheme if too severe. On the scale of a network of users, IUI arising from the FD operation itself can degrade SINR to varying degrees, affecting the achievable rate gains [154], [155], [156], [157]. Therefore, to best make use of FD, the development of a specialized FD MAC is required, which takes into account both the typical interference scenarios in HD schemes, such as IUI across two different BSs, along with new scenarios brought about by FD capability.

The use of an FD MAC has been shown to improve throughput and spectral efficiency for wireless nodes within a network where FD-capable nodes are present [1], [113], [152], [154], [155], [156], [157], [158], [159], [160], [161], [162], [163], [164], [165], [166], [167], [168], [169], [170]. FD MACs have been studied in networks with all HD users [168], [169] or with heterogeneous HD and FD users [113], [160]. Janus [156] uses interference information from probe packets to achieve up to 2.5× rate gain in a four-node CSMA/CA network, while work [154] highlights how rate gains approach 1× as the interference range approaches the transmission range. AFD-MAC [166], with an 802.11-like approach, can produce rate gains as high as 2× as well as halving of queuing delays in networks where only the AP is FD. By considering the buffer state information of each node, SFLS [167] is able to achieve improvement over prior FD MACs appropriate for 802.11 wireless local area network (WLAN) settings. Finally, Kim et al. [170] report an FD MAC with improved throughput benefit with an increasing number of nodes. Overall, prior work has shown that rate gains typically up to 2× are achievable with an FD MAC that takes into account the interference state of all devices.

In addition to CSMA/CA networks or the 802.11 WLAN, recent work has explored the use of FD in mmWave cellular networks [1], [171], [172], [173], which are predominantly schedule-based rather than contention-based, such as CSMA/CA or the 802.11 WLAN. We focus in this section on the phased-array and relay applications. The high path loss experienced by an mmWave signal can severely inhibit link budgets [174], [175], [176], [177], [178], [179]. To overcome this challenge, highly directional phased-array antennas have become ubiquitous in mmWave networks. Furthermore, new network elements, such as relays and integrated access and backhaul (IAB) nodes, are increasing in use. As described in Section VI-A, phased-array antennas provide another opportunity for SIC through beamforming [143], [171] to improve isolation between TX and RX elements. At the network level, this translates into the need for efficient codebooks that produce SI-canceling beams, and if appropriately selected, these codebooks can produce close-to-ideal FD rate gains [173].

New network elements, such as relays and IAB nodes, are another place where FD has the potential to provide benefits. Relays can extend the effective coverage of a BS, but without the ability to operate in FD mode, the relay must receive the entire signal before being able to forward it. With an FD relay, the latency of a relayed transmission can be within microseconds of the latency for a direct transmission [180]. Furthermore, FD relays can themselves enable FD communication between devices that are outside of each other's direct communication range [181]. IAB nodes, which may be used to supplement costly fiber deployments while providing similar throughput and latency [182], [183], can also benefit from FD in a similar way to the FD relay. By appropriate positioning of array antennas on an IAB, SI can suppressed to levels requiring only SIC across the antenna (Section III) and digital (Section V) domains [172]. An overview of FD's role in 6G cellular networks is presented in [1].

B. Transport and Application Layers

The traffic condition at each node directly affects the usefulness of FD in the network [162]. TDD operation is popular in cellular systems due to its flexibility in resource allocation, an important factor for modern wireless communication where DL traffic load can be 6–9× the UL traffic load [184]. This highly asymmetric character is driven in large part through the preponderance of video streaming [185], which may reach up to 80% of overall cellular network traffic by 2028 [184]. This asymmetric traffic demand can easily be supported in the TDD mode by allocating time slots accordingly, for example, in a 6–9:1 DL/UL pattern at the expense of degraded UL latency. FD presents an opportunity for improvement of this degraded UL latency through the support of simultaneous UL and DL transmissions within a TDD scheme [113]. In the general case, improved UL latency can have a significant improvement on the round-trip time (RTT), which is a critical aspect of the TCP or QUIC protocol handshake. In the case of video streaming, reduced RTT can reduce the time taken

for a video to begin playing, which has been identified as a key quality of experience (QoE) indicator [186].

While traffic asymmetry is common, there are emergent applications with much greater parity between UL and DL traffic volumes, such as video conferencing and virtual reality (VR)/augmented reality (AR). In video conferencing, it is typical for participants to be both sending and receiving video at moderate data rates [187], meaning that the throughput benefit of FD can be better realized. Modern VR/AR head-mounted displays (HMDs) typically have high-resolution screens operating at high frame rates [188], to provide a convincing user experience and reduce motion sickness [189]. Simultaneously, a large volume of telemetry data will be generated by the HMD and other controllers, which must be transmitted to the AP. As a result, VR/AR systems will typically have high-BW traffic in both UL and DL, positioning FD wireless as an enabler for tetherless VR/AR.

C. Considerations for the Use of Real FD Radios

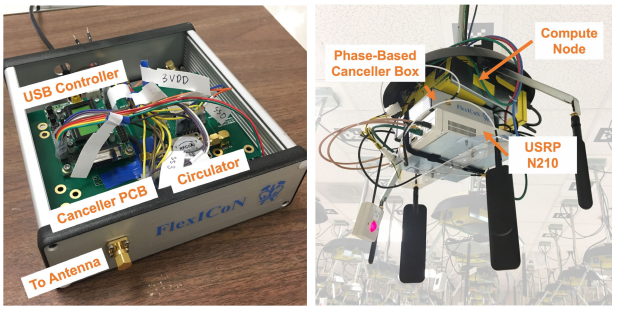
Much of the prior work on FD MAC protocols relies heavily on simulations and mathematical analysis to demonstrate the effectiveness in terms of throughput gain, fairness, and spectral efficiency. Often, attention is given to realistic impairments, such as overheads [165], imperfect SIC [190], and the presence of non-FD users in the network [160]. However, this does not necessarily cover all possible impairments that may be experienced by an FD radio in practice.

As described in Sections V and VII, the ability of an FD radio to achieve the required amount of SIC requires the generation of optimal system configurations across the digital and analog/RF domains. While this configuration occurs at the node level rather than across the entire network, it will generally add overhead in the form of computational delays or the need to perform channel sensing. A changing physical environment will demand a reconfiguration to ensure sufficient SIC at all times. As such, it is likely that any FD MAC deployed in a real network would implement reconfiguration steps as part of the protocol.

As there are comparatively fewer evaluations using real FD radio systems in the literature [68], [113], [155], [156], the impact of this overhead on the overall rate gains is not well understood. To aid the community's efforts in this direction, a set of FD radios have been integrated in the NSF PAWR COSMOS testbed in New York, which is openly available to researchers. We describe this FD testbed, as well as its precursor in the ORBIT testbed, in the following.

D. COSMOS and ORBIT Testbed Integrations

In order to experimentally evaluate benefits of FD wireless at the higher layers of the networking protocol stack, we integrated four FD radios [68] in the indoors Sandbox 2 of the open-access COSMOS testbed [66], [67],



(a) (b)

Fig. 9. *ORBIT FD testbed. (a) Canceller box, showing the various components that enable the box to serve as an FD transceiver, as in Fig. 1, for a USRP N210 SDR. (b) One canceller box integrated in the testbed, showing the USRP N210 and yellow ORBIT compute node.*

[153]. These FD radios are equipped with improved versions of the FDE-based SI cancellers [44], [113] described in Sections IV-D and VII. Altogether, the integrated FD radios comprise the entire system described in Fig. 1. The COSMOS FD testbed was preceded by a similar, albeit smaller scale, integration of the phased-based SI canceller described in Section IV-B in the ORBIT testbed [61], [191], [192].

The ORBIT and COSMOS FD testbeds are remotely accessible experimentation resources available to the broader research community, alleviating the need to develop or purchase FD-capable hardware and/or software-defined radios (SDRs) (see [193] for a hands-on tutorial). The ORBIT FD testbed integration is shown in Fig. 9, and the COSMOS FD integration is shown in Fig. 10. Both the ORBIT and COSMOS FD testbeds are located within indoor laboratories, with environmental variation typically limited to the movement of people within the laboratory; temperature and interference levels are generally stable. This presents an idealized environment not requiring the need for the adaptive configuration methods in Section VII. For the remainder of this section, we will focus on the COSMOS integration. More details on the ORBIT FD testbed may be found in [61] and [68].

1) Design of the COSMOS FD Testbed: The COSMOS FD testbed consists of several major components, as detailed in this section.

a) Canceller box: The COSMOS FD testbed uses an improved version of the PCB SI canceller evaluated in [113]. The PCB SI canceller emulates the FDE approach from Section IV-D, which was originally implemented as an RFIC [44]. The PCB construction improves robustness when integrated at the system level as well as provides a reduced NF and dc power consumption.

The canceller PCB is connected to a circulator and antenna tuner to support a single-antenna interface, and a USB-to-SPI controller is used for hardware control. These four components are included in a "canceller box" depicted in Fig. 10(a), and four such boxes are mounted in the COSMOS FD testbed, as shown in Fig. 10(b). The PCB

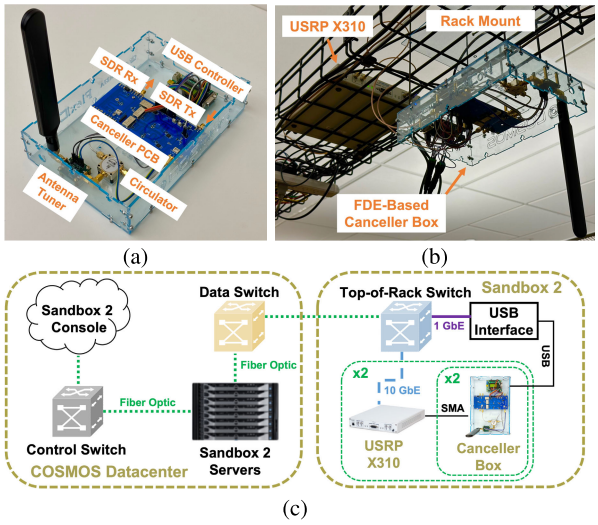


Fig. 10. ***COSMOS FD testbed. (a) Canceller box, showing various components that enable the box to serve as an FD transceiver, as in Fig. 1, for a USRP X310 SDR. (b) One canceller box integrated in the testbed, showing the USRP X310 SDR and custom rack mount hardware. (c) Block diagram showing the architecture of the COSMOS FD testbed.***

canceller is configured manually via the experimentation software; the static laboratory environment housing the FD testbed allows for stable canceller configuration. This also permits experimenters to generate various RF SIC profiles.

b) USRP X310 SDR: Each canceller box is used as the FD transceiver for the SBX-120 daughterboard within a USRP X310 SDR.

c) Experimentation software: The COSMOS FD testbed utilizes GNU Radio for control of the FD hardware. The custom C++ software is contained within an out-of-tree (OOT) module for GNU Radio [194], supporting real-time FD experimentation.

2) Experimentation: Each COSMOS FD radio is capable of 85 dB of overall SIC. This enables the COSMOS FD radios to cancel their SI to the noise floor with a transmit power close to 0 dBm. Due to the proximity of the FD radios within the laboratory environment, this is sufficient for operation with SNRs appropriate for experimentation with 802.11a-like data packets [195]. The COSMOS FD testbed has been used to evaluate the performance of FD radios in a slotted ALOHA-based network, demonstrating achievable network throughput gains that align closely to theoretical results [68].

IX. APPLICATIONS AND FUTURE RESEARCH DIRECTIONS

The benefits that FD can bring to the higher layers of the network stack as described in Section VIII can enable a range of future applications. Moreover, FD has the potential to support applications outside the domain of wireless networking. In this section, we describe a nonexhaustive set of future applications and research directions for FD wireless.

A. FD Internet of Things Gateways

Among wireless communication applications, the Internet of Things (IoT) is a likely candidate for FD deployment [196], driven by low power requirements [197]. IoT gateways form the backbone of the IoT infrastructure by bridging various IoT devices (sensors, cameras, actuators, and so on) or connecting them to the Internet, usually through a wireless network. IoT gateways suffer from packet collision problems due to the high volume of devices using low data rate links (50–800 kb/s in IEEE802.15.4g), hindering scalability of end nodes to a few hundred per gateway. FD MAC protocols as described in Section VIII-A could enable better coordination for end nodes. For example, an FD IoT gateway could simultaneously send an ACK packet (for correctly received packets or busy signal to others) in DL while receiving a UL signal from a different node [164], [198].

B. FD in Next-Generation Wireless

1) mmWave Backhaul and Relaying: The application-level demands as outlined in Section VIII-B will bring massive capacity pressure on backhaul, a somewhat less addressed bottleneck of the overall next-generation (xG) network. In addition to the general benefits of FD for relays and IAB nodes outlined in Section VIII-A, FD can enable the aggregation of E-band frequency bands that are typically used for backhauling over shorter distances between densely deployed BSs [199]. Simultaneous UL and DL at the relay or IAB is essential to reduce latency in such networks [180] and may be overcome through the use of FDD, for example, between the 71–76-GHz and 81–86-GHz bands, using waveguide duplexers. FD would enable such operation in a single-frequency band, enabling aggregation of both bands for increased capacity.

2) FD in Nonterrestrial Networks: 6G networks envisage the integration of ground and air networks using drones, high-altitude platforms (HAPs), and nanosatellites, to achieve worldwide connectivity [1], [200], [201]. Unlike geostationary satellites, which orbit at 35 800 km, these technologies operate at lower altitudes. Drones fly a few hundred meters above the ground, HAPs in the stratosphere at 20 km, and low-Earth-orbit satellites at 200–2000 km [202]. Lower orbits reduce propagation losses, thus reducing the TX and SI power levels. This opens new possibilities for FD operation in aerial networks due to the reduction in the SI requirements and recent advancements in wideband SIC capabilities. FD can benefit IoT services in remote areas by reducing latency and enhancing spectral efficiency and security. Recent studies have explored the feasibility of employing FD communication in unmanned aerial vehicle (UAV) and satellite networks. A system-level link budget analysis was performed in [202] to demonstrate the feasibility of FD in satellite communications. For instance, Grayver et al. [203] proposed to achieve a 130-dB SIC at 915-MHz targeting FD operation in low-Earth-orbit satellite links. Hua et al.

[204] study the scenario where a small cell UAV acted as an FD BS to serve the ground users. In [205], reliability and outage performance of the satellite FD systems have been evaluated. In addition to achieving SIC, implementing FD communication in aerial terminals faces challenges, especially regarding handover and interference control [1]. For example, drones' flight paths can create varying interference patterns between air-to-air or air-to-ground signals and hard-to-predict shadowing conditions. Thereby, integrating aerial or space segments with terrestrial networks requires careful planning. Finally, limited onboard energy could also restrict FD adoption unless lightweight and cost-effective energy storage technologies are developed, making the development of integrated SI cancellers and antenna interfaces of paramount importance.

C. Automotive Systems

1) Automotive Radar: TX-to-RX SI is referred to as spillover in frequency-modulated continuous-wave (FMCW) automotive radars and is one of the remaining issues that needs to be addressed. Spillover can result from limited isolation in the antenna interface and from strong reflections arising from very close objects such as the vehicle's bumper or fascia. The spillover at the RX input can be much stronger than the reflected powers by distant objects that the radar aims to detect [206] and must be suppressed to prevent saturation of the receiver. SI suppression techniques developed in the context of mmWave FD are also applicable to solving the spillover problem in automotive radars. A fully integrated low-loss circulator with high isolation would replace lossy passive shared antenna interfaces such as hybrids (which have a theoretical loss of 3 dB, typically 4 dB), which are widely used at monostatic radars to share a single antenna between the TX and RX. Alternatively, polarization domain is another DoF, which could be exploited to enable loss-free duplexers for monostatic radars [207].

2) Automotive Ethernet: Automotive electronics has become increasingly complex over the last decade as there is a need in today's vehicles to support more features to enhance safety, efficiency, driving, and in-cabin experiences. As a result, in-vehicle networking is evolving at a rapid pace to support higher throughput at lower cost with less number of cables. Automotive Ethernet (100BASE-T1) is emerging as a preferred choice of physical layer standard for in-vehicle networking. Unlike traditional Ethernet, which relies on dual-simplex operation (separate TX and RX paths), 100BASE-T1 operates in FD and uses a single twisted pair for simultaneous TX and RX operation (100 Mb/s in each direction); offering reduced cabling weight, high data rates with low manufacturing cost [208]. Currently, 100BASE-T1 PHYs enable FD operation through transformer hybrids, which are bulky and high cost. Broadband fully integrated circulators developed in the context of FD wireless (Section III-B2) could replace the bulky hybrids in the 100BASE-T1 links. In addition, analog/BB and digital SIC techniques developed for FD wireless (Section V) could be adopted to design wideband echo cancelers for future automotive Ethernet links (e.g., in 1000BASE-T1) to support higher data rates.

D. Interference Cancellation for Multiprotocol TX Coexistence

With an increasingly complex communication and IoT landscape, there is an immense demand for radios to operate simultaneously across multiple protocols. In such situations, the TX signal of one radio can couple to the high-output-power TX of another radio during concurrent transmission, causing TX-to-TX interference. This results in two high-power TX signals mixing due to PA nonlinearity and generating undesirable IM3 products that violate the spectral masks. For example, a 2.4-GHz WLAN TX signal can mix with a 2.4-GHz NB Bluetooth signal to produce undesired IMD components [209]. Interference cancellation techniques that can alleviate the TX-coexistence challenge have not been widely addressed in the literature. Early efforts addressing this issue were proposed in [209] to cancel a 2.4-GHz narrowband interferer (e.g., Bluetooth) appearing at a 2.4-GHz wideband TX (e.g., WLAN) using single-tap phase-domain canceler. Exploring multitap time-delay and/or frequency-domain SI cancelers for addressing the TX-to-TX interference cancellation of wideband signals will be an interesting research direction.

E. Sensing Using RF Signals

Environmental sensing using RF wireless signals is an area of active research [210], [211], [212]. Regardless of RF frequency or specific sensing scenario, separate TX and RX are typically required, as the TX will operate in the HD mode. By employing SIC techniques, the need for a separate RX can be obviated, as the TX will be able to receive the signal as modified by the physical environment. Even in cases where a separate RX is used, SIC can improve the SINR on the RX. As an example, SIC techniques have been explored for use in magnetic resonance imaging (MRI) machines [213], where the excitation of atomic nuclei and subsequent acquisition of the emitted RF signal must be done in a TDD manner. With the inclusion of SIC techniques, concurrent excitation and acquisition is possible, reducing energy costs and the time spent by a patient in the MRI machine.

X. CONCLUSION

In conclusion, this review article has provided a comprehensive overview of circuit approaches for FD wireless systems. We discussed various aspects of hardware design and implementation, focusing on SIC techniques across multiple domains. We first established a system-level understanding of FD wireless systems using link budget calculations. Prior works on antenna interfaces, such as dual antenna schemes, passive hybrids, and integrated circulators, were reviewed. We discussed two FOMs for antenna interfaces for fair comparison and evaluation.

Following that, we discussed the progress in RF and analog-BB SIC circuits, through the review of phase-based cancellers, time-domain cancellers, and frequency-domain cancellers. We also presented FOMs to assess the efficiency of SI cancelers. Later, we reviewed digital SIC techniques, including DSP- and learning-based methods. We then highlighted the opportunities presented by FD in multiantenna systems. We also covered the system-level efforts for integrating FD radios in large-scale testbeds through the Columbia FlexICoN and NSF COSMOS projects. Finally, we discussed future opportunities and applications of the FD systems.

Looking ahead, a crucial area of research will involve enhancing the antenna interface and canceler FOMs through reductions in insertion losses and dc power consumption, as well as improvements in linearity. Moreover, it will be essential to explore the design and implementation of integrated RF and/or analog-BB cancellers with a greater number of taps and/or DoFs. These cancellers will possess the capability to achieve enhanced SIC across a wider signal BW, ultimately improving the SIC-FBW product. With the increased complexity of SI cancelers, another important research direction involves developing more efficient ML-based adaptive algorithms for tuning the RF and BB cancelers with a large number of taps. Due to the extensive search space involved, these algorithms are of paramount importance and present an intriguing avenue for exploration. Furthermore, advancing both single-antenna and multiantenna FD systems requires the co-design and joint optimization of cancellers across different domains, such as between antenna, RF, BB, and digital. This cross-domain optimization is necessary to unlock the full potential of FD systems and represents a key area for further investigation. System-level integration of FD radios, including those available to the research community as in the case of the COSMOS FD testbed, will be an enabler of such research. This includes further research at the higher layers of the networking protocol stack, addressing the coexistence and integration challenges of FD radios with existing wireless systems, including interference management and spectrum sharing techniques. ■

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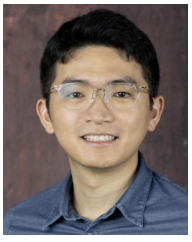

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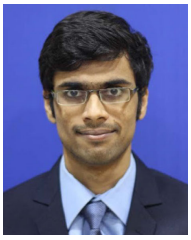

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