Investigation of Reflected Wave Phenomenon in SiC-based Two-Level Split-Phase Inverter-Fed Motor Drives

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***Abstract*—Fast switching speed of Silicon Carbide (SiC) exacerbates Reflected Wave Phenomenon (RWP) in two-level (2L) Voltage Source Inverter (VSI)-based motor drives, causing motor side overvoltage and drive side overcurrent. The 2L split-phase (2L-SP) topology shows prospects of alleviating RWP due to its lower output $\mathrm{d}v/\mathrm{d}t$ facilitated by split-inductors which also serve as an output reactor. This article explores RWP in a 2L-SP-based motor drive and compares it with the 2L with an output reactor, denoted as 2L-LF. For the study, a 2L, 2L-LF and 2L-SP configurable 18 kVA SiC-based prototype is developed and interfaced to an emulated motor load through a bundled shielded cable. At first, simplified lumped Differential Mode (DM) equivalent circuits are derived for modeling RWP transients in 2L-LF and 2L-SP drives. Subsequently, RWP is investigated through Double Pulse Tests (DPT) for various cable lengths, reactor (2L-LF), and split inductor (2L-SP) values. Results show that 2L-SP exhibits lower RWP for longer cables, achieving up to 68 % and 73 % reduction in overvoltage and overcurrent amplitudes for an 8 m cable. An anomalous rising overvoltage pattern for short cables is observed for both drive configurations and analyzed using proposed DM equivalent circuits. Further, from a switching performance standpoint, split-inductors in 2L-SP decouple load and complementary cell's parasitics from the device during switching, achieving 17 % lower switching loss than 2L-LF. Following the DPTs, continuous three-phase tests are performed for 8 m cable for both drive configurations. The 2L-SP drive achieves up to 60 % and 74 % reduction in overvoltage and overcurrent amplitudes than 2L-LF. Overall, 2L-SP outperforms 2L-LF in mitigating RWP in SiC-based 2L VSI motor drives.**

***Index Terms*—Auxiliary L filter, drive-side overcurrent, $\mathrm{d}v/\mathrm{d}t$ profiling, motor-side overvoltage, reflected wave phenomenon (RWP), silicon carbide (SiC), split-phase topology (2L-SP).**

I. Introduction

Advent of Wide Band Gap (WBG) power semiconductors such as SiC has enabled the development of efficient and power-dense 2L VSI-based motor drives [1], [2]. Compared with Silicon (Si), SiC MOSFETs are capable of operating at higher operating temperature and voltage levels and faster switching speeds. Among these benefits, the fast-switching capability ($\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$) of SiC MOSFETs plays a pivotal role in lowering the device switching loss and shrinking size of passive components by permitting high switching frequency [3], [4]. As a result, adopting SiC MOSFETs in 2L motor drives improves the system efficiency and control dynamic performance [5].

Although SiC MOSFETs are promising for enhancing performance and efficiency of next generation 2L motor drives, the fast-switching ($\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$) capability of SiC MOSFETs exacerbates Reflected Wave Phenomenon (RWP) in cable-connected 2L motor drive systems [6], [7]. The RWP arises due to drive-cable and cable-motor impedance mismatch, leading to overcurrent and overvoltage oscillations on the drive side and motor side, respectively. Further, the extent of RWP is related to the $\mathrm{d}v/\mathrm{d}t$ of drive output voltage, cable length, drive-cable and cable-motor impedance mismatch, system damping, and pulse application timing [8]–[10].

From the drive performance perspective, drive-side overcurrent due to RWP influences the switching transient of the device. Due to the lower output capacitance of the SiC devices, their switching transient is susceptible to the parasitics of the circuit. For instance, for a cable-connected motor load, the additional underlying parasitic capacitance of cable and motor alter the switching transient, increasing switching loss [11]. From the cable and motor perspective, motor-side overvoltage due to RWP increases voltage stress on the cable and motor winding insulation, leading to premature insulation failure due to partial discharge [12], [13].

RWP mitigation approaches can be classified into active or passive solutions. Passive solutions rely on using passive filters, based on combination of R, L and C, on the drive or motor side. These filters can be sub-classified into $\mathrm{d}v/\mathrm{d}t$ and impedance matching filters [14]. The commonly used $\mathrm{d}v/\mathrm{d}t$ filters include auxiliary reactor L filter [15], [16], RLC filter [17], RC filter [18], $L||RC$ [19]. Similarly, impedance matching filters lower the RWP by including $L||R$ filter (drive side) [14] and RL-plus-C filter (motor side) [20], [21]. Among various filter types, the L and $L||R$ filters at the drive side are the preferred option in the industry due to their simplicity [14], [15].

Active solutions involve device $\mathrm{d}v/\mathrm{d}t$ profiling [22], [23] or generating mid-level dwell time during pulse rising and falling [24], [25]. For $\mathrm{d}v/\mathrm{d}t$ profiling, the most common approach is to use an Active Gate Driver (AGD), which works by controlling the gate source voltage profile to control the $\mathrm{d}v/\mathrm{d}t$ of the device [22]. However, this is achieved at the expense of increased control complexity and switching loss, especially in a hard-switching topology. Soft-switching inverter topologies with $\mathrm{d}v/\mathrm{d}t$ profiling overcome the the high switching loss limitation of AGD. A soft-switching approach based on Auxiliary Resonant Commutated Pole Inverter (ARCPI) in proposed in [23], which mitigates the RWP by setting the rising and falling time of the switching transition equal to

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antiresonance period of the cable and motor. Although the ARCPI-based approach is shown to be effective, the auxiliary switches, passive components and control complexity offsets the benefits of this technique.

Delving into the mid-level dwell time approach, the idea is to reshape the drive output pulse voltage transition by splitting it into two identical voltage steps with an intermediate mid-level [24]–[26]. The mid-level time duration, known as dwell time, is twice the antiresonance period of the cable and motor. This approach results in the generation of two out-of-phase RWP transients, which cancel each other, diminishing overvoltage at motor terminals.

The dwell time approaches employ either extra switching devices, passive components, or sophisticated control schemes. In [26], a T-type-based three-phase inverter structure is proposed to generate dwell time, requiring six additional IGBTs. A quasi-three-level (Q3L) modulation strategy is proposed in [24] to suppress RWP in a single-phase motor drive fed with a full bridge. The dwell time is introduced through separate carrier waveforms for each half-bridge, displaced with a time duration equal to the dwell time. Further, the authors in [25] propose a DM-coupled inductor between the paralleled half-bridges and the phase output to synthesize mid-level dwell time for three-phase motor drives. According to the test results, the proposed converter topology provides partial to full RWP mitigation, depending on the dwell time matching extent.

Although the dwell time approaches are effective, their performance is contingent upon the accurate dwell time value, which depends on cable and motor characteristics. In practice, dwell time can be estimated from the first antiresonance in the DM impedance of the cable and motor [25]. However, obtaining an accurate DM impedance requires precise compensation of measurement errors due to probes and extra leads used for making connections during measurement. Further, variations in cable and motor insulation characteristics over time also change the dwell time, requiring periodic updates of the dwell time value in the drive control. Besides this, the slew-rate of the drive output voltage pulse, which varies with device and circuit parasitics and load current, also needs to be compensated in the PWM signals for gate drives.

Recently, a SiC-based split-phase (2L-SP) topology has been proposed in the literature, offering several advantages over the standard 2L topology [27], [28]. The 2L-SP topology comprises P- and N-cells, with split inductors L_s connected between the mid-points of these cells. The phase leg of 2L-SP can be derived by splitting the 2L phase leg, provided that a SiC Schottky Barrier Diode (SBD) is placed across the SiC MOSFET. Fig. 1(a)-(c) illustrates the transformation from the SiC-based 2L to 2L-SP phase leg.

The intrinsic SiC MOSFET body diode suffers from a relatively high forward voltage drop and significant reverse recovery losses, which increase with temperature, consequently raising the switching loss at high temperatures. In contrast, the SiC SBD features zero reverse recovery with a lower forward voltage drop [29]. A detailed switching performance comparison of the SiC MOSFET with and without the anti-parallel SiC SBD is provided in [30]. According to the results, the SiC MOSFET with SiC SBD offers lower total switching loss at high current levels throughout the working temperature range (25 ° to 175 ° C). Therefore, incorporating anti-parallel SiC SBD in 2L is effective for improving drive efficiency, especially at high power levels. Furthermore, in the context of 2L-SP, assuming an anti-parallel SiC SBD is used, the number of semiconductor devices in both 2L-SP and 2L is equal.

From the switching performance perspective, split inductors in 2L-SP decouple the switching device from its complementary cell devices' parasitic capacitance. For instance, for P-cell in Fig 1. L_s decouples S_P from parasitic capacitances of S_N (C_{OSS}) and D_N (C_J). This decoupling lowers the total switching loss and increases cross-talk immunity. A device loss analysis for a 2L-SP three-phase inverter with SPWM is conducted in [27]. The analysis explores device loss variations with key metrics such as SPWM modulation index (m), switching frequency (f), power factor angle (ϕ), and conduction current amplitude (I_{cm}). Results indicate that device loss variations for 2L-SP are always upper-bounded by those of the 2L inverter across these metrics. Additionally, experimental efficiency comparisons show that 2L-SP outperforms 2L, with increased efficiency at higher frequencies, making 2L-SP particularly advantageous for SiC devices.

Furthermore, split inductors lower the $\mathrm{d}v/\mathrm{d}t$ at mid-point/AC output, as discussed in [31]. This lower output $\mathrm{d}v/\mathrm{d}t$ can potentially mitigate the RWP. Besides this, the presence of L_s at output also has the potential to serve as an auxiliary L filter. L filter is the simplest passive filter employed for the standard 2L inverter-based drives (2L-LF) in the industry [6]. The filter shifts the reflected wave ringing frequency f_{RW} to a lower value, thereby lowering the slew rate of motor side

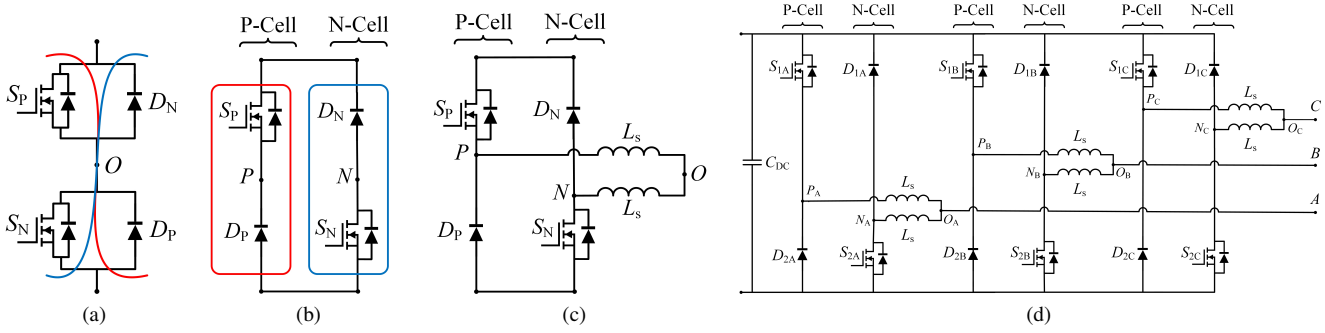

Fig. 1. Derivation of SiC 2L-SP motor drive from 2L. (a) Dissection of 2L phase leg into P and N cells. (b) P and N cells separated. (c) Mid-points of P and N cell P and N connected through L_s to the output node O. (d) Three-phase 2L-SP motor drive.

overvoltage and current oscillation on the drive side to reduce switching loss [15]. However, the performance of L filter in mitigating RWP is inferior as a large value of inductance is required to reduce overvoltage and overcurrent amplitude significantly, increasing system cost and weight [16].

In contrast, 2L-SP shows the prospect of lowering the switching loss and slew rate of motor side overvoltage due to split inductors (acting as L filter) and overvoltage amplitude due to its lower output $\mathrm{d}v/\mathrm{d}t$. This aspect of 2L-SP in motor drive applications with a cable-connected motor is yet to be analyzed. Moreover, with an assumption that the value of L filter is equal to $0.5L_\mathrm{s}$ (parallel combination of L_s), the net filter inductance per phase for both 2L-SP and 2L-LF is equal. This equivalence establishes a fair case for benchmarking the performance of 2L-SP against 2L-LF in lowering RWP.

This article investigates the RWP in a 2L-SP motor drive and compares it with a 2L drive with L filter. A 2L, 2L-LF and 2L-SP reconfigurable 18 kVA SiC-based prototype is developed and connected to an emulated motor load using a bundled shielded VFD cable. The contribution of the article can be summarized as

1) A comprehensive investigation of the RWP, namely drive-side overcurrent and motor-side overvoltage, in a 2L-SP-based motor drive through double pulse and continuous testing for different cable lengths and split inductor values.
2) Performance comparison of 2L-SP and 2L-LF in suppressing RWP, using the same net DM inductance for the split inductor (2L-SP) and the reactor (2L-LF) to ensure a fair comparison.
3) A simplified DM lumped circuit model, incorporating the drive's output $\mathrm{d}v/\mathrm{d}t$, for modeling RWP transients in 2L-SP and its experimental validation. From a design perspective, the proposed model and derived expressions provide a more straightforward means of analyzing the overvoltage and overcurrent transient trends beforehand.
4) Discovery of a potential increasing trend of peak overvoltage with the split inductor/reactor value for short cable lengths in both configurations, along with validation using the proposed simplified DM circuit models.
5) Investigation of RWP in 2L-SP-based integrated motor drives, showing no increasing trend of peak overvoltage with split inductance as observed for short cables.
6) Evaluation of the switching performance of 2L-SP and comparison with 2L and 2L-LF, showing that 2L-SP achieves lower switching loss.
7) Development of criteria for sizing split inductors for 2L-SP-based motor drives.

The article is organized as follows. Section II briefly overviews the lower output $\mathrm{d}v/\mathrm{d}t$ benefit of 2L-SP. Section III delves into switching transition equivalent circuit modeling for RWP to develop simplified lumped DM circuit models for estimating peak overvoltage and overcurrent in 2L-LF and 2L-SP motor drives. Section IV presents the results of Double Pulse Tests (DPT) conducted for RWP investigation for different cable lengths and reactor/split inductor values for 2L-LF and 2L-SP. The remarks and comparison of key performance metrics such as motor side overvoltage and drive side overcurrent are presented. Section V analyzes the increasing overvoltage trend with short cables, observed in Section IV, and extends the DPT-based RWP investigation to a 2L-SP-based integrated motor drive. Further, the device's switching transient ($\mathrm{d}v/\mathrm{d}t$) and switching loss for 2L-LF and 2L-SP are analyzed and discussed in Section VI. Following the investigation through DPT, the RWP study is further extended in Section VII, where continuous test results with SPWM for both configurations are presented and compared. In Section VIII, guidelines for sizing split inductors for 2L-SP-based motor drives and a comparison of 2L-SP with 2L-LF and similar existing drive structures with active RWP mitigation approaches are provided. Lastly, Section IX concludes the article.

II. Output $\mathrm{d}v/\mathrm{d}t$ in 2L-SP

Split inductors in 2L-SP lower the output $\mathrm{d}v/\mathrm{d}t$ during the switching transition [31]–[33]. For any modulation scheme, the switching transition happens in one phase leg at a time. The other phases are clamped to DC link or power ground. For instance, for phase A in Fig. 1 (c), the two switching transitions are $S_{1\mathrm{A}}$ OFF $\rightarrow$ ON and $S_{2\mathrm{A}}$ ON $\rightarrow$ OFF or $S_{1\mathrm{A}}$ ON $\rightarrow$ OFF and $S_{2\mathrm{A}}$ OFF $\rightarrow$ ON. During each of these switching transitions, a complex resonance circuit is formed, which is excited by the switching $\mathrm{d}v/\mathrm{d}t$ of the device undergoing switching. The resonance circuit comprises split inductors of the switching phase leg, complementary cell's MOSFET and diode output capacitances C_{OSS} and C_J, and load and split inductors of other phases [32], [33].

Fig. 2 shows the equivalent switching transition circuit for the $S_{1\mathrm{A}}$ ON $\rightarrow$ OFF and $S_{2\mathrm{A}}$ OFF $\rightarrow$ ON transition for phase A. For coherence, the same switching transition is considered for modeling RWP transients in the following sections. The branch connected to node O_A comprising load and split inductors of other phases is omitted with an assumption that there are no load parasitics and the branch impedance Z is much higher than the parallel branch containing L_s, C_{OSS} and C_J [32]. The voltage source $v_{\mathrm{DS}}(t)$ represents the falling $\mathrm{d}v/\mathrm{d}t$ of $S_{2\mathrm{A}}$, which excites the series resonance circuit. As a result, the voltage of nodes O_A and P_A resonate with the angular frequency $\omega_\mathrm{s} = 1/\sqrt{(2L_\mathrm{s}(C_{\mathrm{OSS}} + C_\mathrm{J}))}$. When the voltage of nodes O_A and P_A reaches zero, forced by $v_{\mathrm{DS}}(t)$ after a time duration of T_Z since the start of the switching transient, the resonance is suppressed as the voltage across C_{OSS} and C_J is clamped. As a result, the output $\mathrm{d}v/\mathrm{d}t$ is lower and has a sinusoidal profile.

The equivalent circuit in Fig. 2(a) can be solved to obtain closed-form time domain expressions for $v_{\mathrm{OA}}(t)$ and $v_{\mathrm{PA}}(t)$, as performed in [32]. However, in [32], a step voltage source (infinite $\mathrm{d}v/\mathrm{d}t$) is used to solve the equivalent circuit, which can over estimate $v_{\mathrm{OA}}(t)$ and $v_{\mathrm{PA}}(t)$. To address this and improve accuracy, the step source can be replaced with a ramp edge with a fall time T_F to represent the $\mathrm{d}v/\mathrm{d}t$ of $S_{2\mathrm{A}}$ in $v_{\mathrm{DS}}(t)$ (1). This approach is adopted in this article in the following sections for modeling RWP in 2L-LF and 2L-SP, respectively.

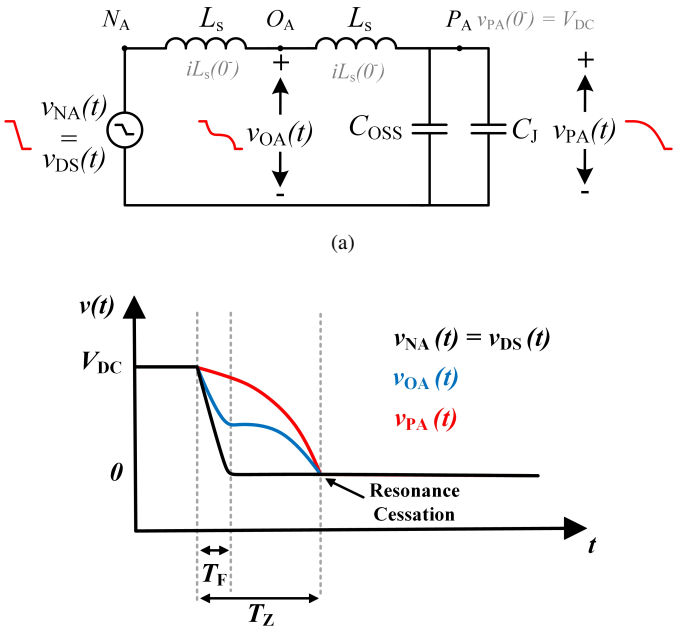

Fig. 2. Phase A S_{1A} ON $\rightarrow$ OFF and S_{2A} OFF $\rightarrow$ ON switching transition. (a) Equivalent circuit. (b) Waveforms.

$$v_{DS}(t) = V_{DC}\left(u(t) + \frac{(r(t-T_F) - r(t))}{T_F}\right) \tag{1}$$

III. DM Equivalent Circuit Modeling for RWP Transients

The RWP is incepted for each switching transition in each phase leg of the motor drive. For instance, Fig. 3 depicts the schematic for 2L-LF and 2L-SP cable-connected motor drive for the phase A bottom switch S_{2A} OFF $\rightarrow$ ON switching transition with phase B and C clamped to DC link (V_{DC}). To maintain consistency, the switching transition in Fig. 3 is considered throughout Sections II-VI. Additionally, for clarity, motor terminal (line-line) voltage and drive side output current, along with their respective peak overvoltage and overcurrent, are denoted as $v_M(t)$, $i_C(t)$, $v_{M(pk)}$ and $i_{C(pk)}$, respectively. i_C represents the negative phase A current $i_{\phi,A(t)}$, which is measured as the drive-side output current in DPTs in Section IV. The representation of phase B $i_{\phi,B(t)}$ and C $i_{\phi,C(t)}$ currents is also based on i_C assuming balanced three-phase conditions ($i_{\phi,B(t)} = i_{\phi,C(t)} = 0.5i_C(t)$).

The root cause of RWP for the switching transition in Fig. 3 is the excitation of the first antiresonance, located at frequency f_{RW}, in the combined DM impedance Z_{DM} of reactor L (2L-LF) or L_s (2L-SP), cable and motor by the dv/dt of S_{2A} [6], [23]. The antiresonances in Z_{DM} result from the interaction between the individual antiresonances in cable and motor load DM impedances $Z_{DM,C}$ and $Z_{DM,M}$, respectively [34]. Although, Z_{DM} has higher order antiresonances, their impact on RWP in 2L-LF configuration is negligible due to the presence of L which substantially lowers the value of f_{RW}, making it the dominant pole of the RWP transient [6], [35]. The same characteristic applies to 2L-SP due to the identical placement of L_s in 2L-SP as compared with the placement of L in 2L-LF.

For obtaining the DM equivalent circuit for modeling RWP transients for Fig. 3 to estimate $v_{M(pk)}$ and $i_{C(pk)}$, it is imperative to obtain DM impedance models for reactor L (2L-LF) or L_s (2L-SP), cable, and motor. The proceeding analysis develops the switching transition equivalent circuit for modeling RWP for the scenario in Fig. 3 for both drive configurations.

A. 2L-LF

The RWP for the 2L-LF scenario in Fig. 3(a) is initiated as the mid-point voltage of phase A steps from zero to V_{DC}, caused by turning ON of S_{2A}. In [35], a simplified lumped DM model is developed for modeling RWP in 2L-LF for the same switching transition. Therefore, for reference the same naming convention of variables is adopted for clarity. The circuit model is depicted in Fig. 4. The model comprises DM models for the L, cable, and motor, accurately modeling the first antiresonance of the actual DM impedance. The voltage source $v_S(t)$ represents the voltage step. Further, L_M represents the DM inductance of the motor which is 1.5 times the per phase inductance L_ϕ ($L_M = 1.5L_\phi$).

For ease of computation, the voltage step can be modeled as a unit step $V_{DC}u(t)$ [36]. However, a step voltage source $u(t)$ has an infinite dv/dt, which does not represent the actual device switching transient and overestimates $v_{M(pk)}$ and $i_{C(pk)}$ for a given cable model parameters and filter L value. To overcome this limitation, a ramp edge with a rise time T_R is considered (2), where T_R can be adjusted based on the device's switching dv/dt.

$$v_S(t) = \frac{V_{DC}}{T_R}\left(r(t) - r(t-T_R)\right) \tag{2}$$

The solution of the equivalent circuit with the ramp edge excitation is summarized in [35]. The response comprises DC (ramp edge) and AC components. The DC ramp edge defines the steady state voltage on the motor L_M, whereas the AC component represents the overvoltage ringing. The AC component, expressed in (4)-(5), comprises sinusoidal terms with angular frequency $\omega_{RW} = 2\pi f_{RW}$ and amplitude scaling factors $f(\boldsymbol{x})$ and $g(\boldsymbol{x})$, which are function of the initial conditions, the less-dominant second antiresonance ω_{P2}, and T_R (5). The expressions for ω_{RW}, $f(\boldsymbol{x})$, and $g(\boldsymbol{x})$ are provided in [35].

$$\begin{aligned} v_M(t) = &\frac{V_{DC}L_M}{T_R(1.5L+L_C+L_M)}\left(r(t) - r(t-T_R)\right) \\ &+ v_{AC}(t)u(t) + v_{AC}(t-T_R)u(t-T_R) \end{aligned} \tag{3}$$

$$v_{AC}(t) = f(\boldsymbol{x})\sin(\omega_{RW}t) + g(\boldsymbol{x})\cos(\omega_{RW}t) \tag{4}$$

$$\begin{aligned} \boldsymbol{x} = &[i_C(0^-), v_M(0^-), iL_M(0^-), iL_{MS}(0^-), v_{MP}(0^-) \\ &, \omega_{RW}, \omega_{P2}, T_R] \end{aligned} \tag{5}$$

Although in an actual motor drive system, the AC part in (3) decays over time due to system damping, the purpose of

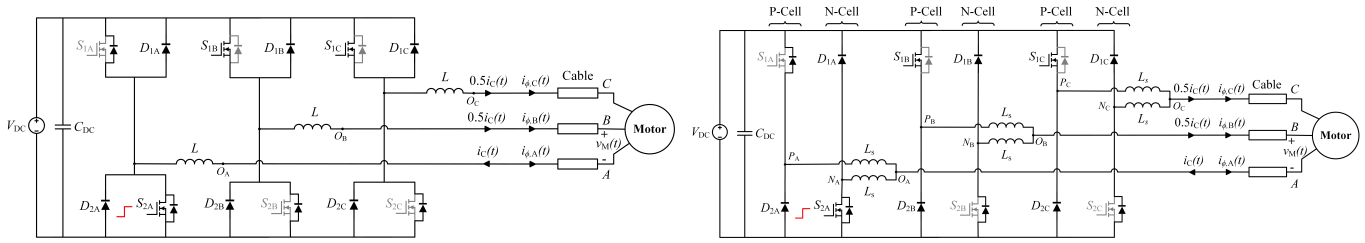

Fig. 3. Schematic for phase A S_{2A} OFF → ON switching transition with phase B and C clamped to the DC link. (a) 2L-LF. (b) 2L-SP.

(3) is to model the voltage rise/fall and estimate $v_{\mathrm{M(pk)}}$ which depends on the maximum value of the AC component and steady state load voltage. Therefore, the value of $v_{\mathrm{M(pk)}}$ using (3) can be expressed as follows

$$\begin{aligned} v_{\mathrm{M(pk)}} &= \frac{V_{\mathrm{DC}} L_{\mathrm{M}}}{(1.5L + L_{\mathrm{C}} + L_{\mathrm{M}})} + max\{v_{\mathrm{AC}}(t) - v_{\mathrm{AC}}(t - T_{\mathrm{R}})\} \\ &= \frac{V_{\mathrm{DC}} L_{\mathrm{M}}}{(1.5L + L_{\mathrm{C}} + L_{\mathrm{M}})} + 2\sin\left(\frac{T_{\mathrm{R}}}{2}\omega_{\mathrm{RW}}\right)\sqrt{f^2(\boldsymbol{x}) + g^2(\boldsymbol{x})} \end{aligned} \tag{6}$$

Further, the voltage across $1.5L + L_{\mathrm{C}}$ $(v_{\mathrm{S}}(t) - v_{\mathrm{M}}(t))$ can be integrated to obtain expression for $i_{\mathrm{C}}(t)$ (7). Consequently, (7) can be manipulated to derive the expression for $i_{\mathrm{C(pk)}}$ in (8) for a given $i_{\mathrm{C}}(0^-)$.

$$i_{\mathrm{C}}(t) = \frac{1}{(1.5L + L_{\mathrm{C}})} \int_0^t (v_{\mathrm{S}}(\tau) - v_{\mathrm{M}}(\tau))\, d\tau + i_{\mathrm{C}}(0^-) \tag{7}$$

$$i_{\mathrm{C(pk)}} = i_{\mathrm{C}}(0^-) + 2\sin\left(\frac{T_{\mathrm{R}}}{2}\omega_{\mathrm{RW}}\right)\left[\frac{\sqrt{f^2(\boldsymbol{x}) + g^2(\boldsymbol{x})}}{\omega_{\mathrm{RW}}(1.5L + L_{\mathrm{C}})}\right] \tag{8}$$

It is pertinent to mention that the equivalent circuit in Fig. 4 does not include the resistance for damping. The underlying reason is based on the observation that the overvoltage and overcurrent transients are underdamped ($\zeta < 1$), with $v_{\mathrm{M}}(t)$ and $i_{\mathrm{C}}(t)$ reaching their peaks $v_{\mathrm{M(pk)}}$ and $i_{\mathrm{C(pk)}}$ at the onset of the transient where the value damping scaling term $e^{-\alpha t} \approx 1$. Also, ignoring damping lowers the order of the characteristic function, yielding a closed-form solution [35].

Further, the argument of the sinusoidal scaling term is $(0.5T_{\mathrm{R}}\omega_{\mathrm{RW}})$. If $T_{\mathrm{R}} = nT_{\mathrm{RW}}$, where n is a set of positive integers $(n = 1, 2, 3, ...)$ and $T_{\mathrm{RW}} = 2\pi/\omega_{\mathrm{RW}}$, then the value of the scaling term $\sin(0.5T_{\mathrm{R}}\omega_{\mathrm{RW}})$ becomes zero. Consequently, the maximum term becomes zero, and the RWP is ideally eliminated. This is also consistent with the time and frequency-domain analysis presented in [23] to show that the RWP is suppressed when the rise/fall time equals nT_{RW}.

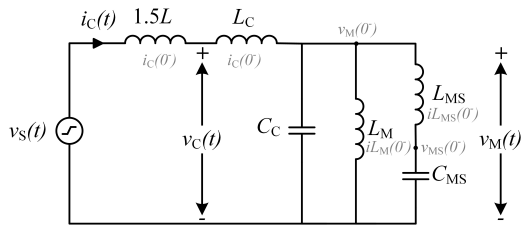

Fig. 4. Switching transition equivalent circuit for Fig. 3(a).

B. 2L-SP

In a 2L-SP drive, during the switching transition, the output and complementary cell's mid-point node voltage transient is determined by the equivalent circuit comprising L_{s}, C_{OSS}, and C_{J} (Fig. 2). Additionally, since the cable and motor are linked to the output node, the excitation of cable and motor parasitics, and consequently, the occurrence of RWP, is also impacted by the output and complementary cell's mid-point node voltage transient.

The excitation process for RWP in 2L-SP involves two subintervals, 1 and 2. Fig. 5 shows the equivalent circuits for the two subintervals and the corresponding specimen waveforms for the switching scenario in Fig. 3(b). The subinterval 1 starts at $t = 0$ with the turning ON of $S_{2\mathrm{A}}$. The output and complementary cell's mid-point node voltages $v_{\mathrm{OA}}(t)$ and $v_{\mathrm{PA}}(t)$ fall with a transient determined by the resonance between P and N-cell L_{s}, C_{OSS} and C_{J} of the P-cell and net DM inductance $0.25L_{\mathrm{s}}$ of phase B and C in series with cable and motor parasitics. Once the voltage of P_{A} reaches zero at $t = T_{\mathrm{Z}}$, the resonance ceases, concluding subinterval 1. Subinterval 2 then begins with a constant voltage V_{DC} applied across the DM equivalent circuit comprising net DM inductance $0.75L_{\mathrm{s}}$ due to split inductors in series with cable and motor. The initial conditions of the components for subinterval 2 are the values at the end of subinterval 1, which govern the transient profile and peak values of $v_{\mathrm{M}}(t)$ and $i_{\mathrm{C}}(t)$, respectively.

The closed-form expressions for $v_{\mathrm{M}}(t)$ and $i_{\mathrm{C}}(t)$ for the 2L-SP drive can be obtained by analytically solving and coupling expressions of both subintervals. However, the circuit for subinterval 1 is higher order and complex to be solved symbolically due to a higher-order characteristic function with a non-generalized closed-form solution. Therefore, subinterval 1 can be solved using numerical methods and the current and voltage values at $t = T_{\mathrm{Z}}$ can be passed onto subinterval 2. The circuit for subinterval 2 is identical to the 2L-LF circuit in Fig. 4 with ramp edge $v_{\mathrm{S}}(t)$ replaced with V_{DC}. The same procedure provided in [35] is followed to yield the following expressions for $v_{\mathrm{M}}(t)$ and $i_{\mathrm{C}}(t)$, along with their respective peaks, $v_{\mathrm{M(pk)}}$ and $i_{\mathrm{C(pk)}}$ (Appendix A).

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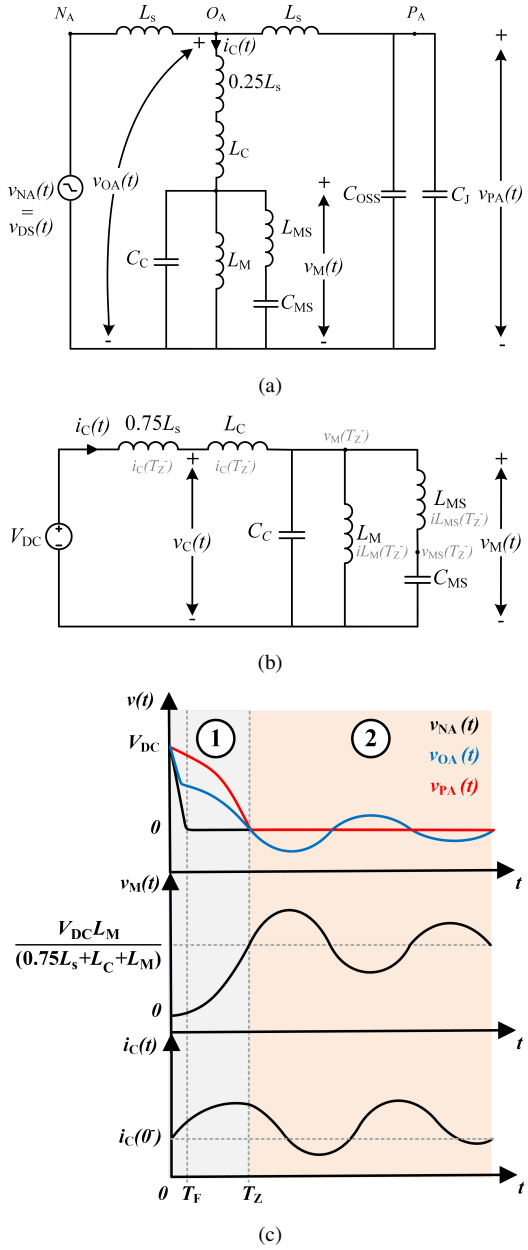

Fig. 5. Switching transition equivalent circuits for Fig. 3(b). (a) Subinterval 1. (b) Subinterval 2. (c) Switching transition waveforms.

$$v_{\mathrm{M}}(t) = \frac{V_{\mathrm{DC}}L_{\mathrm{M}}}{(0.75L_{\mathrm{s}}+L_{\mathrm{C}}+L_{\mathrm{M}})} + v_{\mathrm{AC}}(t) \tag{9}$$

$$v_{\mathrm{AC}}(t) = m(\boldsymbol{y})\sin(\omega_{\mathrm{RW}}t) + n(\boldsymbol{y})\cos(\omega_{\mathrm{RW}}t) \tag{10}$$

$$\boldsymbol{y}=[iL_{\mathrm{O}}(T_{\mathrm{Z}}^-), v_{\mathrm{M}}(T_{\mathrm{Z}}^-), iL_{\mathrm{M}}(T_{\mathrm{Z}}^-), iL_{\mathrm{MS}}(T_{\mathrm{Z}}^-), v_{\mathrm{MP}}(T_{\mathrm{Z}}^-), \omega_{\mathrm{RW}}, \omega_{\mathrm{P2}}] \tag{11}$$

$$\begin{aligned} v_{\mathrm{M(pk)}} &= \frac{V_{\mathrm{DC}}L_{\mathrm{M}}}{(0.75L_{\mathrm{s}}+L_{\mathrm{C}}+L_{\mathrm{M}})} + max\{v_{\mathrm{AC}}(t)\} \\ &= \frac{V_{\mathrm{DC}}L_{\mathrm{M}}}{(0.75L_{\mathrm{s}}+L_{\mathrm{C}}+L_{\mathrm{M}})} + \sqrt{m^2(\boldsymbol{y})+n^2(\boldsymbol{y})} \end{aligned} \tag{12}$$

$$i_{\mathrm{C}}(t) = \frac{1}{(0.75L_{\mathrm{s}}+L_{\mathrm{C}})}\int_0^t (v_{\mathrm{S}}(\tau)-v_{\mathrm{M}}(\tau))\,d\tau + i_{\mathrm{C}}(0^-) \tag{13}$$

$$\begin{aligned} i_{\mathrm{C(pk)}} &= i_{\mathrm{C}}(0^-) + max\left\{\frac{n(\boldsymbol{y})\sin(\omega_{\mathrm{RW}}t) - m(\boldsymbol{y})\cos(\omega_{\mathrm{RW}}t)}{\omega_{\mathrm{RW}}(0.75L_{\mathrm{s}}+L_{\mathrm{C}})}\right\} \\ &= i_{\mathrm{C}}(0^-) + \frac{\sqrt{m^2(\boldsymbol{y})+n^2(\boldsymbol{y})}}{\omega_{\mathrm{RW}}(0.75L_{\mathrm{s}}+L_{\mathrm{C}})} \end{aligned} \tag{14}$$

Likewise, as for the 2L-LF, $v_{\mathrm{M(pk)}}$ and $i_{\mathrm{C(pk)}}$ for 2L-SP also depend on the maximum sum of sinusoids (10). However, the presence of subinterval 1 in 2L-SP indicates a lower extent of RWP as the effective excitation of the cable and load circuit is lowered due to the gradual rise of the output voltage, as concluded in Section II. Further, the cable and motor load components (L_{C}, C_{C}, L_{M}, L_{MS} and C_{MS}) at the start of subinterval 2 have residual current and voltage in the same direction as subinterval 1, implying lower excitation impact of V_{DC} in subinterval 2 and hence lower extent of RWP compared with 2L-LF.

IV. RWP Investigation Through Double Pulse Tests

To analyze and compare RWP in 2L-LF and 2L-SP and validate the proposed DM equivalent circuit models in Section III, a DPT testbed is developed. Fig. 6 shows the DPT schematic and experimental setup. An in-house developed three-phase 2L-SP prototype [37], is utilized for performing DPT on the bottom device $S_{2\mathrm{A}}$ of phase A at 600 V and 31 A. The prototype specifications are listed in Table I. Contrary to the DPT approach in [6], [34], [38], the rationale behind this DPT configuration is to include impact of L_{s} in phase B and C, which in actual drive operation also interact with cable and motor load. The top devices $S_{1\mathrm{B}}$ and $S_{1\mathrm{C}}$ of phases B and C are latched in the ON state, while the grayed-out devices are latched in the OFF state by giving a constant high/low logic to their gate drivers. Further, the external ON and OFF gate resistances for $S_{2\mathrm{A}}$ are set to 2.5 Ω and 0.47 Ω, respectively.

TABLE I
2L-LF/2L-SP Configurable Drive Prototype Parameters

Parameter	Value
SiC MOSFET	CREE C3M0016120D
SiC Schottky Diode	Onsemi FFSH50120A
C_{DC} (μF)	240

For emulating motor, three inductors are developed with impedance response similar to a 2 kW motor [6], [39]. The load is connected to the drive (Fig. 6) with 4-wire 10 AWG 2 kV Lapp 700703 VFD cable. The cable ground wire and shield are connected to the grounded heat sink on the drive side and NEMA box enclosure on the load side. The DM impedances of cable $Z_{\mathrm{DM,C}}$, load $Z_{\mathrm{DM,M}}$ and cable with load $Z_{\mathrm{DM,CM}}$ for different cable lengths (1 m, 2 m, 4 m and 8 m) are measured with Keysight E4990 impedance analyzer based

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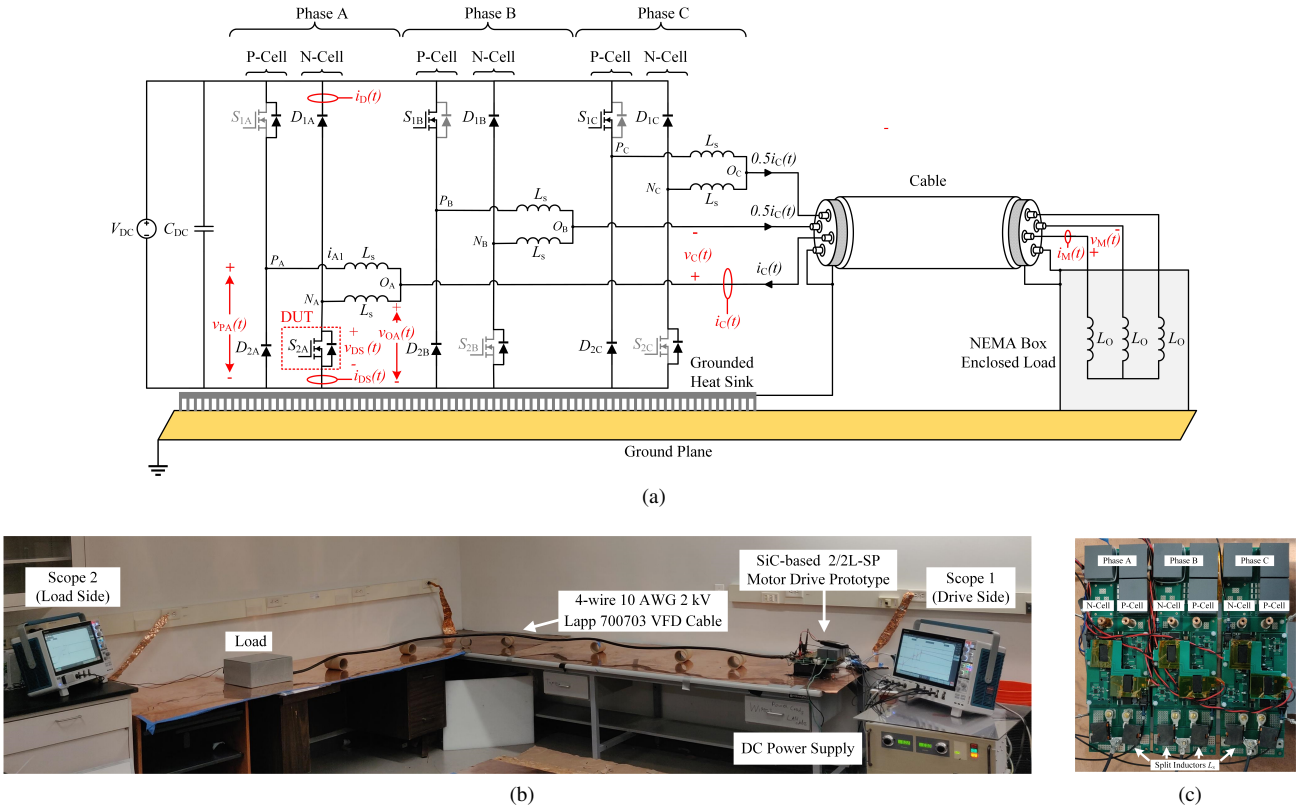

(a)

(b)

(c)

Fig. 6. Testbed for RWP investigation and comparison for 2L-LF and 2L-SP. (a) DPT schematic. (b) Experimental setup. (c) Drive prototype.

on the procedure summarized in [9]. The measurement results are presented in Fig. 7.

For validating the proposed DM circuit models in Section III, it is imperative to obtain values of $L_{\rm C}$, $C_{\rm C}$ for cable and $L_{\rm M}$, $L_{\rm MS}$ and $C_{\rm MS}$ for motor. The values can be estimated by manually characterizing the response to match the impedance response till the first antiresonance, which is tedious. To circumvent this, the Vector Fitting (VF) technique with enforced passivity is employed [40]–[42]. Table II and Table III summarize the obtained values of the cable and load components.

TABLE II
VF EXTRACTED CABLE PARAMETERS

Parameter	1 m	2 m	4 m	8 m
$L_{\rm C}$ (nH)	170.95	278.86	575.84	926.01
$C_{\rm C}$ (pF)	140.20	203.46	381.50	815.07

TABLE III
VF EXTRACTED LOAD PARAMETERS

Parameter	Value
$L_{\rm M}$ (μH)	275.12
$L_{\rm MS}$ (μH)	4.40
$C_{\rm MS}$ (pF)	14.28

A. DPT Results

DPTs are performed for all four cable lengths (1 m, 2 m, 4 m and 8 m) for five values of L (0 μH, 0.075 μH, 0.5 μH, 2.35 μH and 5 μH) for 2L-LF and (0 μH, 0.15 μH, 1 μH, 4.7 μH and 10 μH) for 2L-SP, respectively. The 0-5 μH range for L and 0-10 μH range for $L_{\rm s}$ is chosen to keep the maximum % impedance/inductance to within 3 % of the per-phase value $L_\phi = (2/3)L_{\rm M} = 183.41$ μH (Table III) [43]. The DPT pulse widths are chosen to prevent occurrence of double pulsing. The 2L-LF configuration is realized from 2L-SP by shorting the P and N-cell midpoints using a thick copper busbar, resulting in $L = 0.5L_{\rm s}$. The $L_{\rm s} = 0$ μH case implies the traditional 2L configuration, implemented by shorting the P and N-cell midpoints with $L_{\rm s}$ removed. For non-zero values of $L_{\rm s}$, commercially available off-the-shelf (COTS) inductors from Coil Crafts are utilized. Fig. 8 and Fig. 9 compare the time-domain waveforms for load side voltage $v_{\rm M}(t)$ and drive side current $i_{\rm C}(t)$ for 1 m and 8 m cable lengths for two values of L (0 μH and 5 μH) and $L_{\rm s}$ (0 μH and 10 μH).

For 1 m cable with 2L configuration ($L = L_{\rm s} = 0$), the overvoltage and overcurrent transients in $v_{\rm M}(t)$ and $i_{\rm C}(t)$ have modulated ringing pattern due to proximity of first two antiresonances (19.81 MHz and 27.67 MHz) in $Z_{\rm DM}$ in Fig. 7(c). The modulated ringing pattern is absent in both 2L-LF and 2L-SP and only the first antiresonance $f_{\rm RW} = 4.48$ MHz appears in $v_{\rm M}(t)$ and $i_{\rm C}(t)$ for both configurations. The value of $f_{\rm RW}$ is same for both configurations as the net DM inductance $1.5L$ for 2L-LF and $0.75L_{\rm s}$ for 2L-SP in Fig. 4 and Fig. 5 is equal, which also sets a fair basis for benchmarking performance of 2L-SP. Further, for the 8 m cable, the transients have lower value of $f_{\rm RW}$ than 1 m for all three configurations 2L (5.83 MHz), 2L-LF (1.89 MHz) and 2L-SP (1.89 MHz).

Moreover, in terms of $v_{\rm M(pk)}$ and $i_{\rm C(pk)}$, for 1 m, the 2L-LF and 2L-SP configurations result in an unexpectedly higher $v_{\rm M(pk)}$ than 2L. In particular, the values of $v_{\rm M(pk)}$ for the first

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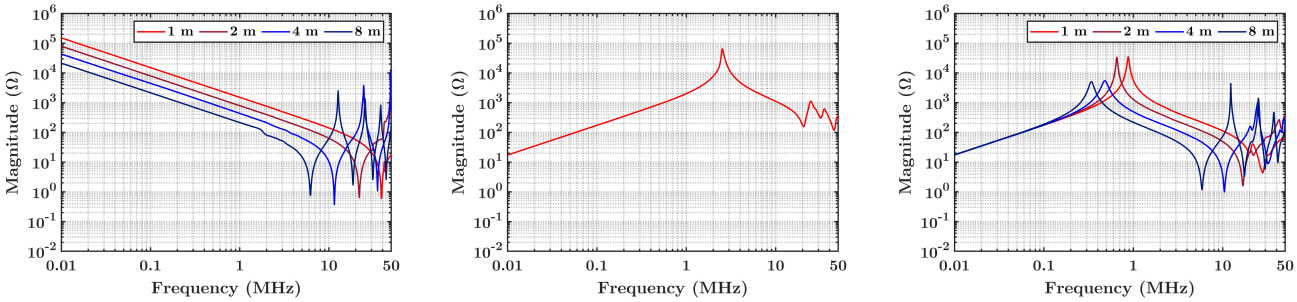

Fig. 7. Measured DM impedances. (a) $Z_{\mathrm{DM,C}}$. (b) $Z_{\mathrm{DM,M}}$. (c) $Z_{\mathrm{DM,CM}}$.

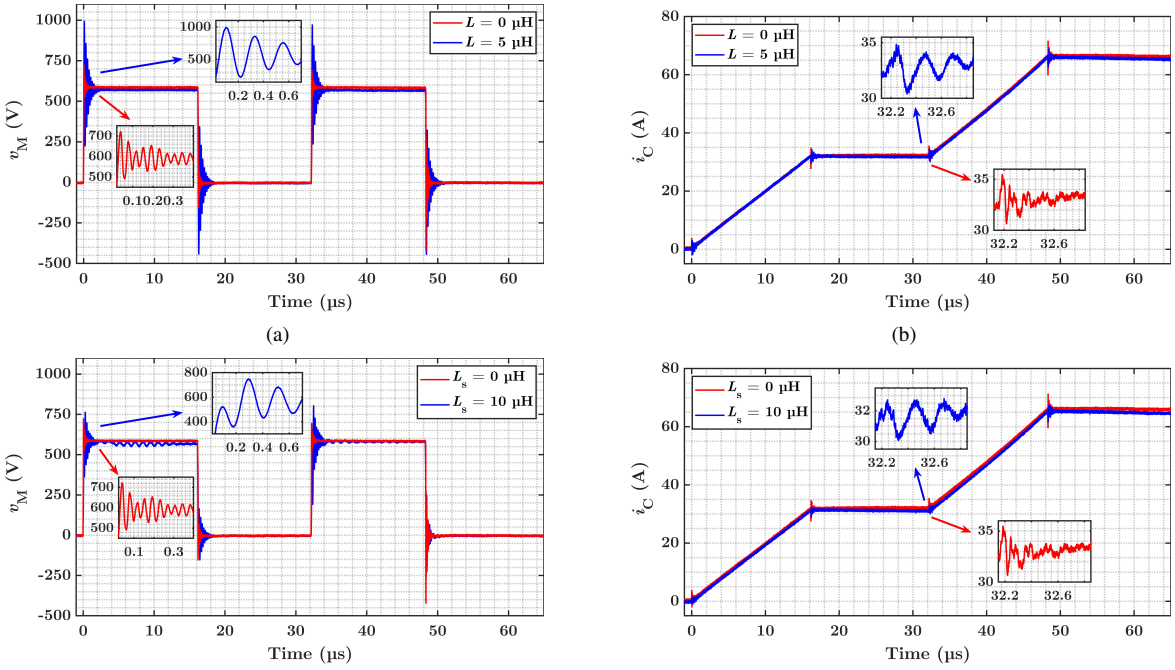

Fig. 8. DPT results for 1 m cable (a) $v_{\mathrm{M}}(t)$ (2L-LF). (b) $i_{\mathrm{C}}(t)$ (2L-LF). (c) $v_{\mathrm{M}}(t)$ (2L-SP). (d) $i_{\mathrm{C}}(t)$ (2L-SP).

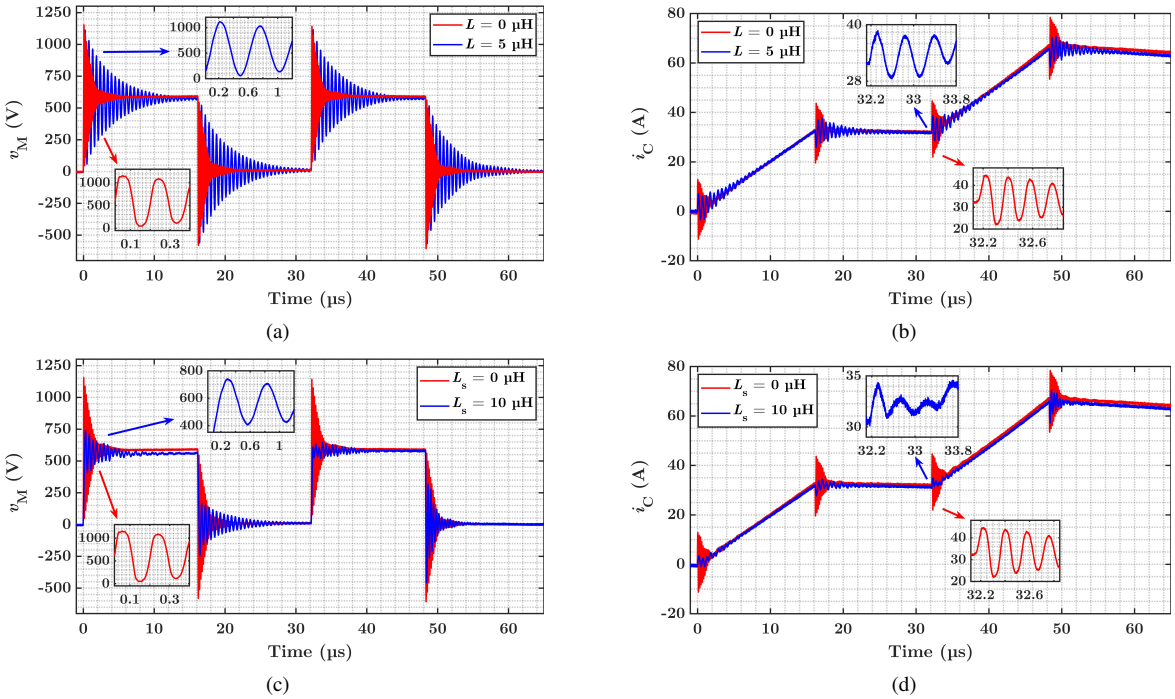

Fig. 9. DPT results for 8 m cable (a) $v_{\mathrm{M}}(t)$ (2L-LF). (b) $i_{\mathrm{C}}(t)$ (2L-LF). (c) $v_{\mathrm{M}}(t)$ (2L-SP). (d) $i_{\mathrm{C}}(t)$ (2L-SP).

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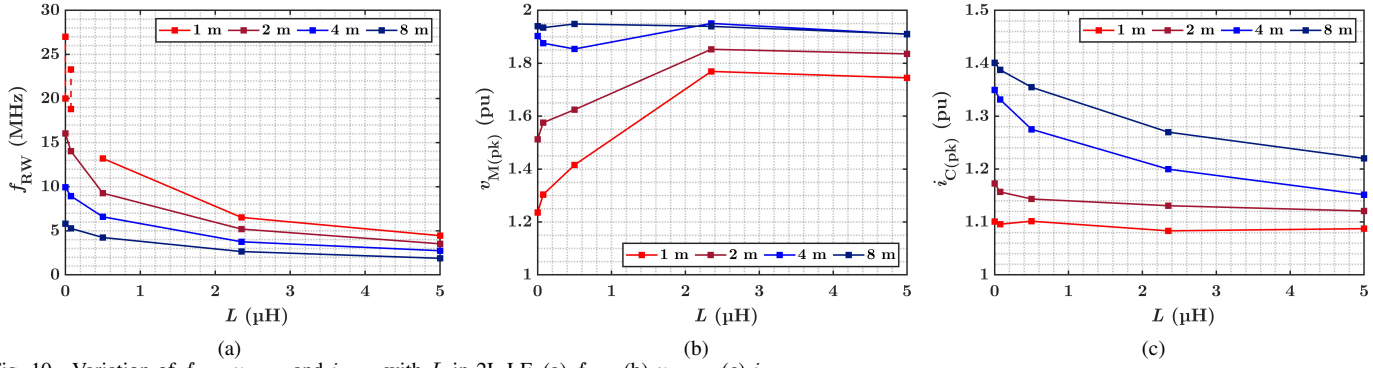
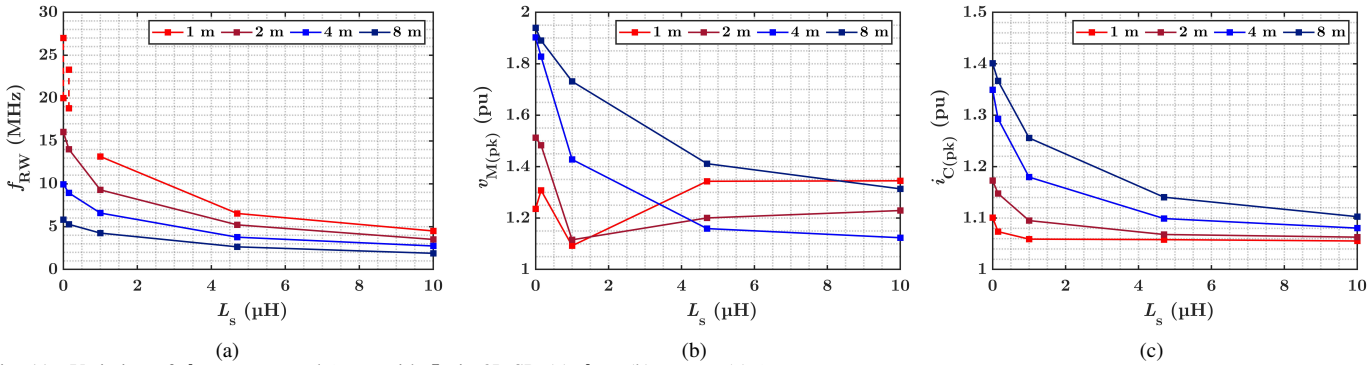


(a) (b) (c)

Fig. 10. Variation of f_{RW}, $v_{M(pk)}$ and $i_{C(pk)}$ with L in 2L-LF. (a) f_{RW}. (b) $v_{M(pk)}$. (c) $i_{C(pk)}$.



(a) (b) (c)

Fig. 11. Variation of f_{RW}, $v_{M(pk)}$ and $i_{C(pk)}$ with L_s in 2L-SP. (a) f_{RW}. (b) $v_{M(pk)}$. (c) $i_{C(pk)}$.

rising pulse edge for $L = 5$ µH (2L-LF) and $L_s = 10$ µH (2L-SP) are 933.4 V and 745.6 V, respectively, which surpass the peak value of 721.6 V for the simple 2L. Compared with 2L-LF, the increase in $v_{M(pk)}$ for 2L-SP is subtle. However, for $i_{C(pk)}$, no significant change is observed for both configurations.

In contrast, for 8 m, significant overvoltage and overcurrent transients in $v_M(t)$ and $i_C(t)$ appear for the 2L configuration. For instance, during the first rising pulse edge, $v_{M(pk)}$ reaches a recorded value of 1154 V and $i_{C(pk)}$ for the turn-ON transient of the second pulse at 31 A nominal is 43.91 A. For 2L-LF, $v_{M(pk)}$ decreases slightly to 1110 V, while $i_{C(pk)}$ is reduced to 38.44 A. On the other hand, the 2L-SP provides a significant reduction in both $v_{M(pk)}$ and $i_{C(pk)}$, with values of 732.7 V and 33.94 A, respectively.

Further, the variation of measured f_{RW}, $v_{M(pk)}$ (first rising edge) and $i_{C(pk)}$ (turn ON of second DPT pulse) with L (2L-LF) and L_s (2L-SP), for all cable lengths is summarized in Fig. 10 and Fig. 11. $v_{M(pk)}$ and $i_{C(pk)}$ are plotted in per unit based on their respective steady-state values as the base.

For f_{RW}, the measured values are the same for both configurations and vary inversely with inductance. The rationale behind this is the dependence of f_{RW} on the combined impedance of cable, load and net DM inductance $1.5L$ (2L-LF) and $0.75L_s$ (2L-SP), which is kept the same ($L = 0.5L_s$) for the DPTs. Additionally, for all cases except lower values of L and L_s for 1 m cable, the measured f_{RW} is the first antiresonance. This is attributed to the considerable spacing between the first two antiresonances f_{RW1} and f_{RW2}, as evident in Fig. 7(c) [44].

In contrast, for $v_{M(pk)}$, a dissimilar trend is observed between short (1 m and 2 m) and long (4 m and 8 m) cable lengths for both configurations. For long cables, $v_{M(pk)}$ falls as L and L_s increases, but the trend is steeper for 2L-SP. For instance, for 4 m cable, the reduction in overvoltage amplitude above the steady-state value, going from $L = 0$ µH to $L = 5$ µH, is a mere 1% for 2L-LF, whereas it is 63 % for 2L-SP. The significant reduction observed for 2L-SP is the presence of subinterval 1, which gradually excites the components of the cable and load equivalent circuits, as discussed in Section III. Conversely, for short cables, an undistorted rising trend is observed for 2L-LF, whereas for 2L-SP, a dip is seen at $L_s = 1$ µH followed by a gradual rise. However, overall, $v_{M(pk)}$ values for 2L-SP are lower than 2L-LF for short cables.

Lastly, similar to f_{RW}, $i_{C(pk)}$ exhibits an inverse falling trend with L and L_s, with the trend being steeper for longer cable lengths (4 m and 8 m). However, for the same cable length, the reduction in $i_{C(pk)}$ with increasing inductance is more significant for 2L-SP than 2L-LF. For instance, for the 4 m cable, the reduction in overcurrent amplitude, going from $L = 0$ µH to $L = 5$ µH, is 56.5 % for 2L-LF, whereas it is 76.8 % for 2L-SP.

V. Increasing $v_{M(pk)}$ Pattern with Short Cables in 2L-LF and 2L-SP

The unexpected rising trend of $v_{M(pk)}$ in Fig. 10(b) and Fig. 11(b) for 1 m and 2 m cables for both 2L-LF and 2L-SP configurations, contradicts the pattern observed for long cables. To analyze this trend, a MATLAB code employing the proposed models from Section III is developed to generate load side waveforms for predicting $v_{M(pk)}$ in 1 m and 2 m cables

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for both configurations. The cable and load parameters listed in Table II and Table III are utilized. The value of switching $\mathrm{d}v/\mathrm{d}t$ of excitation sources $v_{\mathrm{S}}(t)$ and $v_{\mathrm{NA}}(t) = v_{\mathrm{DS}}(t)$, in Fig. 4 and Fig. 5 is extracted from the DPT results. Further, for 2L-SP, the values of C_{OSS} and C_{J} for the subinterval 1 are extracted from the device datasheet at 600 V.

Fig. 12(a) and Fig. 12(b) compare the experimental and proposed circuit model generated waveforms for 2 m cable for $L = 2.35$ µH and $L_{\mathrm{s}} = 4.7$ µH. The proposed circuits accurately model the rising transient for both configurations as the slew rate of the device in $v_{\mathrm{S}}(t)$ is considered. For 2L-SP, the two subintervals are evident and the model accurately predicts the trajectory of $v_{\mathrm{OA}}(t)$, $v_{\mathrm{PA}}(t)$ and $v_{\mathrm{M}}(t)$.

Further, for $v_{\mathrm{M(pk)}}$, the proposed models for 2L-LF and 2L-SP slightly overestimate the value. For 2L-LF, the difference is 27 V, whereas for 2L-SP its 42 V. The overestimation is attributed to two factors. The first is that the actual device switching transient is not perfectly linear and has high and low instantaneous $\mathrm{d}v/\mathrm{d}t$ regions. However, in the proposed model, the linear ramp is considered. Secondly, for 2L-SP, $v_{\mathrm{M(pk)}}$ is achieved at the second peak of the oscillation where the value of damping scaling term $e^{-\alpha t}$ is slightly less than 1, causing a slightly more difference between the measured and predicted $v_{\mathrm{M(pk)}}$. For 2L-LF, the difference is less as $v_{\mathrm{M(pk)}}$ is achieved during the first peak of the oscillation. Lastly, as the proposed model is based on the lossless system without damping, the difference between the measured and modeled waveforms increases as time increases due to system damping. Overall, the proposed DM equivalent circuits effectively model the RWP transient, especially subintervals for 2L-SP, and estimate $v_{\mathrm{M(pk)}}$ with less than 6 % error for both configurations.

Consequently, the developed MATLAB code is extended to generate the $v_{\mathrm{M(pk)}}$ vs inductance pattern for 2L-LF and 2L-SP for 1 m and 2 m meter cables. The comparison of the modeled trend with experimental data is presented in Fig. 13. The modeled trend follows the same as the measured, justifying the efficacy of the proposed equivalent circuit models in predicting $v_{\mathrm{M(pk)}}$ for a given cable-motor system and inverter parameters.

Further, it is important to note that the rising overvoltage pattern is attributed to the collective impact of the variables, whose values are drive and system configuration specific, within the argument vector $\boldsymbol{x}$ and $\boldsymbol{y}$, governing the expression of overvoltages (6) and (12). These variables encompass circuit components, initial conditions, and T_{R} of the drive output pulse. Nevertheless, these variables are highly coupled in (6) and (12). Therefore, the individual impact of each variable can be explored through a dedicated sensitivity analysis study such as Monte Carlo.

A. 2L-SP Inverter for Integrated Motor Drive

Integrated Motor Drives (IMDs) are popular for space constrained applications such as electric vehicles and railway traction systems [45]. An IMD system comprises motor, drive and associated control and communication systems housed in a single package. The motor drive is directly interfaced with the motor without cable, thereby reducing the risk of overvoltage and overcurrent, due to RWP [45], [46].

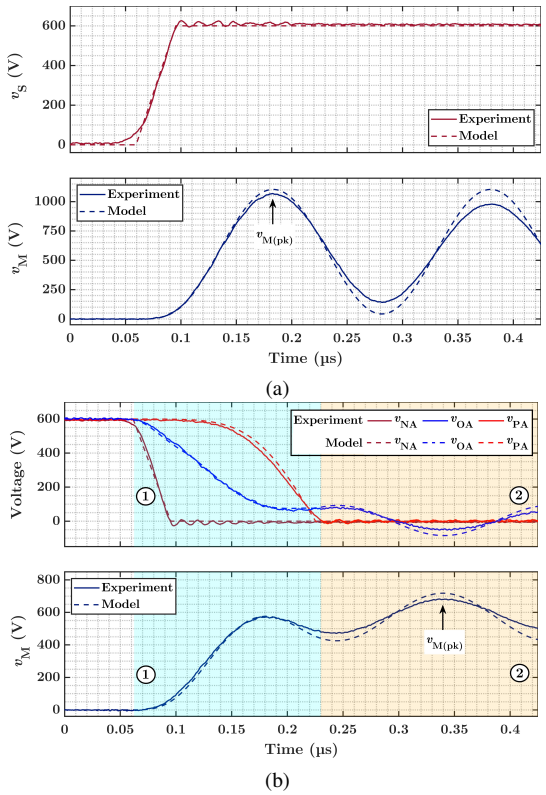

Fig. 12. Comparison of experimental and proposed circuit model generated $S_{2\mathrm{A}}$ turn-ON transient waveforms for the first DPT pulse for the 2 m cable. (a) 2L-LF with $L = 2.35$ µH. (b) 2L-SP with $L_{\mathrm{s}} = 4.7$ µH.

The 2L-SP inverter is a promising candidate for 2L IMDs due to its lower switching loss and high cross-talk immunity compared with the 2L topology [27]. However, the possible exacerbation of RWP due to split inductors, the fundamental component of this topology, raises concerns about its feasibility for an IMD application. As shown in Fig. 11, for a 1 m cable length, which is roughly comparable to an IMD system, an increase in L_{s}, except for $L_{\mathrm{s}} = 1$ µH, results in higher $v_{\mathrm{M(pk)}}$ exceeding the value obtained with the simple 2L configuration ($L_{\mathrm{s}} = 0$ µH). This trend suggests that increasing L_{s} could potentially also lead to high $v_{\mathrm{M(pk)}}$ in an IMD. Therefore, it is crucial to investigate RWP in a 2L-SP-based IMD.

Furthermore, the 2L-LF configuration also shows a higher $v_{\mathrm{M(pk)}}$ than the 2L-SP for short cables in Fig. 11, prompting further investigation. However, it is pertinent to mention that the 2L-LF configuration is intended for mitigating RWP in cable-connected motor drive systems [6], [38]. Therefore, the 2L-LF configuration holds no practical significance and viability for an IMD application.

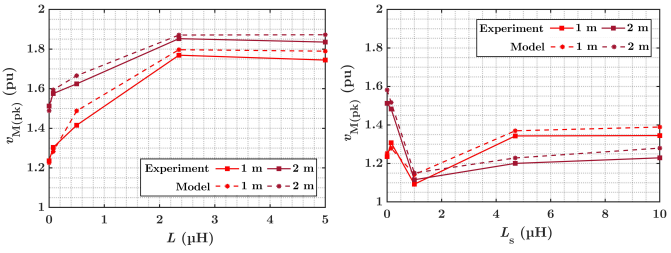

Fig. 13. Comparison of experimental and proposed circuit model calculated $v_{\mathrm{M(pk)}}$ variation with inductance for short cables. (a) 2L-LF. (b) 2L-SP.

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The same experimental setup in Fig. 6 is reconfigured to emulate an IMD by connecting the load to the output of the converter prototype. DPTs are performed for the same five values of L_s (0 µH, 0.15 µH, 1 µH, 4.7 µH and 10 µH) at 600 V. Fig. 14 compare the time domain waveforms of $v_M(t)$ and $i_C(t)$ for the two extreme values. Contrary to the results for 1 m cable in Fig. 8, there is no increase in $v_{M(pk)}$ for $L_s = 0$ µH (2L) compared with $L_s = 10$ µH, except that the dv/dt and ringing frequency for the latter is lower. Similarly, there is no significant variation in $i_C(t)$ for both L_s values.

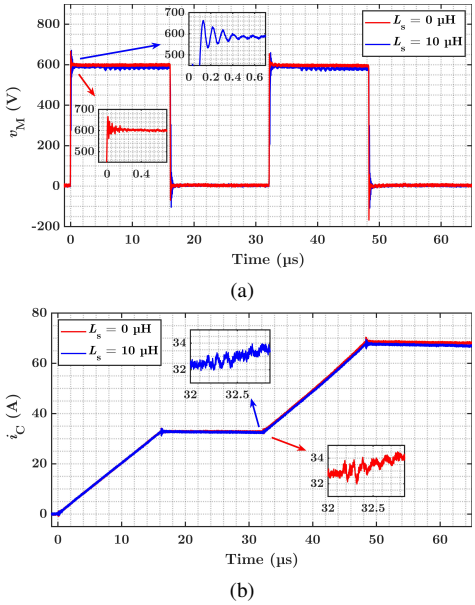

Fig. 14. DPT results for 2L-SP-based IMD configuration for $L_s = 0$ µH and $L_s = 10$ µH. (a) $v_M(t)$. (b) $i_C(t)$.

Further, Fig. 15 provides a summary of the per-unit variations of $v_{M(pk)}$ and $i_{C(pk)}$ with L_s. Both parameters exhibit a consistently flat trend as L_s varies. $v_{M(pk)}$ shows minor fluctuations above and below its value at $L_s = 0$ µH, while $i_{C(pk)}$ falls slightly by 4 % as L_s increases.

The time-domain waveforms in Fig. 14 and the flat trend in Fig. 15 suggest that increasing split inductance in 2L-SP does not exacerbate the RWP phenomenon, as hypothesized. The underlying reason can be explained from the equivalent circuit in Fig. 5. For an IMD, cable components L_C and C_C are no longer in the circuit. With C_C removed, the impedance mismatch at the motor terminals ($v_M(t)$) is minimized, lowering the extent of RWP. The little overvoltage ringing observed in $v_M(t)$ in Fig. 14 at switching transition is due to the excitation of the antiresonance of the motor/load [47].

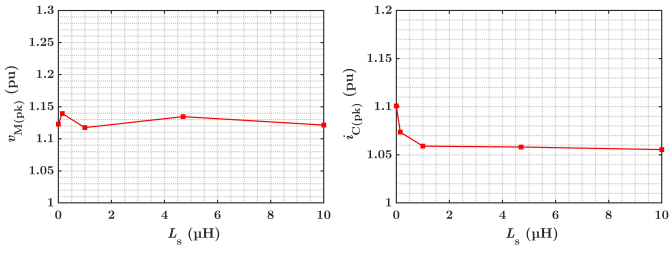

Fig. 15. Variation of measured $v_{M(pk)}$ and $i_{C(pk)}$ with L_s for 2L-SP-based IMD.

VI. Switching Performance Evaluation

Apart from the RWP, the performance and efficiency of a motor drive is dependent on the switching performance of the device. Compared with Si, the high dv/dt and di/dt switching capability of SiC devices plays a crucial role in reducing switching losses (E_{SW}) and dead time for complementary switches in a phase-leg and permitting high switching frequency operation. However, due to their small intrinsic junction capacitance C_{OSS}, the switching behavior of SiC devices is more susceptible to converter and load parasitics [48], [49].

For motor drives, the load parasitics include the cable and motor parasitics, which form a complex impedance network. This complex network does not behave inductively in the device switching-related frequency range (in MHz), impacting the switching transient [34]. In [38], the switching performance of 2L-LF is analyzed and benchmarked against 2L for a 7.5 kW motor connected using 2 m cable. It is shown that for 2L, the antiresonances of the cable and motor load DM impedance cause additional high-frequency ringing current to flow through the device during switching, lowering dv/dt and increasing E_{SW}. In contrast, the auxiliary inductor L in 2L-LF configuration is shown to provide decoupling between load parasitics and the device, leading to up to 10 % reduction in E_{SW} than 2L. Similarly, in [6], the switching performance of 2L-LF is analyzed for a 100 kW PM motor connected through a 4 m cable. The tests conclude 9.1 % reduction in switching loss than 2L configuration. Nevertheless, in both works, the evaluation is only conducted for one cable length.

The 2L-SP topology shows prospects of decoupling the cable and load parasitics from the device during the switching transition. In [27], the switching performance of a SiC-based 2L-SP is investigated through DPT. According to the results, L_s decouples the capacitance of devices in the complementary cell from the switching device. As a result, the turn-ON loss E_{ON} is decreased while the turn-OFF loss E_{OFF} is increased. However, the total loss $E_{SW} = E_{ON} + E_{OFF}$ is lower than 2L. The increase in E_{OFF} is attributed to an increase in turn-OFF dv/dt, which increases the v_{DS} and i_{DS} overlap. Nonetheless, DPTs performed in this work are with a simple DPT inductor, which does not fully represent the cable and motor load. Therefore, it is necessary to analyze the switching performance of 2L-SP for motor drive applications with varying cable lengths to determine if the same trend follows.

The measured switching transients of the DPTs presented in Sections IV and V are used to calculate E_{ON} and E_{OFF} and measured ON and OFF dv/dt for both 2L-SP and 2L-LF for all cable lengths. For 2L-SP, the IMD case is also considered. To ensure accuracy in the E_{SW} calculation, the V-I alignment procedure in [50] is followed. Fig. 16 compares the time-domain turn-ON and OFF switching transient waveforms of S_{2A} and associated with switching energies for 8 m for 2L, 2L-LF ($L = 5$ µH) and 2L-SP ($L_s = 10$ µH). Similar to [27], for 2L-SP E_{ON} is substantially lower, by 50 %, whereas E_{OFF} is higher, by 83 %, than 2L and 2L-LF due to higher turn-OFF dv/dt. Nevertheless, the total E_{SW} for 2L-SP (658 µJ) is lower than 2L (852 µJ) and 2L-LF (774 µJ). Moreover, the

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v_{DS} of S_{2A} for ON and OFF transients for 2L and 2L-LF has a little ringing pattern superimposed on the large-signal voltage step. Whereas for 2L-SP, the transition is smooth with higher ON and OFF dv/dt of 19.5 V/ns and 35.8 V/ns than 15.8 V/ns and 20 V/ns for 2L-LF and 14.5 V/ns and 18.1 V/ns for 2L, respectively.

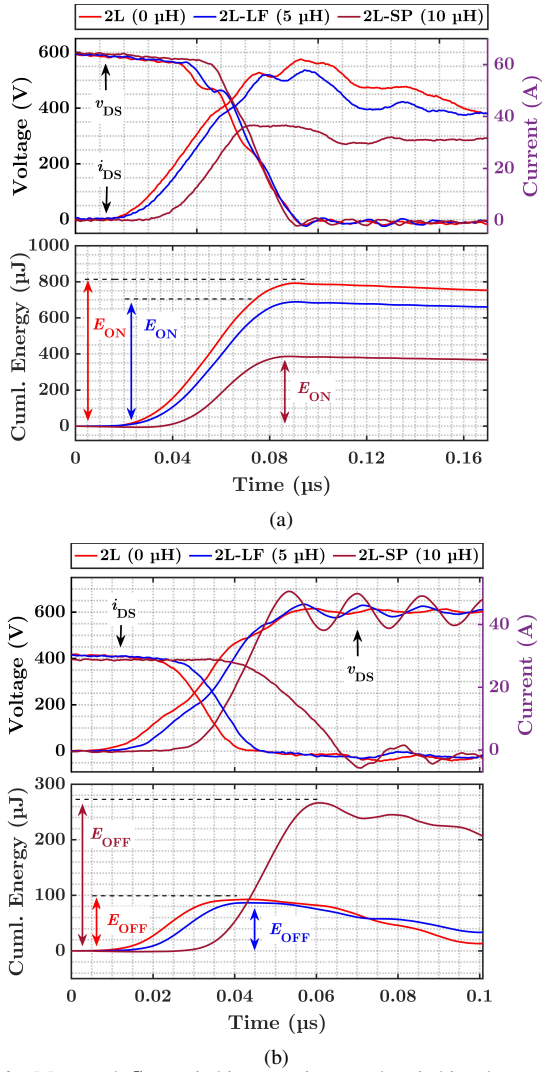

Fig. 16. Measured S_{2A} switching transients and switching losses for 8 m cable. (a) Turn-ON. (b) Turn-OFF.

The variation of ON and OFF dv/dt for all cable lengths and inductances for both configurations is plotted in Fig. 17. In the case of 2L-LF, both ON and OFF dv/dt exhibit variance for lower values of L. The dv/dt value increases slightly till $L = 0.5$ µH and then saturates for all cable lengths, implying decoupling of load parasitics from the device. The net average increase in ON and OFF dv/dt from the 2L baseline case is 1.8 V/ns and 1.2 V/ns, respectively. Likewise, for 2L-SP, both ON and OFF dv/dt increase with L_s until $L_s = 4.7$ µH and saturate around the same value for all cable lengths. This implies that the impedance offered by $L_s > 4.7$ µH is large enough to fully decouple cable and motor load parasitics, regardless of the cable length. However, compared with 2L-LF, the net average increase in dv/dt for 2L-SP from the 2L baseline case is notably higher, with values of 5.5 V/ns for ON and 23.2 V/ns for OFF dv/dt, respectively. The higher dv/dt observed for 2L-SP is attributed to the additional decoupling of the capacitance of complementary cell devices (Phase A P-cell for the given case) by L_s. In contrast, for 2L-LF, the complementary cell devices are paralleled with the switching device, increasing overall capacitance and lowering the switching speed.

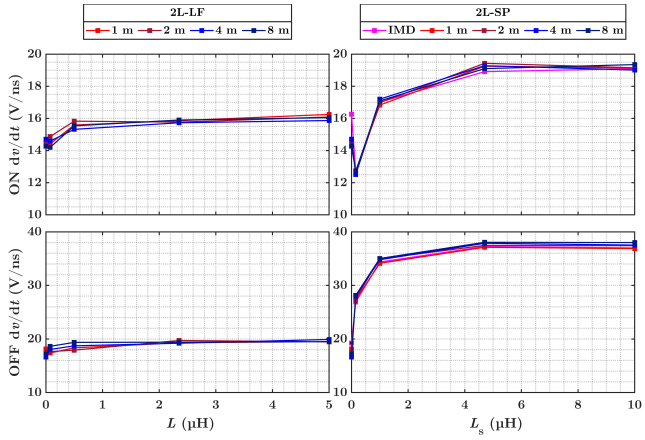

Fig. 17. Comparison of ON and OFF dv/dt for both configurations for all cable lengths.

Further, the switching loss trend for both configurations is summarized in Fig. 18. For 2L-LF, E_{ON} and E_{OFF} show a slightly falling trend with an increase in L for all cable lengths. In contrast, for 2L-SP, the switching energies follow a trend similar to what is presented in [27]. E_{ON} falls sharply until $L_s = 1$ µH and then saturates, reaching nearly the same value for all cable lengths. This trend is due to a higher ON dv/dt, which leads to a smaller overlap between v_{DS} and i_{DS} in 2L-SP than in 2L-LF. On the other hand, E_{OFF} follows a rising pattern until $L_s = 1$ µH and then saturates, remaining invariant for all cable lengths. This trend is attributed to a higher OFF dv/dt, which leads to a higher overlap between v_{DS} and i_{DS}. Despite having a higher E_{OFF}, the total loss E_{SW} for 2L-SP for $L_s > 1$ µH is nearly 17 % lower than 2L-LF.

Based on the trends shown in Fig. 17 and Fig. 18, it can be concluded that in both 2L-LF and 2L-SP, irrespective of cable length, the motor and cable parasitics are decoupled from the switching device if the inductance of L and L_s is large. A large value of L and L_s lowers the ringing frequency of additional currents induced due to cable and motor load parasitics. As a result, the resonant period of the parasitics-induced currents is much longer than the switching commutation time, eliminating the influence of these currents on the switching transient [38].

Further, from the design perspective, the criterion developed for 2L-LF in [38] is also extendable to 2L-SP as the DM impedance $1.5L$ (2L-LF) and $0.75L_s$ (2L-SP) for $L = 0.5L_s$ is identical. Lastly, in addition to decoupling the load parameters, 2L-SP decouples the capacitance of the complementary cell devices from the switching device, further lowering E_{SW} and increasing motor drive efficiency compared with both 2L and 2L-LF.

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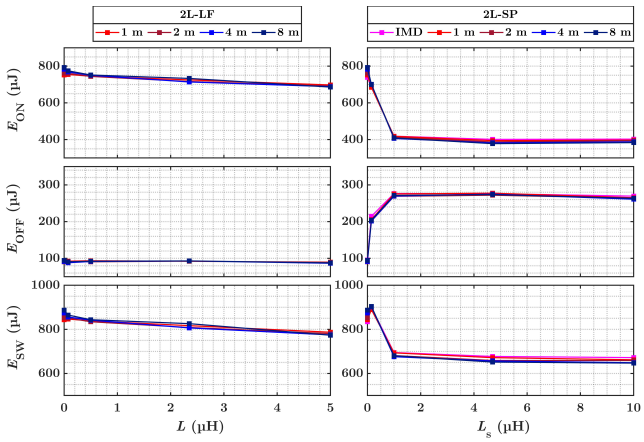

Fig. 18. Comparison of E_{ON}, E_{OFF} and E_{SW} for both configurations for all cable lengths.

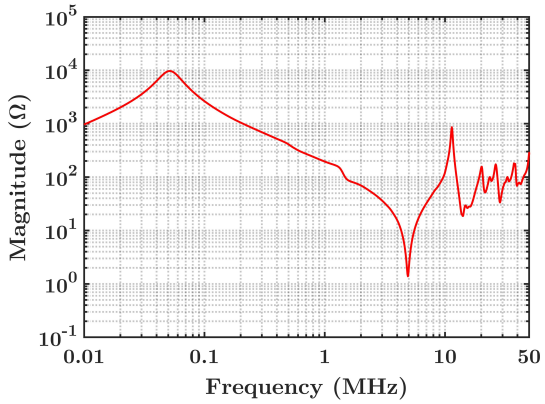

Fig. 19. Measured $Z_{DM,M}$ of RL load.

VII. RWP Investigation Under Continuous Operation

The DPT approach in Section IV provides an insight into the occurrence of RWP in 2L-SP and 2L-LF drives. However, the DPT approach in Section IV focuses on one switching state, which does not emulate the RWP in an actual motor drive system where the output voltage and current waveform vary over one fundamental cycle f_O, synthesized by transitioning between different switching states in a pattern [7].

Further, as evident in the simplified DM equivalent circuit models in Section III, the transients in $v_M(t)$ and $i_C(t)$ are a function of initial conditions $i_C(0^-)$, $v_M(0^-)$, $iL_M(0^-)$, $iL_{MS}(0^-)$ and $v_{MP}(0^-)$ at the start of switching transition and the dv/dt of the switch. Therefore, the RWP in a motor drive system is expected to vary for each switching transition due to varying initial conditions and switching dv/dt over f_O and hence warrants RWP performance evaluation of 2L-SP in continuous operation and its comparison with 2L and 2L-LF.

The experimental setup in Fig. 6 is reconfigured for continuous testing for 8 m cable. The inductive load is replaced with a three-phase RL load with phase resistance R_{PH} = 10 Ω and L_{PH} = 15.1 mH to emulate a loaded induction motor operating at 0.87 power factor. The RL load is constructed using high-power wire wound resistors from Ohmite and three-phase reactors from MTE connected in series. The emulation of the motor using an RL load is predominantly employed in the literature for evaluating motor drive topologies [7], [23], [51], [52]. The impedance response $Z_{DM,M}$ is depicted in Fig. 19, with high-frequency response similar to 15 kW and 5.5 kW motors in [6] and [39], respectively.

Further, SPWM is chosen and implemented on an Intel Cyclone IV FPGA for drive modulation with 30 kHz and 60 Hz as the carrier and fundamental frequencies, respectively. The SPWM modulation index is set to 0.86 to achieve 208 V L-L RMS output voltage from the drive at 400 V DC link. Lastly, Tektronix Tekscope PC Analysis tool is utilized to capture and view waveforms from the drive and load side oscilloscopes on a single screen.

Fig. 20 compares the drive and load side phase A to phase B line-to-line voltages $v_C(t)$ and $v_M(t)$ and phase A currents $i_C(t)$ and $i_M(t)$ for 2L, 2L-LF (L = 5 µH) and 2L-SP (L_s = 10 µH) configurations. For 2L-LF and 2L-SP, $v_C(t)$ is measured across the cable terminals after the inductors. As can be noticed, for 2L, significant overvoltage and overcurrent exist in $v_M(t)$ and $i_C(t)$. The peak of $v_M(t)$ levels around $2V_{DC}$ with few peaks, exceeding $2V_{DC}$ and reaching 870 V due to double-pulsing and varying load current [6], [7].

In the case of 2L-LF, a notable reduction of 30.1 % in overcurrent amplitude is observed in $i_C(t)$. However, the overvoltage in $v_M(t)$ is exorbitant, with overvoltage peak reaching upto 998 V for few pulses. The underlying reason is severe double-pulsing, compared with 2L, due to lower f_{RW} caused by the presence of L and large oscillation damping time. This is evident in Fig. 9(a) and is also discussed in [6].

In contrast, the 2L-SP configuration shows the least RWP. The maximum overvoltage observed is 642 V, which in terms of amplitude is 48.5 % and 59.5 % lower than 2L and 2L-LF, respectively. Likewise, there is a 81.9 % reduction in overcurrent amplitude compared with 2L and a 74.1 % reduction compared with 2L-LF. This is because the cable and load parasitics are gradually excited in subinterval 1 in the 2L-SP configuration, as discussed in Section III. Moreover, the degree of double-pulsing is also lower due to lower damping time, which is visible in Fig. 9(c).

It is worth noting that for both 2L-LF and 2L-SP, the difference between $v_C(t)$ and $v_M(t)$ is minimal. This can be explained by examining the equivalent circuits in Fig. 4 and Fig. 5(b). The values of L and L_s are significantly larger than L_C of the cable. As a result, the voltage drop across L_C is almost negligible, leading to $v_C(t) \approx v_M(t)$.

Further, the maximum values of $v_{M(pk)}$ and $i_{C(pk)}$ over f_O in Fig. 20 for all drive configurations do not appear at the same switching pulse/state. For instance, Fig. 21 shows the zoomed-in comparison of RWP transient in $v_M(t)$ and $i_C(t)$ for all drive configurations at which the maximum $v_{M(pk)}$ value (998 V) for 2L-LF in Fig. 20 is observed. $v_S(t) = v_C(t)$ is the drive output phase A to phase B line-to-line voltage for the 2L case.

The double-pulsing in $v_M(t)$ is evident for all three drive configurations. However, the overvoltage transient for the given switching transition is less severe for 2L-SP, with $v_{M(pk)}$ lower than the observed maximum (642 V). This is because $v_{M(pk)}$, according to (6) and (12), is related to the collective

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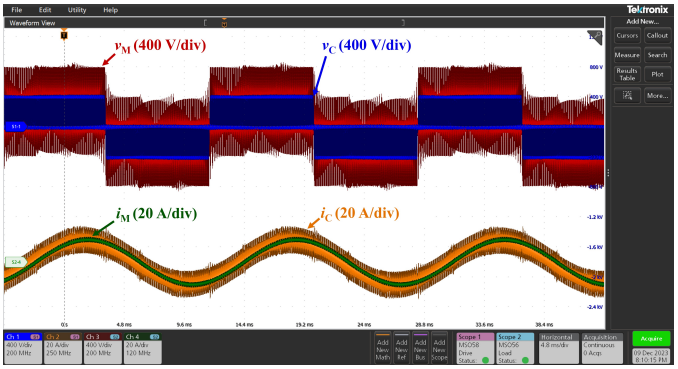
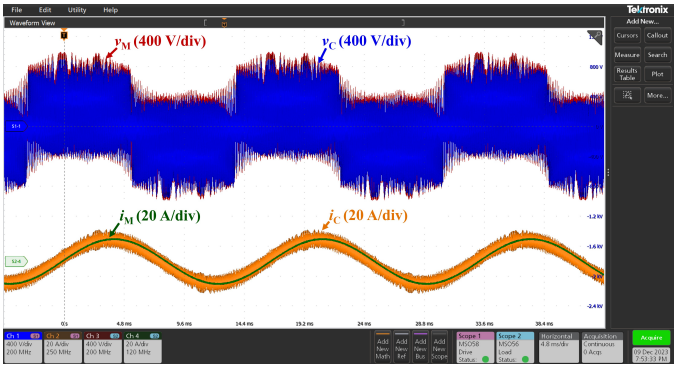
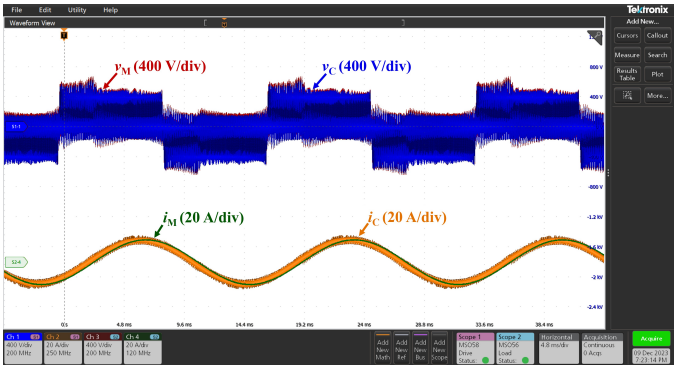


(a)



(b)



(c)

Fig. 20. Continuous test results for the 8 m cable connected to an RL load. (a) 2L. (b) 2L-LF with $L = 5$ µH. (c) 2L-SP with $L_s = 10$ µH.

impact of the variables, having different values for each drive configuration, within the argument vector $\boldsymbol{x}$ (5) and $\boldsymbol{y}$ (11). For the given switching transient, the collective impact of these variables yields the maximum and lower $v_{M(pk)}$ value for 2L-LF and 2L-SP, respectively.

Additionally, the peak i_{Cpk} value in Fig. 21 is the highest for 2L, followed by 2L-LF and 2L-SP, respectively. This trend, similar to $v_{M(pk)}$, for the given transient is also attributed to the collective impact of variables within the argument vector $\boldsymbol{x}$ and $\boldsymbol{y}$, governing (8) and (14).

VIII. 2L-SP Motor Drive Design Considerations and Comparative Review Study

The DPT and continuous test results in Sections IV and VII show that 2L-SP provides enhanced RWP mitigation than 2L and 2L-LF. However, for the design perspective, it is crucial to size L_s optimally to meet motor performance and compliance

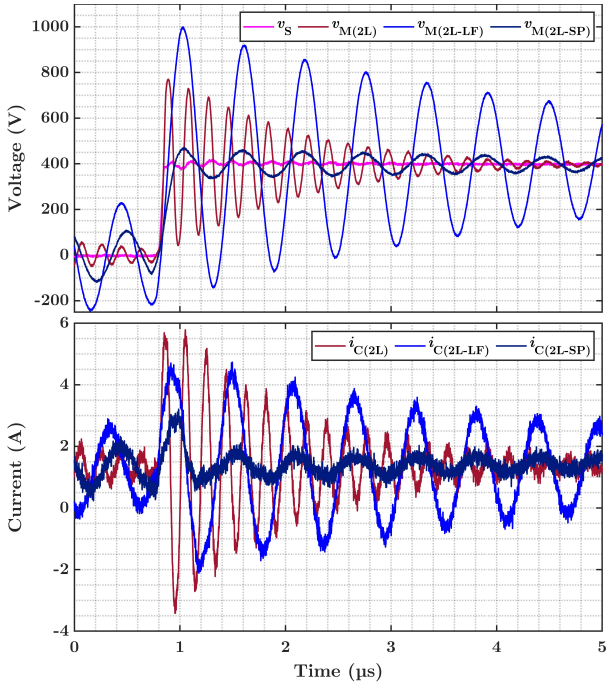


Fig. 21. Zoomed-in comparison of a RWP transient in $v_M(t)$ and $i_C(t)$ in Fig. 20 for all drive configurations.

targets. Further, for practical application it is crucial to review and compare 2L-SP performance and viability with existing approaches that leverages similar structure as 2L-SP but employ auxiliary reactor (2L-LF) or active control techniques to partially or fully mitigate RWP.

A. Split Inductor L_s Sizing

The split inductors in 2L-SP, owing to their location, also act as auxiliary reactors L in 2L-LF. This is evident from the same measured f_{RW} in Fig. 10 and Fig. 11 for both configurations with $L = 0.5L_s$. For 2L-LF, the value of reactor L is motor impedance/power rating dependent. The standard practice is to limit L such that its impedance/reactance at the fundamental frequency f_O is around 3 % or 5 % of the per-phase motor impedance/reactance [43]. The underlying reason is to avoid power factor deterioration and significant voltage drop across the reactor, lowering output torque [53]. Therefore, to prevent severe performance degradation due to an oversized L_s, the same 3 % or 5 % impedance criteria for 2L-LF can also be extended to 2L-SP with $L = 0.5L_s$ to have the same net DM inductance as 2L-LF. Consequently, L_s value in terms of rated phase RMS current I_ϕ and phase voltage V_ϕ, f_O and the % impedance factor Z_F (0.003 or 0.005), can be expressed as

$$L_s = \frac{Z_F V_\phi}{4\pi f_O I_\phi} \tag{15}$$

However, another design constraint on L_s sizing is the current ramp-up/spike Δi_s during the switching transition (subinterval 1 in Fig. 5) which is shown to follow inverse relation with L_s, as analyzed in [32], [33]. In [32], closed from expressions for Δi_s, ignoring the load branch, are provided. The load branch is ignored based on the fact that its impedance is much higher than L_s; otherwise, a significant output voltage

would drop across L_s. Further, this also helps reduce the circuit order to yield closed-form expressions for ease of Δi_s estimation.

Finally, taking into account the % impedance and Δi_s constraints, the general design approach for L_s sizing for 2L-SP-based cable-connected motor drives is to estimate L_s using (15) and use it as a maximum limit for finding the optimal value from the Δi_s versus L_s curve for given drive parameters. The obtained optimal value of L_s can then be used in the proposed DM model in Fig. 5 to estimate $v_{M(pk)}$ beforehand for a given cable and motor, ensuring that $v_{M(pk)}$ is not increased, as seen for short cable lengths in Fig. 11(b).

B. 2L-SP Versus Existing Approaches for RWP Mitigation

The RWP mitigation approaches for 2L motor drives involve using additional passive components as filters and/or semiconductor devices. The 2L-SP, compared with the 2L topology, requires additional split inductors, provided SiC SBD is used to keep the semiconductor count the same. Further, 2L-SP has a similar structure with 2L-LF and existing active control RWP mitigation approaches [24], [25], [54]. Therefore, questions about the advantages and limitations of the 2L-SP and existing approaches arise from a practical application perspective.

Table IV compares 2L-SP with 2L-LF and existing approaches in terms of the number of components, control complexity, and extent of RWP mitigation. The control complexity of 2L-LF and 2L-SP is the same. Moreover, provided that a SiC SBD is utilized for 2L-LF and an inverse coupled inductor is used for 2L-SP [32], the number of components for 2L-LF and 2L-SP are same but RWP mitigation with 2L-SP is higher. In contrast, the active control techniques employ more semiconductor switches per phase with their associated gate drives than 2L-SP and 2L-LF but provide partial to full RWP mitigation at the expense of increased control complexity and cost.

Further, in terms of cable length, 2L-LF, and 2L-SP bring concern of exacerbated overvoltage transients for short cable lengths, which can be analyzed beforehand using the proposed DM equivalent circuit models in Fig. 4 and Fig. 5, respectively. For active techniques, cable length directly impacts the dwell time and needs to be adjusted in the control. According to the theoretical analysis presented in [24], [25], dwell time follows a linear relationship with cable length, lowering the maximum achievable modulation index (maximum fundamental drive output voltage). However, the linear dwell time-cable length relationship is not validated experimentally and might not hold for the case where the antiresonance of the cable is greater than that of the motor, with motor antiresonance dominating the RWP [39]. In this case, the predicted dwell time does not match the actual, and partial RWP mitigation would be achieved [25].

Finally, the choice of RWP mitigation solution for 2L drives entirely depends on the acceptable RWP level and risk for a particular application. For instance, for conservative aircraft applications with drive operation at high altitudes where the Partial Discharge Inception Voltage (PDIV) is lower, the active control RWP mitigation approaches could be more suitable in achieving full RWP mitigation. On the other hand, for industrial applications where the 2L-LF configuration is the first common choice for RWP mitigation upto 300 ft cable length [43], [54], 2L-SP appears to be more viable. This is because the component count, control, and DC bus requirements for 2L-SP are similar to 2L-LF, allowing for a smooth and feasible transition from 2L-LF to 2L-SP within the industry.

TABLE IV
COMPARISON WITH EXISTING TECHNOLOGIES

Parameter	2L-LF	Ref[24]	Ref[25]	2L-SP
RWP mitigation mechanism	Auxiliary reactor	Mid-level dwell-time	Mid-level dwell time	Auxiliary reactor + Lower output dv/dt
RWP mitigation approach	Passive	Active	Active	Passive
RWP mitigation extent	Slight	Partial to full (dependent on dwell time matching)	Partial to full (dependent on dwell time matching)	Partial
Impact of cable length	Possible exacerbation of overvoltage transient for short cable lengths	Dwell time increases and drive output voltage range decreases	Dwell time increases and drive output voltage range decreases	Possible exacerbation of overvoltage transient for short cable lengths (lower than 2L-LF)
Control complexity	Same as 2L	Additional carrier displaced by dwell time required	Time shift equal to dwell time required between paralleled half-bridges + Power imbalance active control	Same as 2L
Number of passive components per phase	1 (inductor)	-	1 (inverse coupled inductor)	1 (inverse coupled inductor) or 2 (discrete inductor)
Number of SiC switching devices per phase	2	4	4	2
Number of SiC anti-parallel diodes per phase	Optional	Optional	Optional	2

IX. Conclusion

RWP is more pronounced in SiC-based 2L motor drives owing to fast switching capability of SiC devices, causing excessive motor side overvoltage and drive side overcurrent. This article explored RWP in a 2L-SP inverter-based motor drive and benchmarked its performance against the closest matching 2L drive with an auxiliary reactor L filter (2L-LF). Compared with simple 2L topology, 2L-SP shows prospects of RWP mitigation owing to its lower output $\mathrm{d}v/\mathrm{d}t$ due to split inductors, which also act as L filter. For modeling RWP, in contrast to transmission-line theory, which qualitatively describes the RWP in terms of reflection coefficient, lumped DM equivalent circuit models are developed for 2L-LF and 2L-SP to model the first antiresonance of the cable and load, the root cause of RWP. The models are coupled with a ramp edge source to represent the drive output, including the switching $\mathrm{d}v/\mathrm{d}t$ of the device.

The RWP is first investigated through DPTs for different cable lengths and inductor values on a 2L-SP/2L-LF configurable SiC-based motor drive prototype. The inductor values for 2L-LF and 2L-SP are chosen to achieve the same net DM impedance. For long cables, overvoltage and overcurrent peaks show a more significant reduction with an increase in inductance for 2L-SP than 2L-LF. The underlying reason is the presence of an intermediate subinterval in 2L-SP, which lowers the output $\mathrm{d}v/\mathrm{d}t$ and consequently the excitation of the cable and load parasitics. In contrast, overcurrent falls inversely with inductance for short cables for both configurations, while overvoltage exhibits an anomalous rising trend. The rising overvoltage trend is analyzed and validated through the proposed DM equivalent circuit models. Hence, these DM circuit models hold practical significance in assessing RWP in 2L-SP and 2L-LF motor drives and determining the impact of inductance on overvoltage beforehand, speeding up the design process.

Additionally, the analysis on short cable also led to an investigation of RWP in the 2L-SP inverter-based integrated motor drive system, where the results show no presence of RWP due to the absence of cable. Moreover, from a switching performance perspective, both 2L-SP and 2L-LF decouple the load parasitics from the device, thereby reducing switching loss. However, split inductors in 2L-SP also decouple the complementary cell's output capacitance from the switching device, further lowering switching loss compared with 2L-LF.

Further, the article also analyzed RWP under continuous operation for both configurations. According to the results, the overvoltage and overcurrent peak varies over the fundamental cycle due to varying load current and double-pulsing. The 2L-LF shows the highest overvoltage owing to severe doubling pulsing due to large oscillation damping time. On the other hand, the 2L-SP configuration has a lower degree of RWP due to lower excitation of the cable and load parasitics, and a reduced level of double-pulsing.

Finally, based on DPT and continuous test results, it can be concluded that 2L-SP is a better candidate than 2L-LF for mitigating RWP, provided that a SiC SBD is utilized to maintain the same semiconductor count. Although 2L-SP requires two inductors per phase-leg compared with one in 2L-LF, this limitation can be overcome using a single inductor with a center tap or an inverse coupled inductor. Additionally, with Medium Voltage (MV) SiC technology evolving and enabling direct use of low-level drive topologies such as 2L, 2L-SP also becomes an attractive option owing to its lower output $\mathrm{d}v/\mathrm{d}t$, superior switching performance, cross-talk immunity and enhanced RWP mitigation.

As part of future work, the authors' focus is on analyzing the impact of each variable in the expressions for peak overvoltage and overcurrent through sensitivity analysis to identify the dominant variables impacting RWP transients. Furthermore, from the magnetics perspective, the authors plan to investigate and compare inductor losses (core and copper) in 2L-LF and 2L-SP for different modulation strategies. The findings of these works will be shared in future publications.

Acknowledgments

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Appendix A
Derivation of $v_{\mathrm{M}}(t)$ and $i_{\mathrm{C}}(t)$ for 2L-SP

The circuit for subinterval 2 in Fig. 5(b) is identical to the equivalent circuit for 2L-LF (Fig. 4) with $1.5L$ replaced with $0.75L_{\mathrm{s}}$ and ramp edge $v_{\mathrm{S}}(t)$ replaced with constant V_{DC}. Therefore, the expressions for characteristic function and complex poles ω_{RW} and ω_{P2}, derived for the 2L-LF in [35], are applicable to the subinterval 2 with L replaced with $0.5L_{\mathrm{s}}$.

The underlying characteristic function is expressed as follows

$$k_2 s^4 + k_1 s^2 + k_0 = 0 \tag{16}$$

The coefficients k_2, k_1, and k_0 are given by

$$k_2 = (0.75L_{\mathrm{s}} + L_{\mathrm{C}})L_{\mathrm{M}}L_{\mathrm{MS}}C_{\mathrm{C}}C_{\mathrm{MS}}$$

$$\begin{aligned} k_1 =& L_{\mathrm{M}}(0.75L_{\mathrm{s}} + L_{\mathrm{C}})(C_{\mathrm{C}} + C_{\mathrm{MS}}) \\ &+ L_{\mathrm{MS}}C_{\mathrm{MS}}((0.75L_{\mathrm{s}} + L_{\mathrm{C}}) + L_{\mathrm{M}}) \end{aligned}$$

$$k_0 = 0.75L_{\mathrm{s}} + L_{\mathrm{C}} + L_{\mathrm{M}}$$

The roots of the characteristic function are given by

$$s_1, s_2 = \pm\sqrt{\frac{\frac{\sqrt{k_1^2 - 4k_2k_0} - k_1}{k_2}}{2}} \tag{17}$$

$$s_3, s_4 = \pm\sqrt{\frac{-\frac{\sqrt{k_1^2 - 4k_2k_0} + k_1}{k_2}}{2}} \tag{18}$$

The response of the equivalent circuit is oscillatory, implying complex roots/poles ($s_1 = s_2^*$ and $s_3 = s_4^*$). Further, as there is no damping term in the system ($s = j\omega$), the magnitude of the complex roots are the angular frequencies $\omega_{\text{P1}} = \omega_{\text{RW}}$ and ω_{P2} with $\omega_{\text{P1}} < \omega_{\text{P2}}$ and $\omega_{\text{P1}} = \omega_{\text{RW}}$ being the dominant pole.

$$\omega_{\text{P1}} = \omega_{\text{RW}} = |s_1| = |s_2| \tag{19}$$

$$\omega_{\text{P2}} = |s_3| = |s_4| \tag{20}$$

The roots of the characteristic function serve as the basis for solving the equivalent circuit for subinterval 2 to obtain expressions for $v_{\text{M}}(t)$ and $i_{\text{C}}(t)$, respectively.

A. $v_{\text{M}}(t)$

Contrary to the ramp edge $v_{\text{S}}(t)$ in Fig. 4, the excitation source for the subinterval 2 is constant V_{DC}. The expression for $v_{\text{M}}(t)$ in s-domain, for the constant V_{DC} excitation, can be derived using the node voltage analysis as follows

$$v_{\text{M}}(s) = \frac{w_3 s^3 + w_2 s^2 + w_1 s + w_0}{(s+i\omega_{\text{RW}})(s-i\omega_{\text{RW}})(s+i\omega_{\text{P2}})(s-i\omega_{\text{P2}})} \tag{21}$$

The coefficients w_3, w_2, w_1, and w_0 are given by

$$w_3 = v_{\text{M}}(T_{\text{Z}}^-) - \frac{L_{\text{M}} V_{\text{DC}}}{0.75L_{\text{s}} + L_{\text{C}} + L_{\text{M}}}$$

$$w_2 = \frac{i_{\text{C}}(T_{\text{Z}}^-) - iL_{\text{M}}(T_{\text{Z}}^-) - iL_{\text{MS}}(T_{\text{Z}}^-)}{C_{\text{C}}}$$

$$w_1 = \frac{L_{\text{M}}(v_{\text{MS}}(T_{\text{Z}}^-) - V_{\text{DC}}) + (0.75L_{\text{s}} + L_{\text{C}})v_{\text{MS}}(T_{\text{Z}}^-)}{L_{\text{MS}}C_{\text{C}}(0.75L_{\text{s}} + L_{\text{C}} + L_{\text{M}})} + \frac{v_{\text{M}}(T_{\text{Z}}^-)(0.75L_{\text{s}} + L_{\text{C}} + L_{\text{M}}) - L_{\text{M}}V_{\text{DC}}}{L_{\text{MS}}C_{\text{MS}}(0.75L_{\text{s}} + L_{\text{C}} + L_{\text{M}})}$$

$$w_0 = \frac{i_{\text{C}}(T_{\text{Z}}^-) - iL_{\text{M}}(T_{\text{Z}}^-)}{L_{\text{MS}}C_{\text{MS}}C_{\text{C}}}$$

The time-domain expression is obtained by taking the inverse Laplace transform of (21) and is given by (9). $v_{\text{AC}}(t)$ in (9), likewise for 2L-LF, is the sum of sinusoids expressed as

$$v_{\text{AC}}(t) = m(\boldsymbol{y})\sin(\omega_{\text{RW}}t) + n(\boldsymbol{y})\cos(\omega_{\text{RW}}t) \tag{22}$$

$\boldsymbol{y}$ represents the set of variables in (11). Further, the amplitude of the sinusoidal terms $m(\boldsymbol{y})$ and $n(\boldsymbol{y})$ are related to w_3, w_2, w_1 and w_0 and angular frequencies ω_{RW} and ω_{P2} as

$$m(\boldsymbol{y}) = \frac{w_0 - w_2\omega_{\text{RW}}^2}{\omega_{\text{RW}}(\omega_{\text{P2}}^2 - \omega_{\text{RW}}^2)} \tag{23}$$

$$n(\boldsymbol{y}) = \frac{w_1 - w_3\omega_{\text{RW}}^2}{(\omega_{\text{P2}}^2 - \omega_{\text{RW}}^2)} \tag{24}$$

Finally, $v_{\text{M(pk)}}$ can be expressed (12) as the sum of the steady-state DC value and the maximum value of $v_{\text{AC}}(t)$.

B. $i_{\text{C}}(t)$

The current $i_{\text{C}}(t)$ is the integral of the voltage $(v_{\text{S}}(t) - v_{\text{M}}(t))$ across $0.75L + L_{\text{C}}$ (13). The peak value $i_{\text{C(pk)}}$, given by (14), is mainly dependent on the maximum value of the integral of $max\{v_{\text{AC}}(t)\}$ (10).

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