An Integrated TMR-Based Current Sensing Solution for WBG Power Modules and Converters

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***Abstract*— This article proposes a contactless and high-precision current measurement solution using tunneling magnetoresistance (TMR) sensors to address the challenges of current measurement in wide bandgap (WBG) power electronics with high *dv/dt*, *di/dt* and switching frequencies. The solution, referred to as two TMR sensor (TTS), utilizes TTSs placed on opposite sides of the current-carrying trace, which can be printed circuit board (PCB) or bus bar-based. At first, the derivation and working principle of the TTS technique is presented, followed by its design and validation on an in-house developed SiC-based power module and power converter. A slitted PCB terminal design with minimum parasitic capacitance is proposed for the power module to alleviate skin effects and simplify sensor placement. The slitted terminal design is tested at 50 A and 70 kHz square wave pulse. Similarly, for the power converter, a bus bar-based TTS design is developed and compared with the existing shunt-based current measurement in continuous testing at 500 V and 3.5 kW. The TTS solution outperforms the shunt measurement with high SNR and bandwidth.**

***Index Terms*— Capacitive coupling, current sensing, differential output, power converters, power modules, signal-to-noise ratio, skin effect, slitted design, tunneling magnetoresistance (TMR), wide bandgap (WBG).**

I. Introduction

With the advent of next-generation power semiconductor devices based on wide bandgap (WBG) technology, the switching frequency of the power electronic converters is moving into the megahertz range to guarantee higher power density through decreasing size of passive components and high power efficiency due to fast switching capability and low on-resistance of WBG devices [1]. In order to keep up with the fast improvements in high-frequency power electronics, influential developments are needed on the other essential elements of the power converters, like controllers, sensors, and thermal management.

Current state variable is a critical parameter in a power electronic converter, which is used for various purposes such as closed-loop control, short circuit and over current protection [2], [3], [4], diagnostics/prognostics [5], and life prediction through health monitoring using techniques such as digital twin (DT) [6]. However, traditional current sensing strategies are not feasible for measuring current in modern power converters as they require considerably high bandwidth and accuracy while holding a small footprint. Therefore, it is essential to research various high-bandwidth current sensing solutions for measuring the current in the modern power electronic systems [7].

Power converters can be divided into two main groups: power converters based on power modules or based on discrete devices, each with pros and cons and challenges in developing advanced current sensing approaches.

Power modules provide various benefits, such as housing multiple components like switching devices, such as transistors and diodes, and usually, thermal management and cooling parts in a single package [8]. Therefore, using power modules for developing power converters can simplify the design. However, power modules are not available for all required configurations and ratings. Furthermore, they are costly with proprietary designs.

On the other hand, using discrete devices provides more freedom in choosing the switching devices and configurations based on the application's requirements. However, this privilege comes at the cost of more complexity and challenges accompanied by thermal management solutions.

Therefore, based on the limits and requirements of the application, power converters can be designed with discrete devices or power modules. It should be mentioned that, in either case, the necessity of measuring the current holds the same, and each of these approaches poses various challenges when implementing high-frequency current measurement solutions.

The current measurement approach compatible with the high power density and high-efficiency power converters must have different features such as the following.

1) *Wide current measurement bandwidth:* Capturing acceptable switching details of a WBG device demands its accompanying current sensor to have a wide bandwidth, ideally from dc to the megahertz or gigahertz range [9].
2) *Wide current range:* The current measurement solution should be able to handle high currents, primarily based on the requirements of the application, if it may be subjected to transient currents and spikes [4].
3) *Noninvasive integration with no or minimum stray inductance addition and design change:* Stray inductance can generate voltage over/undershoots when

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switching WBG devices. Therefore, it is critical that the current measurement adds as negligible as possible inductance to the current path. Also, it is preferred that the addition of the current measurement solution does not change the design of the power module or add more complexity [10], [11].

4) *Small dimension:* To achieve high power density, the size of the power converter needs to be small. Therefore, the selected measurement solution should also be small to make integration feasible yet have high reliability and precision [12].
5) *High noise immunity:* Due to a harsh dv/dt environment driven by the fast switching of devices, common-mode (CM) noise-related concerns may appear, mainly since growing power density necessitates components to be placed near each other, which exacerbates electromagnetic interference problems, leading to errors in the current measurement. Therefore, selecting a measurement solution immune to noise or applying techniques to acquire this feature is essential [11], [13], [14], [15].
6) *Lower cost:* Developing converters with lower cost is one of the main goals in all applications. This aim highlights the need for applying current measurement solutions with low cost but prominent in other features [16].
7) *Wide temperature range:* Fast switching of devices can lead to higher temperatures, especially inside the power modules. Therefore, the selected current measurement solution should have stability and acceptably low drift over a wide temperature range [17], [18].

This article is organized as follows. Section II reviews different current sensing technologies for WBG-based converters and the merits and drawbacks of each solution. Section III presents the proposed TTS current sensing solution based on TMR sensors. This is followed by Section IV, where a case study of implementing the TTS solution into an in-house developed power module is discussed. Several layouts, aiming to lower parasitic capacitance and simplify sensor placement, are evaluated through simulation and hardware tests. This section is followed by Section IV, where the TTS solution is extended to the inductor current measurement of the dc–dc stage of an in-house developed 75 kVA SiC-based power converter. Test results are presented to validate the performance of the proposed solution, which underscores its performance and efficacy. Lastly, Section VI concisely summarizes the article's key findings.

II. Review of Current Sensing Technologies for WBG-Based Converters

Several current measurement sensor classes are commercially available in various current ratings. These sensors are categorized into two main classes [19]: 1) sensors that measure voltage drop as a proxy for current, non-magnetic methods and 2) sensors that measure magnetic field as a representative of the current in a conductor, magnetic methods. These type of sensors uses one of a variety of magnetic sensing techniques.

The shunt resistor is the most straightforward current sensor from non-magnetic methods and does not depend on magnetic field measurement.

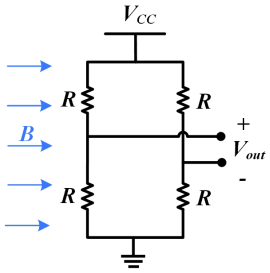


Fig. 1. Structure of an MR current sensor.

On the other hand, magnetic methods include various approaches such as current transformer, Hall effect current sensor, Rogowski coil current sensor, and magnetoresistor (MR) current sensor. Table I summarizes the features of each measurement solution.

As it can be observed from Table I, considering bandwidth, integration difficulty, accuracy and limits, MR sensors are the most compatible options to be used for integrated current measurement. However, their drawbacks, noise immunity and temperature drift, should be alleviated for integrated current sensing.

MR sensors work by the linear variation of resistance of MR caused by the magnetic field generated by the current to be measured. In the configuration of MR sensors, resistors are configured as a Wheatstone bridge to enhance the linearity of the sensor and compensate for thermal drift. As exhibited in Fig. 1, the V_{out} is proportional to the magnetic flux density and the current. MR sensors have different types, but all have the same measuring principle. The different sensors are known as anisotropic magnetoresistive (AMR), giant magnetoresistive (GMR), and tunnel magnetoresistive (TMR) [20], [21]. The only difference between the three groups is the selected magnetoresistors.

AMR only includes a single layer of ferromagnetic materials. The resistance variation of AMR magnetoresistors is about 2%–4% as the magnetization in the layer turns from parallel to perpendicular to the current direction. The minor resistance deviation ratio means low SNR, the AMR's main weakness [20], [22].

GMR is introduced to enhance the resistance change ratio. The fundamental phenomenon of GMR consequences is the current flowing through two magnetic elements separated by a thin, non-magnetic spacer layer, which enhances the resistance change of the GMR to 12%–20% [20], [22].

The later-developed MR sensor, TMR, can further enhance the resistance change ratio. Table II compares the characteristics of magnetic sensors using AMR, GMR, and TMR elements from TDK [23]. TMR has the highest resistance variation percentage, which leads to the highest SNR [29]. Moreover, TMR has the lowest temperature drift, which is essential when used to measure the current inside the power modules since the temperature inside a power module can alter considerably for different loads.

Therefore, based on the promising features of TMR sensors in high-frequency current measurement, they are the best options to be used for high-frequency current measurements solution. In this article, a solution for increasing the SNR and

TABLE I

COMPARISON OF EXISTING CURRENT SENSING TECHNOLOGIES [19], [21], [24]

Sensing Solution	Bandwidth	System Integration	Accuracy	Limits
Shunt	MHz	Low	Medium	Bulky, addition of power loss and parasitic inductance
Current Transformer	MHz	High	High	Bulky and unable to measure DC current
Hall effect sensor	kHz	High	High	Low bandwidth and noise immunity and temperature drift
Rogowski coil	MHz	Low	Medium	Unable to measure DC current
MR sensor	MHz	Low	High	Noise immunity and temperature drift

TABLE II

CHARACTERISTIC COMPARISON OF TDK MAGNETIC SENSOR [23]

Parameter	AMR	GMR	TMR
MR Ratio	3	12	100
Output (mV)	150	500	3300
Temperature Dependency (%/°C)	-0.29	-0.23	-0.13

alleviating the limitations of MR sensors, which are noise immunity and temperature drift, is proposed. The presented method can be applied on any type of MR sensors.

III. TWO TMR SENSING SOLUTION

To enhance the accuracy of current measurement and mitigate noise-induced errors, TTS method with a novel configuration is proposed. Considering the importance of the integrated current measurement in power modules and discrete device level power converters, implementation of the proposed approach for both classes is applicable.

The concept of using two sensors to augment sensitivity and counter temperature drift for MR technology has been proposed in [25] and [26]. Although, the same approach can be extended to the TMR technology, the sensor layout adopted in these works exhibits performance limitation for WBG-based power modules and power converter. For instance, [25] proposes a U-shaped design with sensor placed on the two legs of the trace in parallel. In this way, the magnetic field in the interior of the U-shaped structure is maximized, thereby increasing the sensitivity of the sensor. However, the U-shaped structure potentially forms a loop antenna (H-field). Since, WBG devices are capable of switching at high frequencies, the U-shaped loop can become an effective antenna and interfere with other critical control and power circuitries nearby. Similarly, the loop is also susceptible to the external H-fields, thereby corrupting the signal output. Lastly, the foot print of the layout is also large, making it infeasible for integration on the terminal or inside the power module.

Moreover, a TMR-based two sensor solution for Si IGBT power module is presented in [26]. The design provides a reaction time of 530 ns. However, the signal conditioning structure, developed in this research, is not differential and is highly prone to noise. Further, the sensors are placed relatively far from each other, leading the sensors to be exposed to different temperatures and noisy environments. Therefore, using the differential method will not be beneficial to provide a clean reading from the measurement system. Besides this, the validation of the proposed solution is only done at 1 kHz, which is substantially less than the nominal switching frequency of WBG devices.

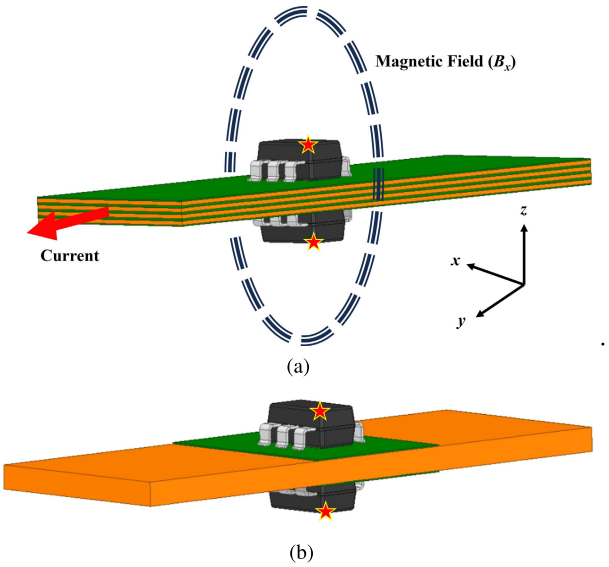


Fig. 2. TTS method implementation for (a) PCB-based terminal and (b) copper terminal.

The proposed TTS method overcomes the limitation of the structures in the above-mentioned literature by placing the two sensors parallelly with the conductor/printed circuit board (PCB) sandwiched between them. Fig. 2 shows the implementation of the TTS method for PCB-based terminal and copper terminal, respectively, which can be used for power module or power converters. The central copper trace, in between sensors, generates a magnetic field, which is sensed by two identical current sensors positioned in opposite directions. These sensors yield output signals denoted as V_{S1} and V_{S2}, respectively. Because of the arrangement of the sensors, V_{S1} is equal to the negative of V_{S2}. Further, as the sensors are in proximity, they are exposed to the same temperature and interference from external fields. Therefore, V_{S1} and V_{S2} can be modeled as

$$V_{S1} = S_1 \cdot B_1 + \Delta V_1 + K_1 \cdot \Delta T_1 \quad (1)$$

$$V_{S2} = S_2 \cdot B_2 + \Delta V_2 + K_2 \cdot \Delta T_2 \quad (2)$$

where S_1 and S_2 are the sensitivities of the TMR sensors in V/mT, ΔV_1 and ΔV_2 are the errors of the output voltage due to external fields, B_1 and B_2 are the magnetic fields the sensors are exposed to, and K_1 and K_2 are the sensitivities of the sensors due to temperature variation, representing the errors in output voltage generated from temperature fluctuations. The difference of V_{S1} and V_{S2}, $\Delta V_S = V_{S1} - V_{S2}$ can be written as

$$\Delta V_S = (S_1 B_1) - (S_2 B_2) + (K_1 \Delta T_1) - (K_2 \Delta T_2). \quad (3)$$

TABLE III
CROCUS TMR CURRENT SENSOR SPECIFICATIONS [27]

Parameter	Value
Part Number	CT100
Operation Magnetic Filed Range	±50 mT
Bandwidth	DC- 1MHz
Non- Linearity	0.5% from -20 mT to +20 mT
Hysteresis	0.05%
Operation Temperature	-40 to 150 °C

Considering the specific arrangement of sensors, $V_{S1} = -V_{S2}$ and $B_1 = -B_2$. Moreover, placing sensors on two sides of the terminal grantees, they are exposed to similar temperatures, which means $\Delta T_1 = \Delta T_2$. Therefore, (3) can be simplified as

$$\Delta V_S = 2S_1 \cdot B_1. \tag{4}$$

Therefore, the noise cancellation effect is maximized by strategically locating the sensors in similar positions to experience comparable magnetic fields and noise. Besides, rather than increasing the resolution or sensitivity of the current measurement system, TTS reduces the impact of temperature fluctuations on sensor performance, as errors induced by temperature sensitivity are also mitigated in the current measurement system output.

The proposed TTS technique can be extended to both WBG-based power modules and converters. The following sections present the case studies of implementing the proposed TTS method for both applications. The sensor used for both studies is CT100 from Crocus [27]. CT100, similar to the other MR sensors, generates linear output voltage with a changing magnetic field (in the magnetic field in the range of ± 50 mT). The characteristics of the sensor is summarized in Table III.

IV. TTS SOLUTION FOR A DOUBLE-SIDED COOLED SIC POWER MODULE

For validation the proposed TTS concept for the power module, a case study of a double-sided cooled SiC power module, developed in [28], is considered. The first step in designing the TTS solution is to decide the placement of the sensor. The TTS solution can either be embedded inside the module on the direct bonded copper (DBC) or on the ac output terminal. Considering the complicated magnetic and electric fields generated by high di/dt and dv/dt transients of SiC switching devices and the small area inside the power module, placing the sensors on the DBC board can cause errors due to coupling and interference [29], [30].

Moreover, a general solution that can implemented on any power module design without changing the layout of the module is more favorable. Therefore, the most suitable option is to place sensors on two sides of the ac terminal of the power module. In this location, both sensors will be exposed to similar external magnetic fields and temperature variations. Hence, the differential current measurement solution, TTS, can cancel noise and temperature variation errors. Fig. 3(a) presents a conceptual drawing for the power module with the proposed TTS solution, attached to the output ac terminal. The power module is built on split-output configuration and has two ac terminals which are shorted to form a simple half-bridge configuration with a single ac output terminal.

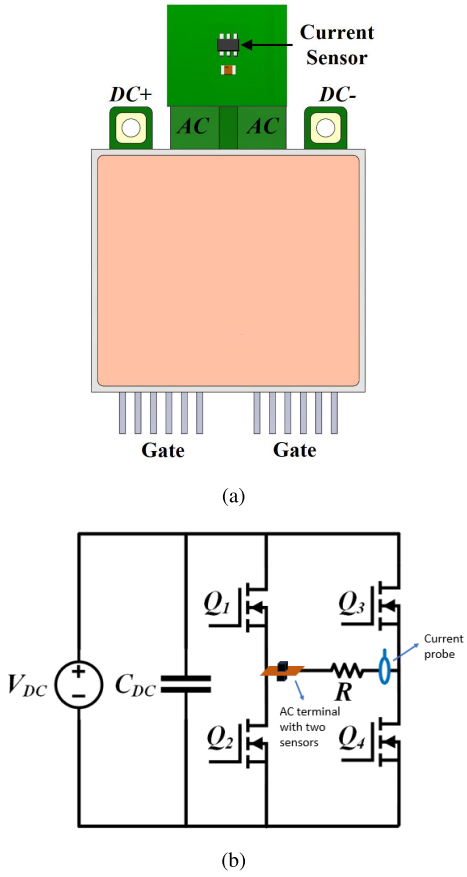


Fig. 3. (a) Conceptual drawing of a power module in [28] with TTS on ac terminal. (b) Test circuit schematic.

As stated earlier, the proposed TTS method is a general method for any configuration of power module or converter. Therefore, to ensure that the solution is applicable for both unipolar and bipolar currents, bidirectional TMR sensors are selected (Table III) for the study. For testing the sensor, a full-bridge testbed is developed. The test schematic is depicted in Fig. 3(b) and comprises a full bridge formed by coupling the power module (half-bridge) to another off-the-shelf half-bridge evaluation board KIT-CRD-8FF90P from Wolfspeed. The gate drivers for the module and evaluation board are driven by Texas Instrument F28379D DSP. Further, the sensors are supplied from an isolated 5-V power supply. The output voltage of the sensors is measured using Tektronix TDP1500 differential probe. Fig. 4 shows the test setup to verify the TTS method.

For the test current, a square pulse (resistive load) is chosen over the triangular waveform (inductive load). The literature predominantly employs the triangular waveform for testing sensors [26], [31]. However, the di/dt of a triangular waveform is considerably less than that of a square pulse and there is no constant dc (B field) interval. As WBG devices can handle high di/dt, it is also imperative to test and benchmark the sensor's performance with test current having high di/dt transients. The square pulse provides both fast rising and falling di/dt transients and constant dc interval and is, therefore, more realistic than a triangular waveform.

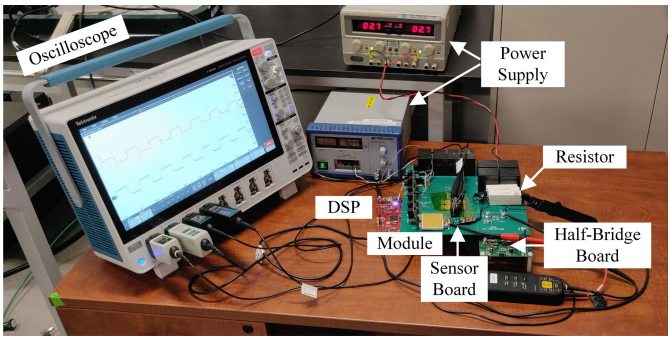
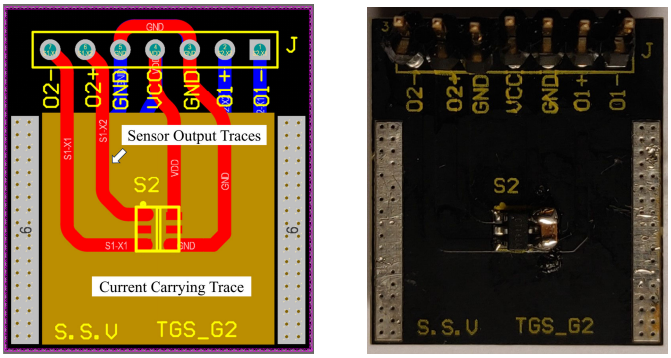


Fig. 4. Experimental setup for schematic in Fig. 3(b).



(a) (b)

Fig. 5. Design I for TTS validation (top view). (a) PCB layout. (b) Prototype.

The accurate TTS current measurement system is achieved systematically by improving the layout in four stages (Designs I–IV). Each design stage targets and improves various issues accompanied by high-frequency current measurement.

A. Design I

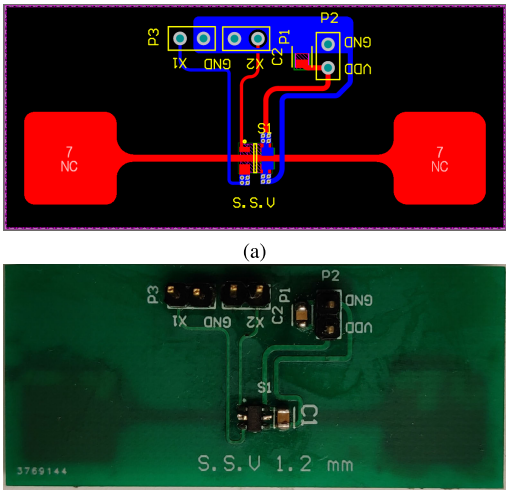
The first design consists of full wide current-carrying PCB trace with dimensions kept the same as that of the ac output terminal of the in-house designed power module. The two sensors (CT100) are placed on both sides of the PCB [Fig. 5(a)]. The main current-carrying trace comprises four PCB layers, each 6 oz thick to meet the current-carrying requirement. The sensor supply and output traces are routed on extra layers on both sides and brought out at one corner.

Fig. 6 illustrates the output of a single sensor from the TTS method and the current probe (Tektronix TCP0030A) for 50 A peak-to-peak 70 kHz current pulses. This test evaluates each sensor's performance and impact on the TTS system. While the current measured by the current probe shows some deviations from a perfect square-wave shape due to parasitic inductance, the current sensor output displays a similar waveform corrupted with spikes at the switching transition intervals. These spikes are caused by capacitive coupling between the main current-carrying trace and the sensor output traces [32]. The high dv/dt producing during the switching transient causes noise to couple to the sensor output.

B. Design II

To solely analyze and troubleshoot the impact of capacitive coupling in Design I, a PCB terminal with a thinned current trace strategically passing underneath the sensor is developed, as depicted in Fig. 7. This modification reduces the coupling between the main current-carrying trace and the sensor output trace, as there is minimum overlap between the main current-carrying trace and the sensor supply and output traces.

Fig. 6. Design I test results for 50 A peak-to-peak 70 kHz current pulses.



(a)

(b)

Fig. 7. Design II for investigating the impact of capacitive coupling. (a) PCB layout. (b) Developed prototype.

The developed prototype is tested with a current pulse of 70 kHz and 30 A peak and the test results are presented in Fig. 8. As can be observed from the test results, thinning the current-carrying trace reduces the coupling between the main trace and sensor pads. However, thinning the trace brings concerns about the heating of the trace and, hence is not a feasible solution. A slitted current-carrying trace is then designed to address this concern.

C. Design III

Although Design II provides better results, but the limited current-carrying capacity overshadows its effectiveness. This limitation can be addressed by slitting Design I in the center to create a thin trace and place a sensor on this thin trace in the center of the terminal. The proposed concept PCB layout is illustrated in Fig 9. The current-carrying trace is divided into three sections, and the sensor is placed in the middle part.

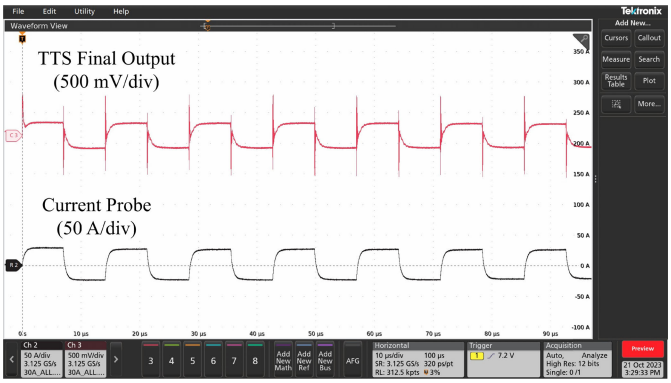
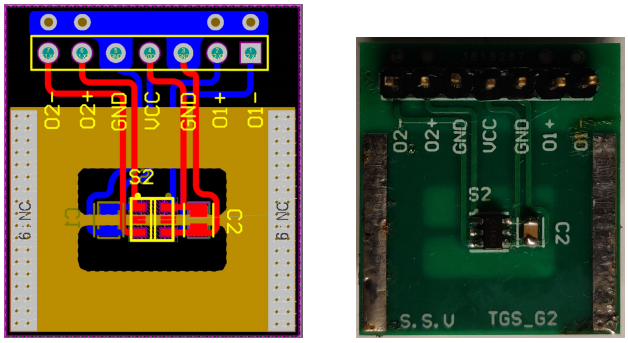


Fig. 8. Design II test results for 30 A 70 kHz current pulses.



(a) (b)

Fig. 9. Design III, slitted current trace for alleviating capacitive coupling issue and enabling high current-carrying capability. (a) PCB layout. (b) Developed prototype (top view).

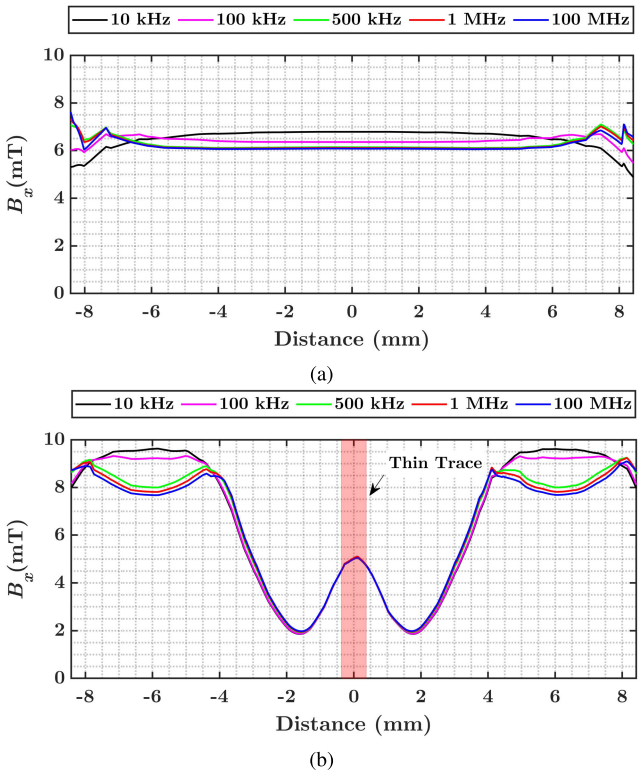


Fig. 10. Simulation results for B_x field component. (a) Design I. (b) Design III.

The thin trace carries a portion of the primary current, which will be sensed by the sensors above the trace on the two sides of the board. By slitting the main current-carrying trace, this design approach not only helps decrease coupling with the thin trace beneath the sensor but it also provides freedom in selecting current sensors with low B-field sense ratings, even for high current applications.

Another approach to implementing a slitted current trace involves dividing the current-carrying trace into two sections: a thin sensing trace and a thick side trace. However, in this configuration, the proximity effect causes the maximum magnetic field to shift toward one side. Consequently, this phenomenon disrupts the sensor's exposure to the maximum magnetic field when placed in the middle of the thin trace, thereby compromising its performance. Thus, opting for a design with the thin trace positioned in the middle and two thick traces on the sides emerges as the optimal solution.

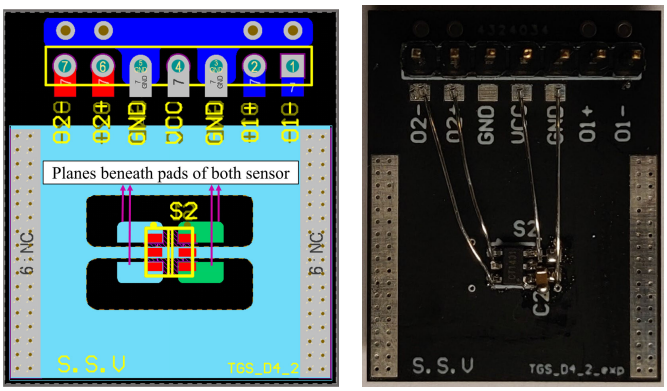
Further, the thin-slitted trace also provides the benefit of having uniform magnetic field distribution over a wide frequency range. For a wide full trace (Design I), one challenge is the concentration of the magnetic field around the corner due to the skin effect at high frequencies. Consequently, if the sensor is placed in the middle, its sensitivity to detecting high-frequency current decreases. Hence, optimal sensor placement is required, which is mainly performed using finite-element analysis (FEA) [26], [31]. However, the slitted trace is thin enough such that the variation in magnetic field with frequency is little due to the lower cross section area of the thin trace. To validate this, a simulation is performed in ANSYS Maxwell using eddy current solver to determine and compare the magnetic field component along the x-axis B_x (sensing axis of CT100 in Fig. 2) for 50 A current for various frequencies for Design I and Design III PCB layouts. The results are summarized in Fig. 10.

As evident from the simulation results in Fig. 10, the concentration of magnetic field density along the corners increases with frequency for Design I due to the skin effect [33]. This phenomenon, owing to the skin effect, causes error in sensor reading for high-frequency content and the underlying sensor output signal does not truly represent the frequency spectrum of the excitation current. This limitation is addressed in the thin-slitted trace design [Fig. 10(b)], where the magnetic field around the thin trace (highlighted region) stays constant over the wide frequency range (10 kHz–100 MHz), minimizing the impact of skin effect. Hence, the sensor placement on the thin trace for Design III is always optimal.

An one approach to substituting the design involves splitting the current-carrying terminal into two thick traces on both sides, with one side featuring a thicker trace and the thin sensing trace positioned on the other. However, in such a configuration, the proximity effect causes the maximum magnetic field to shift toward one side. Consequently, this phenomenon disrupts the sensor's exposure to the maximum magnetic field when situated in the middle of the thin trace, thereby compromising its performance. Thus, opting for a design with the thin trace positioned in the middle and two thick traces on the sides emerges as the optimal solution.

The developed prototype in Fig. 9 is tested using the experimental setup in Fig. 4. The tests results for 70 kHz,

Fig. 11. Design III test results for 50 A peak-to-peak 70 kHz current pulses.



(a) (b)

Fig. 12. Design IV. (a) PCB layout. (b) Developed prototype (top view).

Fig. 13. Design IV test results for 50 A peak-to-peak 70 kHz current pulses.

50 A are presented in Fig. 11. Compared with Design I, the final sensor output is cleaner and captures the pulse waveform shape. However, voltage spikes due to capacitive coupling appear at the switching transition [26]. The root cause of these spikes is the parasitic capacitance between the main trace and the sensor pins/pad and sensor output traces routed to the connection header over the main trace. This conclusion serves as the motivation for developing Design IV with lower parasitic capacitance.

D. Design IV

The traces connecting the sensor output to the connection header in Design III are capacitively coupled to the main-slitted current-carrying trace, leading to voltage spikes during the switching transient. To lower the coupling, these connections must be brought out to the header with sufficient separation between the main and the sensor output traces. For this purpose, wire bonding the connection between the sensor output pad and the traces is feasible. Further, another source of parasitic capacitance is the coupling between the sensor pads and the main current-carrying trace, which can reduced by adding shield pads beneath the pads of the sensor. These modifications constitute Design IV.

Further, to investigate the impact of proposed modifications on coupling effect and accuracy of current measurement, parasitic extraction is performed using ANSYS Q3D to estimate the capacitance between the pads and the main trace. Table IV summarizes the results. Placing shields beneath the sensor pads helps decrease the capacitance in Design III. However, eliminating the sensor output traces over the main current-carrying trace has a prominent influence on capacitance reduction (99.12%). Based on the limits of the application, the sensor traces can be routed externally through wire bonding.

The developed prototype for Design IV is depicted in Fig. 12. The sensor pads are connected to the headers using a 12-mil thick wire bond with a height of 1.5 mm above the PCB surface. For practical application, the wire bonds can be encapsulated to protect them against getting detached or displaced. The prototype is tested on the setup in Fig. 4 with the same 70 kHz, 50 A current pulse. The test results are presented in Fig. 13. Compared with Design III, the extent of voltage spikes is reduced considerably, justifying the efficacy of the proposed TTS solution.

Despite using the wire bonds, small spikes still appear during the switching transition. The cause of these spikes is the intrinsic capacitive coupling between the sensor package (SOT-26) pins and the current-carrying trace, which is uncontrollable. The extent of these spikes can be reduced by using a low-pass filter [34]. The low-pass filter needs to be designed to achieve adequate bandwidth and fast response time.

Further, although wire bonds proved effective in lowering the capacitive coupling between the main trace and the sensor output traces, a concern related to distortion in the measurement due to the wire bonds' parasitic inductance arises. Nevertheless, it is worth noting that the wire bonds serve as replacements for traces on the PCB in prior Designs I, II, and III. The traces on the PCB also introduce parasitic inductance similar to wire bonds. Moreover, the output of each TMR sensor is differential (two signal outputs $V_{\text{out}+}$ and $V_{\text{out}-}$ with respect to the ground). In a differential configuration with the same length of both signal lines, the impact of parasitics is suppressed as both lines have the same distortion or noise, which is eliminated in the differential measurement [35]. The length of wire bonds for each sensor output pair ($V_{\text{out}+}$ and $V_{\text{out}-}$) is kept the same in the developed prototype for Design IV (Fig. 12). As a result, the noise or distortion due to wire bond parasitics is the same in both lines for each TMR sensor and is canceled.

Lastly, a two-stage signal conditioning circuitry can be used to amplify the output of sensors and their difference to

TABLE IV
ESTIMATED PARASITIC CAPACITANCE USING ANSYS Q3D

Design Case	Parasitic Capacitance (pF)
Design II	3.44
Design III with pad shielding	3.33
Design III with pad shielding and externally routed traces (Design IV)	0.03

make it compatible with commercially available ADC having 3.3 or 5 V reference. The schematic and design of the signal conditioning circuitry is discussed in Section V focusing on the TTS application in a 75-kVA SiC-based power converter.

E. Design Considerations for Slitted Current Trace

The slitted current trace needs to be designed properly to prevent saturation of the TMR sensor due to current I_s flowing through the thin trace. Theoretically, I_s, assuming uniform cross section of the PCB layer, depends on the width of the trace w_s and the width of the thicker trace w_c on each side. The widths ws and wc are in millimeters. The expression for I_s, based on current division rule, can be written as

$$I_s = \frac{w_s}{w_s + 2w_c} I. \tag{5}$$

I represents the total current flowing out of the ac terminal of the module. After computing the value of I_s, the next step is to estimate the magnetic field density across the sensing trace. Considering the magnetic axis orientation of Fig. 2, the relevant magnetic field component is along the x-axis B_x. B_x in mT can be calculated using (6), derived from the Biot–Savart law in [36]. h, in millimeter, represents the vertical distance of the sensor above the sensing trace

$$B_x = 4\left[\frac{I_s}{w_s}\tan^{-1}\left(\frac{w_s}{2h}\right)\right]10^{-1}(\text{mT}). \tag{6}$$

In the linear range, the output voltage V_S of each sensor in millivolt is related to B_x as

$$V_S = SB_x. \tag{7}$$

S is the sensitivity of the sensor in mV/V/mT, specified in the datasheet for a specific supply voltage [27]. Combining (5)–(7), V_s is related to the total current I as

$$V_S = 4S\left[\frac{I}{w_s + 2w_c}\tan^{-1}\left(\frac{w_s}{2h}\right)\right]10^{-1}(\text{mV}). \tag{8}$$

It is pertinent to mention that (8) is applicable only when B_x is within the linear range of the sensor. Therefore, from the design perspective, w_s can be set to the maximum for the given sensor package, leaving width of thicker trace w_c as the only design parameter. w_c needs to be adjusted till the maximum value of B_x for the maximum value of I falls within the linear range.

Finally, assuming symmetry of the two sensors S_1 and S_2, the TTS output $\Delta V_S = V_{S1} - V_{S2}$ can be expressed as

$$\Delta V_S = 8S\left[\frac{I}{w_s + 2w_c}\tan^{-1}\left(\frac{w_s}{2h}\right)\right]10^{-1}(\text{mV}). \tag{9}$$

V. TTS SOLUTION FOR A 75-KVA SIC-BASED POWER CONVERTER

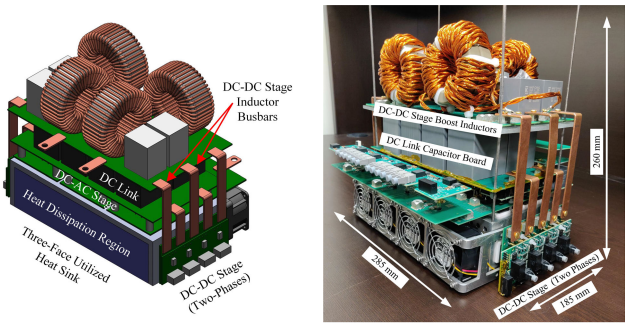
Power converters comprise passive components such as inductors, capacitors, and power semiconductor devices, which can be in discrete or module packages. The components degrade over time due to switching actions. Hence, it is imperative to promptly monitor these components' health to prevent major system failures [37]. Several approaches have been proposed in the literature that rely on measuring the converter current and voltage state variables to determine the values of health precursors [38], [39]. For instance, a DT-based health monitoring approach is developed for monitoring health of dc–dc stage of an in-house designed 75-kVA SiC-based power stage [40]. The performance of the DT approach relies on accurate measurement of current and voltages in the megahertz range [41].

Conventionally, shunt and hall-based sensors are predominantly used for sensing current for high-power applications. However, they suffer from having low bandwidth (hundreds of kilohertz) and conduction losses. For instance, in shunt measurement, the resistor must carry the rated current, generating heat, and if the resistor breaks down, the connection between the converter and the load breaks, potentially causing system instability or breakdown [20]. Similarly, Hall effect sensors suffer from large footprint, magnetic saturation, and high-temperature sensitivity.

For the in-house developed converter [40], a shunt-based current sensor is used for measuring inductor current of the dc–dc stage. The sensor comprises a thin-film resistor, with lower parasitics, coupled with an isolated AMC1302x series optically isolated differential amplifier from Texas Instruments, based on delta–sigma ($\Delta\Sigma$) modulator, with a bandwidth up to 800 kHz. However, due to parasitics of the resistor, the shunt measurement results have distortion and variable time delay. To counter this, digital filtering (Savitzky–Golay) filter and synchronization algorithms are used, which increases the computational complexity and slow the DT response time [42].

Fig. 14 shows the structure of the converter, developed in [40]. The power stage of the intelligent power stage (IPS) is electro-mechanically-thermally co-designed and 3-D packaged on a cylindrical hole-based heat sink, providing optimal thermal performance and mechanical stability. The dc–dc stage is split into two parts, each comprising two phases, placed on the side of the heat sink. The dc–ac stage is arranged on the top side of the heat sink, with the dc-link capacitor PCB sitting on top of it. The dc–dc stage boost inductors are placed on the top with side bus bars connecting the inductors with the boards.

The proposed TTS solution in Fig. 2(b) is low-cost and noninvasive and has the potential to alleviate the performance



(a) (b)

Fig. 14. Three-dimensional packaged dc–dc–ac converter in [40]. (a) Conceptual drawing. (b) Hardware prototype.

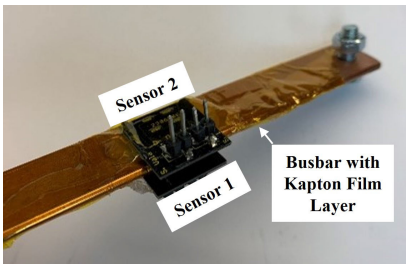


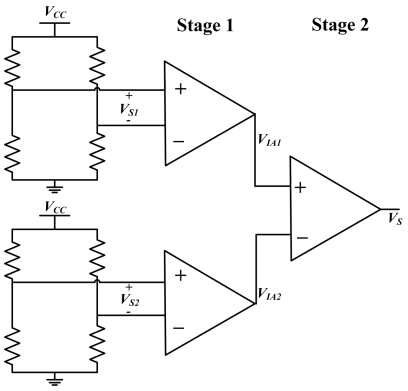
Fig. 15. Bus bar with TTS solution.

limitation of the shunt-based measurement system. The sensors can be placed on the top and bottom side of the bus bar and their output can be subtracted to yield the final sensor output. Fig. 15 shows the converter bus bar for channel 1 of the dc–dc stage with TMR sensor PCBs attached on both sides. The TMR sensor employed is CT100 from Crocus (Table III). The sensor pins on the board are shielded using the same approach of Design IV in Fig. 9. Further, the PCB is 0.8 mm thick and serves as an insulator between the sensor and the current-carrying bus bar.

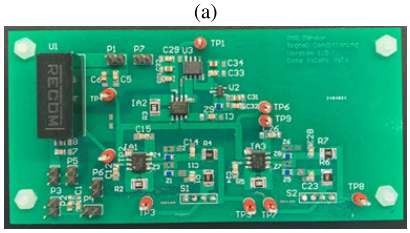
For amplifying the output of the sensor, a signal conditioning board using Texas Instruments INA821 Instrumentation Amplifier (IA) is developed for concept validation. Fig. 16 depicts the schematic and the developed board. The signal conditioning comprises two-stage amplification. In stage 1, the individual output of each of sensor is amplified. As the TMR sensor output and IA input are fully differential, the CM noise is canceled to a greater extent in the first amplification stage. The amplified output in stage 1 is then fed to the final IA, which subtracts the sensor outputs to yield the final single-ended output with an offset of $V_{CC}/2$. Any residual unattenuated CM noise after the first amplification stage is further attenuated in the second stage. The final sensor output can be expressed as

$$V_S = G_2 G_1 (V_{S1} - V_{S2}). \tag{10}$$

G_1 and G_2 are the gains of the first and second stage, respectively. The peak inductor current for the dc–dc stage is 37.5 A for which the sensor produces an output of 6 mV with 5 V supply for the given thickness (2.5 mm) and width (15 mm) of the bus bar [27]. Therefore, to amplify the output



(a)



(b)

Fig. 16. Signal conditioning for the proposed TTS solution. (a) Schematic. (b) Developed board.

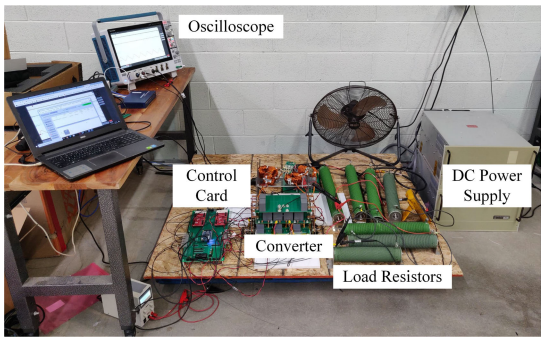


Fig. 17. Experimental setup.

TABLE V
DC–DC STAGE TEST CONDITIONS

Parameter	Value
Input voltage (V)	500
Output Voltage (V)	800
Power (W)	3500
Switching Frequency (kHz)	70

substantially, G_1 and G_2 are both set to 9, providing a total gain of 81 with 1 MHz bandwidth.

The developed bus bar with TTS solution is assembled back to the converter and continuous standalone tests for the dc–dc stage are performed at 500 V dc and 3.5 kW (Fig. 17). The test conditions are summarized in Table V. The TMR sensors and the signal condition circuitry is powered from an isolated 5-V power supply on the control card. For benchmarking, the shunt current sensor, originally developed for the converter, is also connected in series with the bus bar. Fig. 18, shows the excerpt of the measured current waveforms. The first trace from top is the current waveform captured by the hall-based current probe (Tektronix TCP0030A). The second trace is the final

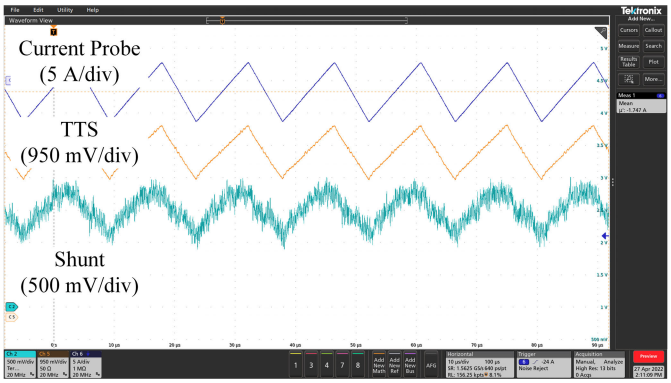


Fig. 18. Test results comparing the performance of current probe, shunt resistor, and TTS solution.

output of the TTS solution, followed by the output of shunt sensor in the third trace. Both TTS and shunt sensor are able to capture the triangular shape of the inductor current waveform. However, the output of the shunt sensor is superimposed with high-frequency noise. In contrast, the output of TTS solution is clean and follows the current probe results, justifying the efficacy of the proposed approach.

VI. Conclusion

This article presents a low-cost, noninvasive, precise, and high-bandwidth TTS current measurement solution based on TMR current sensors for next-generation WBG-based power modules and power converters. The TTS measurement solution consists of TTSs located on two sides of a PCB-based terminal or PCB boards sandwiching the copper terminal. Both proposed arrangements are compatible with any configuration, power module or power converter. Further, due to the proximity of the two sensors, the TTS solution is insensitive to temperature variation with twice the sensitivity. The efficacy of the TTS solution is validated on an in-house developed double-sided cooled power module and a 3-D packaged power converter. A slitted PCB terminal design is devised for the power module, which alleviates the skin effect and has lower parasitic capacitive coupling due to wire-bonded connections. Likewise, a bus bar-based TTS solution, coupled with a high CMRR-based signal conditioning, is developed and benchmarked against the existing shunt measurement solution for the power converter. The TTS solution outperforms the shunt measurement system with high bandwidth, enabling the development of advanced health monitoring and fault prognostics and diagnostics for future WBG-based power electronics.

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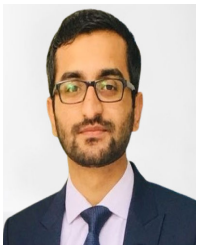

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