Split Inductor Design Considerations for Split-Phase Three-Phase Inverter

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***Abstract*—Two-Level Split-Phase (2L-SP) topology has emerged as a promising candidate for Wide Band Gap (WBG)-based Two-Level (2L) three-phase inverters. 2L-SP comprises P and N-cells whose mid-points are connected through split inductors. Compared with standard 2L, 2L-SP provides better immunity to crosstalk, lower switching loss, and conducted EMI emissions, which is favorable for WBG devices. However, these performance metrics depend on the value of split inductance. Further, split inductors experience a current spike during the switching transition. Although increasing split inductance is shown to improve the metrics and suppress the current spikes, an approach for optimal selection of split inductance is yet to be devised. This paper presents an analysis for design considerations, based on current spikes, for split inductor sizing. At first, a simplified model is derived and validated on a 75 kVA SiC-based hardware prototype. This is followed by an analysis of proposed model in the context of split inductor sizing.**

***Index Terms*—Current spikes, split-inductor sizing, split-phase topology (2L-SP), two-level inverter (2L), wide band gap (WBG).**

I. Introduction

Adopting WBG devices in a standard 2L inverter topology has enabled high power density and efficiency targets [1], [2]. However, the fast-switching capability (dv/dt and di/dt) of WBG devices brings several concerns and challenges [3], [4]. These include increased switching losses, Electromagnetic Interference (EMI), and the possibility of spurious or Miller turn ON of the complementary device during switching events [5], [6]. Furthermore, the increased dv/dt exacerbates Partial Discharge (PD) and the Reflected Wave Phenomenon (RFP) in cable connected motor drives, resulting in premature insulation failure and reduced operational lifespan [7]. Addressing these challenges is imperative to fully capitalize on the benefits offered by WBG devices in 2L inverter topology, ensuring enhanced system performance, reliability, and lifespan.

Recently, split-phase (2L-SP) topology has been proposed to be effective in overcoming the above-mentioned challenges associated with WBG device-based 2L inverters [8]–[11]. 2L-SP topology comprises P and N-cells, with split inductors L_s connected between the mid-point of these cells (Fig. 1). This configuration provides several benefits such as increased crosstalk immunity, lower combined (turn ON and OFF) switching loss and reduced EMI emissions [12], [13]. In [12], a comprehensive device loss analysis is conducted for a 2L-SP inverter with Sinusoidal Pulse Width Modulation (SPWM). The analysis covers device loss variation with key performance metrics, including SPWM modulation index (m), switching frequency (f), power factor angle (ϕ), and conduction current amplitude (I_{cm}). According to the results, the device loss variation with performance metrics (m, f, ϕ and I_{cm}) for 2L-SP is always upper bounded by that of the 2L inverter.

Further from an EMI/EMC perspective, the dv/dt of the mid-point voltages of P and N-cells is lower due to presence of split inductors [9], [12]. During the switching transition in a 2L-SP phase-leg, the split inductors and complementary cell power devices' output capacitance form a low frequency resonant circuit resulting in slower rise of the mid-point voltages [9]. The resonance ceases once the mid-point voltage reaches the DC link V_{DC} and the voltage is clamped. The lower dv/dt provides a potential benefit of lowering Common Mode (CM) emissions, which has been analyzed in [14].

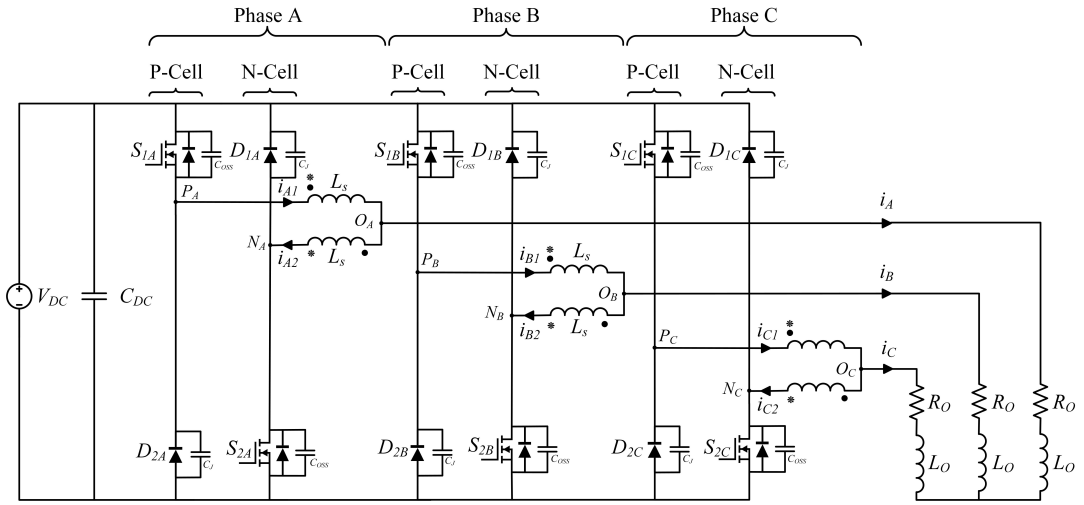


Fig. 1. 2L-SP three-phase inverter schematic.

Despite the benefits offered by WBG-based 2L-SP over 2L, split inductors L_s brings concern of current spikes/ramp-up during the switching transition [9]. Due to L_s, the P and N-cell mid-point voltage rises/falls with different slew rates, resulting in a significant transient voltage applied across L_s and causing ramp-up of current. In [9], the switching transition equivalent circuit has been analyzed in detail for 2L-SP phase-leg and is extended briefly to the three-phase configuration. It is concluded that increasing L_s aids in lowering current spikes. However, the analysis presented is solely for the uncoupled inductor configuration with zero initial conditions. Further the analysis does not focus on sizing and optimization aspect of L_s with different coupling configurations (direct and inverse).

This paper presents design considerations for split inductor sizing for a 2L-SP three-phase inverter, based on current spike amplitude. At first, a simplified switching transition equivalent circuit model is proposed, which is load independent and incorporates initial conditions. The proposed model is validated on a 75 kVA SiC-based hardware prototype with SPWM. This is followed by a discussion on the proposed model in context of split inductor sizing for uncoupled and coupled configurations.

II. Switching Transition Equivalent Circuit Modeling

Fig. 1 shows the schematic of three-phase 2L-SP inverter. The split inductors L_s in each phase can be either uncoupled, direct or inverse coupled. According to [9], during the switching transition, a transient voltage appears across L_s leading to current spike/ramp-up. For any modulation scheme, the switching transition happens in one phase-leg at a time. The other phases are clamped to VDC + (DC link) or VDC – (power ground). For instance, in phase A, the two switching transitions are S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF or S_{1A} ON $\rightarrow$ OFF and S_{2A} OFF $\rightarrow$ ON. The symbolic waveforms for S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF switching transition are shown in Fig. 3.

The equivalent circuit during switching transition comprises L_s and complimentary cell's MOSFET and diode output capacitances C_{OSS} and C_J. The equivalent switching transiting circuit for phase A for S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF transition in s-domain is shown in Fig. 2. The current sources represent the inductor currents or capacitor waveforms at start of switching transition. Assuming, balanced system ($i_A + i_B + i_C = 0$), the circuit can be reduced to circuit 1, where phase B and C parameters are lumped. This circuit representation can be further reduced assuming R_O and $L_O >> L_s$, which is generally the case otherwise significant output voltage will drop across L_s. Hence, the middle branch containing L_s, L_O and R_O can be removed as its impedance Z is much higher than the right parallel branch containing L_s, C_{OSS} and C_J. This yields the final reduced circuit model 2, which is load independent, incorporates L_s initial conditions and is applicable for all phases.

For S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF, $v_s(t) = V_{DC}u(t)$ and $V_O = 0$ and for S_{1A} ON $\rightarrow$ OFF and S_{2A} OFF $\rightarrow$ ON $v_s(t) = V_{DC}(1 - u(t))$ and $V_O = V_{DC}$ with nodes P_A and N_A swapped and I_{A2} replaced with $-I_{A1}$. Further, $v_s(t)$ represents MOSFET' $v_{DS}(t)$, which is considered as step voltage source in the analysis.

Solving final reduced circuit model 2 in Fig. 2 with $L = 2L_s \pm 2kL_s$ and $C = C_{OSS} + C_J$ yields the expressions for $v_{OA}(t)$, $v_{NA}(t)/v_{PA}(t)$, time rise t_r and current rise $\Delta i_s = \Delta i_{A1} = \Delta i_{A2}$ (1)-(8). The voltages expressions $v_{OA}(t)$, $v_{NA}(t)/v_{PA}(t)$ are derived with reference to DC link negative (0 V). Further, k represents the coupling factor and kL_s is the mutual inductance term. Based on the current direction assumed in Fig. 1 in each phase leg, kL_s is 0 for uncoupled, takes positive + sign for inverse coupling (represented by dot) and negative - sign for direct coupling (represented by asterisk).

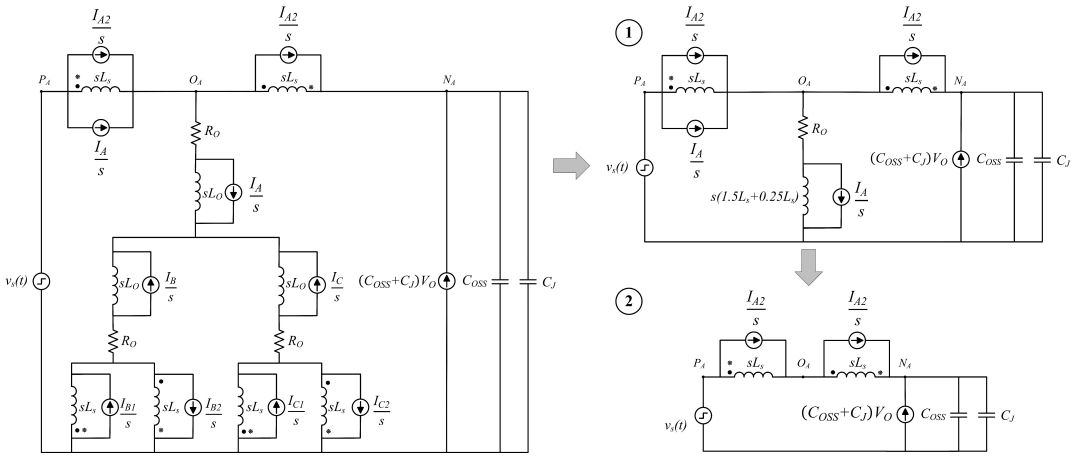


Fig. 2. S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF switching transition equivalent circuit model reduction.

A. S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF

$$v_{NA}(t) = V_{DC}\left(1 - cos\left(\frac{t}{\sqrt{LC}}\right)\right) + I_{A2}\sqrt{\frac{L}{C}}sin\left(\frac{t}{\sqrt{LC}}\right) \quad (1)$$

$$t_r = \sqrt{LC}tan^{-1}\left(\frac{V_{DC}}{I_{A2}}\sqrt{\frac{C}{L}}\right) \quad (2)$$

$$v_{OA}(t) = V_{DC}\left(1 - \frac{1}{2}cos\left(\frac{t}{\sqrt{LC}}\right)\right) + \frac{I_{A2}}{2}\sqrt{\frac{L}{C}}sin\left(\frac{t}{\sqrt{LC}}\right) \quad (3)$$

$$\Delta i_s = V_{DC}\sqrt{\frac{C}{L}}sin\left(\frac{t_r}{\sqrt{LC}}\right) - 2I_{A2}sin^2\left(\frac{t_r}{2\sqrt{LC}}\right) \quad (4)$$

B. S_{1A} ON $\rightarrow$ OFF and S_{2A} OFF $\rightarrow$ ON

$$v_{PA}(t) = V_{DC}cos\left(\frac{t}{\sqrt{LC}}\right) - I_{A1}\sqrt{\frac{L}{C}}sin\left(\frac{t}{\sqrt{LC}}\right) \quad (5)$$

$$t_r = \sqrt{LC}tan^{-1}\left(\frac{V_{DC}}{I_{A1}}\sqrt{\frac{C}{L}}\right) \quad (6)$$

$$v_{OA}(t) = \frac{V_{DC}}{2}cos\left(\frac{t}{\sqrt{LC}}\right) - \frac{I_{A1}}{2}\sqrt{\frac{L}{C}}sin\left(\frac{t}{\sqrt{LC}}\right) \quad (7)$$

$$\Delta i_s = -V_{DC}\sqrt{\frac{C}{L}}sin\left(\frac{t_r}{\sqrt{LC}}\right) + 2I_{A1}sin^2\left(\frac{t_r}{2\sqrt{LC}}\right) \quad (8)$$

The voltage expressions $v_{OA}(t)$, $v_{NA}(t)/v_{PA}(t)$ for both switching transition have sinusoidal terms due to series resonance between split inductors and device output capacitance with the resonant frequency ω_s

$$\omega_s = \frac{1}{\sqrt{LC}} \quad (9)$$

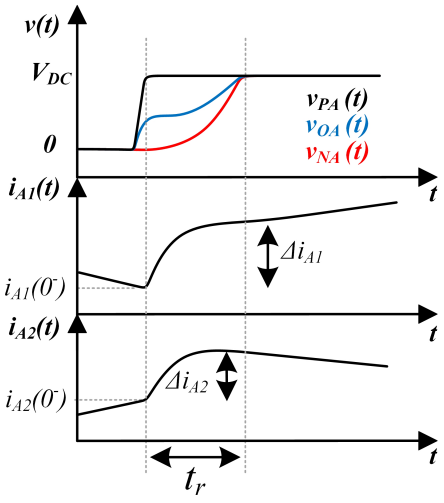


Fig. 3. S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF.

The voltage of nodes P_A, O_A, N_A resonate with angular frequency $\omega = \omega_s$ after the switching transition. When the voltage reaches the final value VDC + or VDC –, depending upon the switching transition, the resonance is suppressed as the voltage is clamped by the DC link. Similarly, the current also oscillates and the current rise Δi_s is the portion of the ringing current till the resonance lasts.

For both switching transitions, it is evident that the expressions for t_r (2) and (6) are the same with respective initial conditions (I_{A1} and I_{A2}). Similarly, the expressions for Δi_s (4) and (8) exhibit sign inversion in sinusoidal terms but yield the same absolute value. Hence for simplicity, the final generalized expressions for t_r and Δi_s for both switching transitions, with I_{A1} and I_{A2} denoted as $iL_s(0^-)$, can be written as

$$t_r = \sqrt{LC}tan^{-1}\left(\frac{V_{DC}}{iL_s(0^-)}\sqrt{\frac{C}{L}}\right) \quad (10)$$

TABLE I
PROTOTYPE SPECIFICATIONS

Parameter	Value
DC Link (V)	800
Output Voltage (V)	480 L-L RMS
Carrier Frequency (kHz)	30
Fundamental Frequency (Hz)	60
SiC MOSFET	CREE C3M0016120D
SiC Schottky Diode	Onsemi FFSH50120A

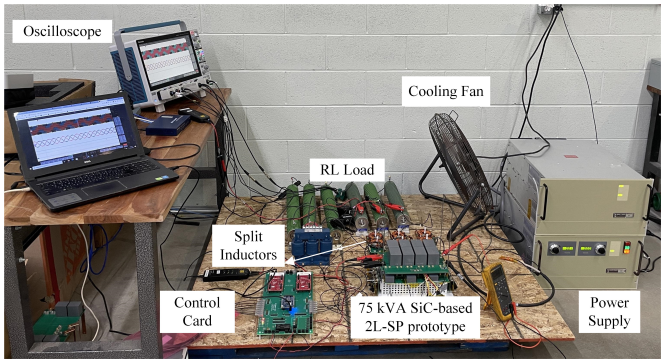


Fig. 4. Experimental Setup.

$$\Delta i_s = \underbrace{V_{DC}\sqrt{\frac{C}{L}}sin\left(\frac{t_r}{\sqrt{LC}}\right)}_{\text{zero-state response}} \underbrace{-2iL_s(0^-)sin^2\left(\frac{t_r}{2\sqrt{LC}}\right)}_{\text{zero-input response}} \tag{11}$$

III. Model Validation

A 75 kVA SiC-based prototype, inspired from [15], for 2L-SP is developed and tested to validate the proposed simplified model. Fig. 4 shows the experimental setup. The DC link V_{DC} is set to 800 V with 0.979 SPWM modulation index to achieve 480 V L-L RMS. The inverter output is connected to 10 kVA 0.7 pf R-L load. The prototype specifications are tabulated in Table I.

Fig. 5 compares the experimental and proposed model-based S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF switching transition waveforms for phase A with $L_s = 10$ µH and $iL_s(0^-) = 0$. The theoretical results are computed using (1)-(4) with device output capacitances values C_{OSS} and C_J, at 800 V, extracted from the manufacturer's datasheet [16], [17]. The theoretical results agree well with the experimental results, justifying the efficacy of the proposed model.

IV. Split Inductor Sizing

According to (11), the current rise/spike Δi_s is a non-linear function of L_s, power devices' output capacitances (C_{OSS} and C_J) and L_s initial condition ($iL_s(0^-)$). From a performance perspective, the current rise should be minimum to minimize core and conduction loss. For devising criteria for achieving lower Δi_s, the effect of each variable needs to be analyzed.

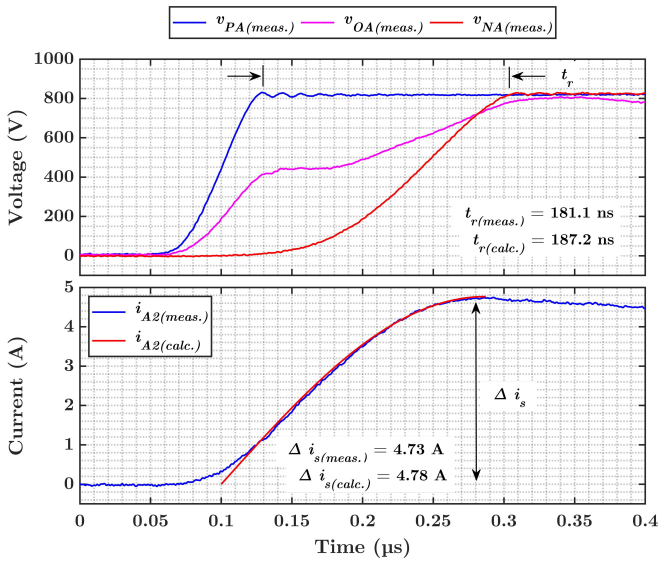


Fig. 5. Experimental results for S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF switching transition.

A. $L = 2L_s \pm 2kL_s$ and $C = (C_{OSS} + C_J)$

L and C appear in amplitude and argument of sinusoidal terms in (11). Substitution of t_r simplifies the argument of sinusoidal terms in (11) as

1) Zero-State Response:

$$V_{DC}\sqrt{\frac{C}{L}}sin\left(tan^{-1}\left(\frac{V_{DC}}{iL_s(0^-)}\sqrt{\frac{C}{L}}\right)\right) \tag{12}$$

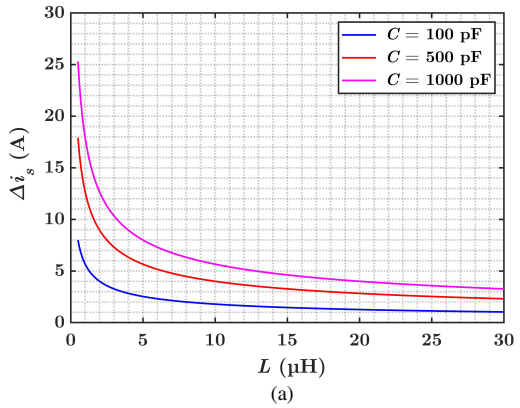
2) Zero-Input Response:

$$2iL_s(0^-)sin^2\left(0.5tan^{-1}\left(\frac{V_{DC}}{iL_s(0^-)}\sqrt{\frac{C}{L}}\right)\right) \tag{13}$$

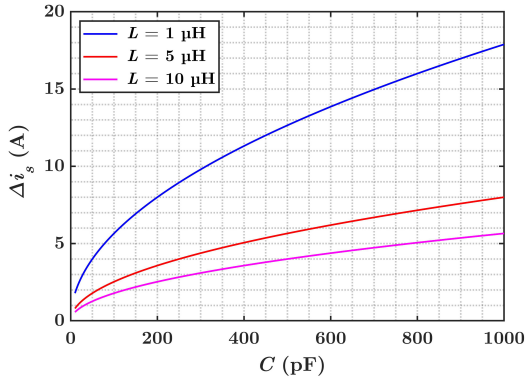
According to [9], $iL_s(0^-)$ must be > 0 for the equivalent circuit in Fig. 2 to be applicable. For instance, for S_{1A} OFF $\rightarrow$ ON and S_{2A} ON $\rightarrow$ OFF switching transition if $iL_s(0^-) = I_{A2} < 0$, then as S_{1A} turns ON and S_{2A} turns OFF, i_{A2} commutates from the channel of S_{2A} to its body diode, clamping node N_A to 0 while node P_A is clamped to V_{DC}. This results in quick freewheeling that lasts till i_{A2} becomes zero. After this, the equivalent switching transition circuit becomes the one in Fig. 2 with $iL_s(0^-) = I_{A2} = 0$.

As $iL_s(0^-)$ must be > 0, the argument of tan^{-1} term is always ≥ 0, which implies $0 \leq tan^{-1} \leq \pi/2$. For the same $iL_s(0^-)$ and V_{DC} as L increases, tan^{-1} decreases and sin decreases. Similarly, the amplitude scaling term $V_{DC}\sqrt{(C/L)}$ decreases. Finally, as a result, Δi_s decreases . In other words, increasing L has a compound effect in lowering $iL_s(0^-)$. However, the trend is the opposite for C. As C increases, tan^{-1} increases and sin increases. Also, the amplitude scaling term $V_{DC}\sqrt{(C/L)}$ and eventually Δi_s increases.

A parametric study is performed to examine the influence of L and C on Δi_s. The study involves varying L and C in (10)-(11), one at time with $V_{DC} = 800$ V and $iL_s(0^-) = 0$. To



(a)



(b)

Fig. 6. Variation of Δi_s. (a) With $L = 2L_s \pm 2kL_s$. (b) With $C = (C_{OSS} + C_J)$.

analyze the impact of inductance L on Δi_s, L is varied from 0.5 µH to 30 µH for three values of C (100 pF, 500 pF and 1000 pF). Similarly, to investigate the effect of capacitance C on Δi_s, C is varied from 10 pF to 1000 pF for three valued of L (1 µH, 5 µH and 10 µH). The results are summarized in Fig. 6.

According to the results in Fig. 6(a), Δi_s follows an inverse relation with L for all values of C. Additionally, the curves demonstrate a positive offset dependency with C. For lower values of L_s, Δi_s falls steeply, with the extent of steepness being proportional to the value of C. However, as L increases, the curves exhibit a knee point where the reduction in Δi_s with further increase in L becomes minimal. Beyond this knee point, Δi_s tends to saturate. Therefore, from a design perspective, selecting the value of L at the knee point is optimal to prevent oversizing of $L = 2L_s \pm 2kL_s$.

In contrast, Δi_s exhibits a non-linear increasing relationship with C for all values of L (Fig. 6(b)). The rise in Δi_s with C is steeper for low values of L. Moreover, compared with L, there is no knee-point in Δi_s with C. Finally, from a design perspective, the non-linear rising trend of Δi_s with $C = (C_{OSS} + C_J)$ implies that WBG devices (SiC and GaN) with lower output capacitance than their Si counterparts are more feasible for 2L-SP.

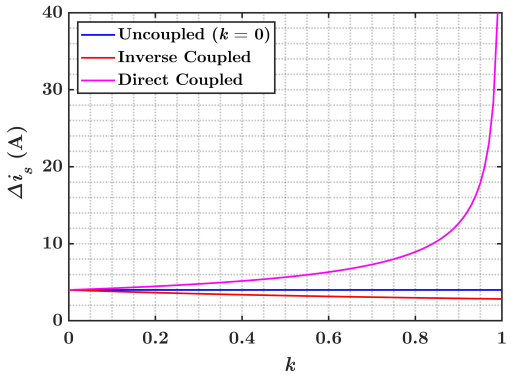


Fig. 7. Variation of Δi_s with k.

B. Coupling Factor k

A 2L-SP phase-leg comprises two split inductors, which can be uncoupled, direct or inverse coupled. The total inductance L is sum of self inductances L_s and the mutual inductance kL_s ($L = 2L_s \pm 2kL_s$). The extent of coupling is determined by the coupling factor k, ranging from 0 to 1. Based on the current direction through L_s assumed each phase-leg in Fig. 1 and Fig. 2, kL_s is zero for uncoupled, additive for inverse coupling (represented by dot) and subtractive for direct coupling (represented by asterisk).

According to trend seen in Fig. 6(a), Δi_s varies inversely with L. The value of L is dependent on L_s and kL_s. As kL_s is additive for an inverse coupled configuration, it is evident that the inverse coupled configuration will result in maximum L and, consequently, minimum Δi_s. On the other hand, the direct coupled configuration will yield minimum L and maximum Δi_s for a given combination of k and L_s. This trend is further illustrated in a Fig. 7, which plots the variation of Δi_s with k for all coupling configurations, assuming $L_s = 10$ µH, $C = 500$ pF, $iL_s(0^-) = 0$, and $V_{DC} = 800$ V.

As k increases, Δi_s rises exponentially for direct coupled configuration while it decreases slowly for inverse coupled configuration. A horizontal line is included in the plot for comparison purposes, representing the uncoupled case ($k = 0$). The slight decrease of Δi_s with an increase in k can be explained from Fig. 6. For the inverse coupled configuration, the total inductance L is higher than L_s and may surpass the knee-point, beyond which the influence of L on Δi_s becomes minimal.

C. Initial Condition $iL_s(0^-)$

The initial condition $iL_s(0^-)$ appears in the denominator in the argument of tan^{-1} term in (12)-(13), implying that as $iL_s(0^-)$ increases, tan^{-1} decreases, sin decreases and finally Δi_s decreases. Further, the zero-input response containing $iL_s(0^-)$ in amplitude in (13), has the opposite sign to the zero-state response, implying that as $iL_s(0^-)$ increases Δi_s decreases. In other words, $iL_s(0^-)$ aids in lowering Δi_s .

For exemplification, Fig. 8 shows an inverse trend of Δi_s with increasing $iL_s(0^-)$ for three combinations of L and C with $V_{DC} = 800$ V. The baseline is the $L = 1$ µH, $C = 100$ pF

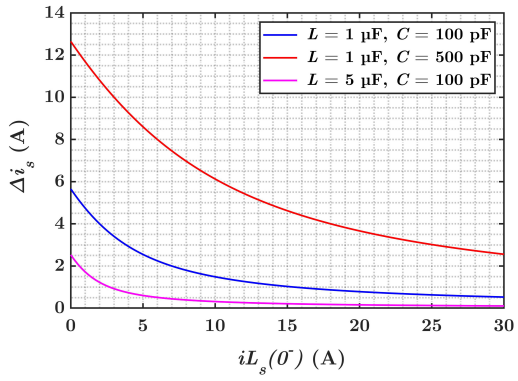


Fig. 8. Variation of Δi_s with $iL_s(0^-)$.

combination. The impact of increasing one parameter L or C is analyzed in the other two combinations. Increasing L from 1 µH to 5 µH lowers the maximum Δi_s (at $iL_s(0^-) = 0$) along with gradual decrease in Δi_s with increase in $iL_s(0^-)$. The trend is the opposite when increasing C from 100 pF to 500 pF. Finally, from a design perspective, the maximum Δi_s occurs for $iL_s(0^-) = 0$ and hence (11) with zero initial condition can be used for sizing $L = 2L_s \pm 2kL_s$ for a given k, V_{DC} and C.

Lastly, in a 2L-SP inverter, Δi_s changes dynamically over the fundamental cycle due to varying $iL_s(0^-)$. Based on the analysis above, maximum Δi_s occurs for $iL_s(0^-)$. Hence from the design perspective, (11) with $iL_s(0^-) = 0$ can be used for sizing L_s for a given k, V_{DC} and C.

V. Conclusion

2L-SP topology can alleviate the challenges of increased crosstalk, switching loss and EMI emissions associated with standard 2L topology with WBG devices. However, split-inductors in 2L-SP experience current spikes/ramp-up during switching the transition. For optimal sizing of split inductors, a switching transition circuit needs to be derived and analyzed. This paper proposes a generalized, load-independent switching transition equivalent circuit model for coupled and uncoupled inductor configurations. The model is verified on a 75 kVA SiC-based 2L-SP prototype. Finally, based on parametric analysis of the model, it can be concluded that inverse coupled configuration for split inductors and devices with lower output capacitances are the most effective combination in achieving lower current spikes. Lastly, since WBG devices have lower output capacitance than Si, they are well suited for the 2L-SP topology.

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