

Investigation of Common-Mode EMI in Three-Phase Split-Phase Inverter

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Abstract—Compared with the traditional two-level (2L) inverter, two-level Split-Phase topology (2L-SP) provides better cross-talk immunity without deadtime between the top and bottom devices. From the Common Mode (CM) EMI perspective, split inductors in 2L-SP tend to increase the CM noise path impedance and decrease the dV/dt across the device during the switching transition due to the interaction between split inductors and the semiconductor device's parasitic capacitance. This phenomenon, in turn, reduces the dV/dt of the CM voltage, making 2L-SP topology a promising candidate with lower CM emission for Wide Band Gap (WBG) devices-based 2L inverters, switching at high frequency. However, the CM EMI of 2L-SP and its comparison with 2L have yet to be analyzed comprehensively. This paper investigates conducted CM EMI emission of a SiC-based 2L-SP three-phase inverter with SPWM. At first, the derivation of the CM equivalent circuit model through frequency domain analysis is presented. This is followed by a comparative study of CM emission of 2L-SP three-phase inverter on a hardware prototype for different values of split inductance. The results show that increasing split-inductance significantly lowers the CM magnitude with a maximum reduction of 17.85 dB.

Index Terms—Common Mode (CM), Electromagnetic Interference (EMI), Frequency Domain Analysis, Silicon Carbide (SiC), Split-Phase Inverter.

I. INTRODUCTION

Adopting Wide Band Gap (WBG) devices in a standard 2L inverter topology has enabled high power density and efficiency targets. WBG devices allow high-frequency operation, effectively shrinking the size of the output filter [1]. Further, compared with Silicon (Si), WBG devices offer lower switching loss at high switching frequency. However, the fast switching capability of WBG brings concerns of spurious/Miller turn ON of complementary device during switching due to high dV/dt , a potential cause of current shoot through. Although having deadtime between top and bottom switches can alleviate crosstalk, deadtime increases THD in the output current and voltage.

Moreover, the pulse width modulation (PWM) in a 2L inverter generates a continuously varying Common Mode Voltage (CMV), which results in conducted and radiated CM emissions [2], [3]. 2L inverters based on WBG devices are intended to have higher switching frequencies, compared with their Si counterparts. The high switching frequency and dV/dt compatibility of WBG devices worsens the CM spectrum in the interested 150 kHz–30 MHz range with a higher possibility of violating EMI standards. This tightens the constraints on the

EMI filter design, resulting in a bulky filter for suppressing CM noise. Additionally, if the inverter is connected to a motor, high dV/dt can lead to excessive motor bearing currents and partial discharge in the winding insulation, requiring an additional output dV/dt filter [4]–[6].

Recently, split-phase (2L-SP) topology has been shown to be effective in overcoming challenges associated with WBG device-based 2L inverter [7], [8]. 2L-SP topology comprises a dissected version of the phase legs of a traditional 2L inverter. The phase-legs are split to form P-cell and N-cell, with split inductors L_s connected to the mid-point of these cells on one side and shorted on the other side (Fig. 1). The concept is similar to the split-scaling technique adopted in power modules for lowering parasitic inductance [9]. Insertion of split inductors helps to decouple P-cell and N-cell. For instance, the split inductors isolate the bottom switch from the top switch and its antiparallel diode and vice versa. Decoupling between P and N-cell allows the inverter to operate with zero deadtime, without possible current shoot-through. Moreover, the effective parasitic capacitance across the switch is reduced due to the decoupling of the device's antiparallel diode and complementary switch. This leads to reduced ON switching loss, slightly high OFF switching, but reduced total switching loss of the device [8], [10].

A detailed device loss analysis is performed in [8] for a 2L-SP inverter with SPWM. The device loss is analyzed for various metrics such as switching frequency f , modulation index M , power factor angle ϕ and conduction current amplitude I_{cm} . The results show that the device loss for 2L-SP is always upper bounded by loss for traditional 2L inverter for all considered performance metrics (f , M , ϕ and I_{cm}). Most notably, the total power device loss follows a direct relationship with f for 2L-SP and 2L. However, the increase in loss for 2L is higher than for 2L-SP as f increases, making 2L-SP a better candidate over 2L topology for WBG-based two-level three-phase inverters.

From the CM EMI perspective, the split inductors lower the dV/dt of the mid-point voltages of P and N-cells [8], [11]. During the switching transition, the mid-point voltages rise/fall slowly. This is caused by the interaction between split inductors and complimentary cell power devices' output capacitance [11]. The reduced dV/dt provides a potential benefit in lowering CM emission. However, this aspect has yet to be analyzed comprehensively. Among all existing literature

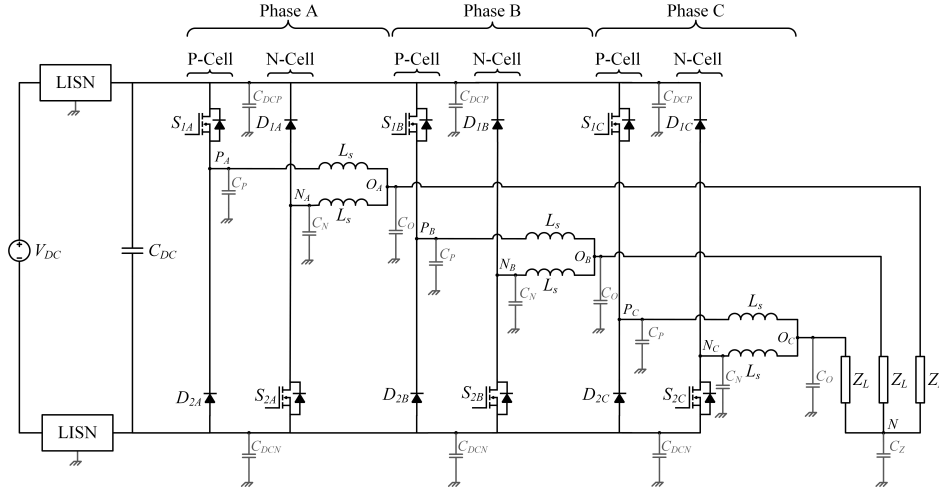


Fig. 1. 2L-SP three-phase inverter schematic.

presented, the EMI benefit has been explained in terms of FFT of output voltage. It is concluded that with the inclusion of split inductors, the magnitude of high-frequency harmonics is less due to lower dV/dt [8]. Nevertheless, no analysis in terms of conducted CM EMI is presented.

This paper investigates and compares the DC side CM emission of a 2L-SP three-phase inverter. Firstly, the CM equivalent circuit model is developed using frequency domain analysis. This is followed by a discussion on the variation of dV/dt of P and N-cell midpoint voltages with L_s . Lastly, the CM spectrum is examined for various values of L_s through experiments on a SiC-based hardware prototype.

II. 2L-SP CM EMI MODELING

EMI models are effective in analyzing EMI characteristics of power converters. The model aids in predicting and comparing EMI; evaluating the performance of EMI filters and devising techniques for EMI reduction. Hence to analyze CM emissions of 2L-SP topology, it is imperative to develop a CM EMI model for the 2L-SP three-phase inverter.

A. Derivation of CM Equivalent Circuit

Two basic approaches have been used predominantly for modeling EMI: Time Domain and Frequency Domain Analysis. Both approaches model the noise propagation paths and EMI noise source [12], [13]. The time domain approach relies on characterizing the noise sources based on behavioral or physical structure-based modeling. The models can be simulated using software to mimic the noise source. The noise spectrum is predicted through Discrete Fourier Transformation (DFT). The computation of DFT requires vast memory resources and the noise models need to be derived meticulously to ensure simulation convergence.

On the other hand, the frequency domain approach relies on substitution theory to replace the switching devices in the circuit with noise sources (voltage or current) to linearize and simplify the circuit [14]. The noise sources

have identical time-domain waveforms as in the actual circuit. The simplified circuit is modeled in the Laplace domain to derive analytical expressions for noise propagation paths. The analytical expressions provide insight into the potential noise propagation paths and is helpful in analyzing the CM emission profile. Therefore, the frequency domain analysis technique is chosen for modeling CM equivalent circuit for 2L-SP.

Fig. 1 shows the schematic of a DC fed three-phase 2L-SP inverter with LISNs connected on the DC side. The first step in CM modeling is to model the noise source. Assuming identical construction of three-phases, a single phase-leg can be first used for modeling and then extended to other phases.

The proceeding analysis utilizes phase A (Fig. 1). The CM emission depends on parasitic ground capacitances. The capacitances are distributed across the circuit and depend on the inverter assembly's structure. In Fig. 1, five capacitors (C_{DCP} , C_{DCN} , C_P , C_O and C_N) are considered for each phase to provide a path for CM current. C_{DCP} and C_{DCN} represent the parasitics capacitance from DC bus positive and negative to the ground chassis/heat sink. C_P , C_O and C_N represent the ground capacitors from mid-points of P-cell, N-cell and AC output to the ground respectively.

Fig. 2(a) shows the phase A circuit with substitution theory applied. The switches S_{1A} and S_{2A} are replaced with noise voltage sources v_{1A} and v_{2A} , mimicking switches' drain-source voltage. Similarly, the diodes D_{1A} and D_{2A} are replaced with noise current sources i_{1A} and i_{2A} respectively. It shall be noted that the noise sources v_{1A} , v_{2A} , i_{1A} and i_{2A} shall have the same time-domain waveforms. The circuit in Fig. 2(a) can be analyzed through the principle of superposition. The DC link capacitor C_{DC} acts as a short circuit due to its small impedance at high frequency. Further, it is evident that the current sources i_{1A} and i_{2A} are shorted out by noise voltage sources v_{1A} and v_{2A} . This leads to the model in Fig. 2(b), which can be extended to phases B and C, assuming symmetrical construction of the three-phases.

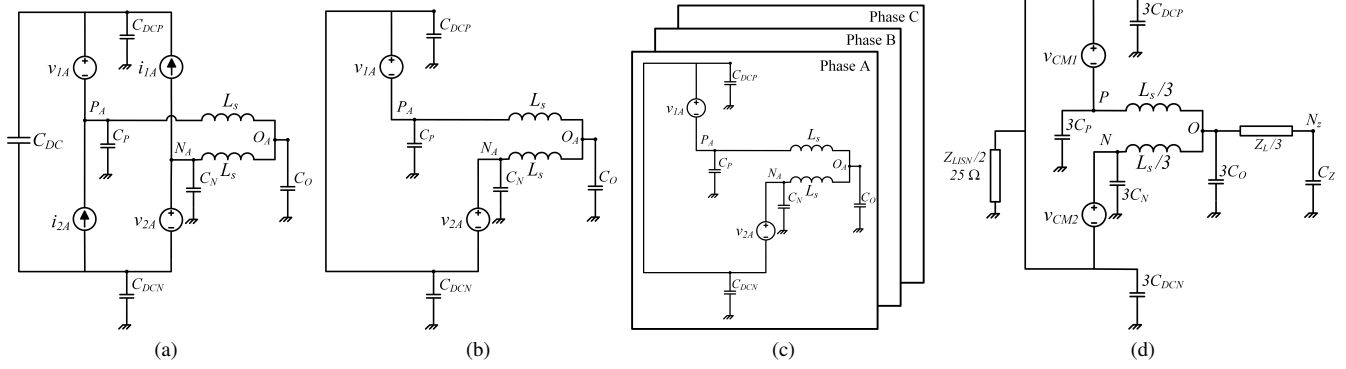


Fig. 2. CM EMI modeling of three-phase 2L-SP. (a) Phase A with noise sources. (b) Removal of current noise sources that do not contribute to CM noise. (c) Extension to three-phase. (d) CM equivalent model.

The noise voltage sources for phase B and C are phase shifted by 120° . Using superposition principle, the CM equivalent circuit for three-phase 2L-SP can be derived by defining two common-mode voltages v_{CM1} and v_{CM2} as

$$v_{CM1} = \frac{v_{1A} + v_{1B} + v_{1C}}{3} \quad (1)$$

$$v_{CM2} = \frac{v_{2A} + v_{2B} + v_{2C}}{3} \quad (2)$$

The final CM equivalent circuit with LISN and load Z_L is depicted in Fig. 2(d). In general for inverters, the CMV v_{CM} is defined as the voltage between load neutral point N_Z and ground [15]. From Fig. 2(d) it is evident that

$$v_{CM} = \frac{v_{CM1} + v_{CM2}}{2} \quad (3)$$

B. Analysis of Common Mode Voltages v_{CM1} and v_{CM2}

A three-phase 2L inverter can be realized from 2L-SP topology by bypassing the split inductors or shorting the midpoints of P and N-cell in each phase. The CM models proposed in the literature for simple 2L inverter comprises one CMV source, which is the average of three-phase voltages [15], [16]. In contrast, 2L-SP decouples the P-cell and N-cell, resulting in two separate CMV sources v_{CM1} and v_{CM2} .

As discussed in [8], [11], due to the insertion of split inductors, the voltages of midpoint of P-cell, N-cell and AC output rise gradually with lower dV/dt . The delay t_r depends on the value of split inductance L_s and output capacitances C_{OSS} and C_J of the MOSFET and diode of the other cell. As a result, the voltage transition of these midpoints varies. For instance, in phase A in Fig. 1, when the bottom switch s_{2A} turns OFF and top switch s_{1A} turns ON, the voltage of node P_A rises quickly with dV/dt of s_{1A} to V_{DC} . However, node O_A and N_A voltages rise slowly due to the interaction of split inductors with device capacitance. This implies that the CMV sources v_{CM1} and v_{CM2} have the same voltage levels and are in phase but differ during voltage level transition depending upon the switching transition from bottom to top switch or vice versa.

Fig. 3 shows the symbolic waveforms of CMVs v_{CM1} and v_{CM2} and the resultant v_{CM} . Both v_{CM1} and v_{CM2} have the same voltage levels $V_{DC}/2$, $V_{DC}/6$, $-V_{DC}/6$ and $-V_{DC}/2$. However, the rise/fall profile differs during voltage level transition, as shown by the zoomed-in view at two voltage level transitions in Fig. 3. For $V_{DC}/6$ to $V_{DC}/2$ transition, v_{CM1} rises quickly whereas v_{CM2} rises slowly due to L_s . The trend reverses for $V_{DC}/2$ to $V_{DC}/6$ where v_{CM2} falls quickly and v_{CM1} falls slowly. v_{CM} is the average of both CMVs and is bounded by them. If $L_s = 0$ (2L topology), both CMVs v_{CM1} and v_{CM2} become identical, leading to one CMV source as proposed in [16].

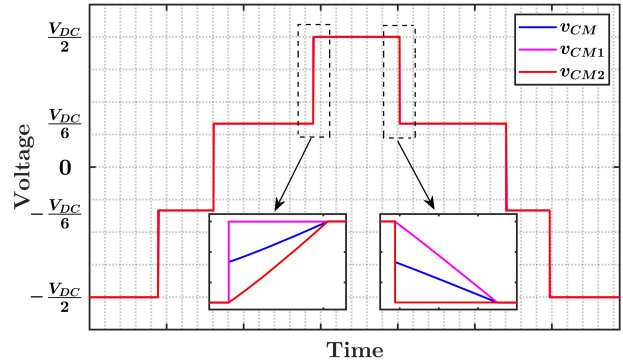


Fig. 3. Symbolic CMVs waveform for three-phase 2L-SP.

III. 2L-SP CM EMI EXAMINATION

To analyze and compare the CM emission of three-phase 2L-SP inverter for various values of L_s , a 18 kVA SiC based inverter prototype, inspired from [17], is developed. The proceeding subsections discuss the experimental setup and measured CM emission results.

A. Experimental Setup

Table I tabulates the specifications of the inverter prototype shown in Fig. 4. The inverter is built using discrete devices in TO-247 package with a vertical loop for power PCBs to lower parasitic inductance. The P-cell and N-cell mid-point

TABLE I
IPS SPECIFICATIONS

Parameter	Value
DC Link (V)	500
Output Voltage (V)	208 L-L RMS
Carrier Frequency (kHz)	30
Fundamental Frequency (Hz)	60
SiC MOSFET	CREE C3M0016120D
SiC Schottky Diode	Onsemi FFSH50120A

terminals are taken out separately on the power PCB. This layout allows the inverter to be configured as simple 2L or 2L-SP. Commercially off-the-shelf (COTS) inductors from Coil Crafts are used for split inductance. The inductors offer shielding and high self-resonant frequency (> 1 MHz).

For CM measurement, it is imperative to make unwanted CM noise propagation paths as inefficient as possible. One such unwanted path is through the gate drivers. The CM noise can propagate through PWM signal line from the control card or through the gate driver auxiliary power supply [18]. In the developed prototype, CM chokes are added in both 24 V and 5 V auxiliary power supply lines. For gate signals, a fiber optic interface is utilized, which provides flexibility in placing the control card at a distance and complete electrical isolation.

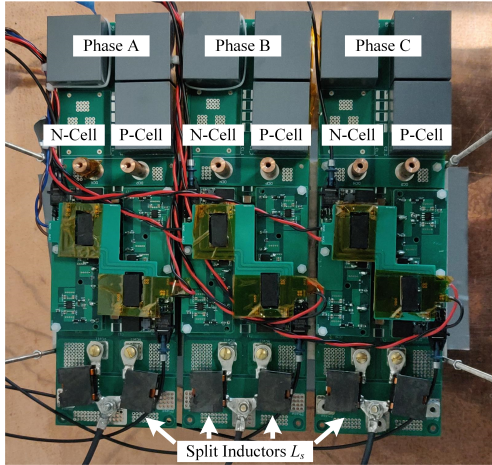


Fig. 4. Developed three-phase 2L-SP inverter prototype.

Fig. 5 shows the experimental setup for CM EMI measurement. A 2 kVA RL load is connected to the inverter's output side. The input DC side is connected through LISNs to a 1:1 ratio isolated Phase Shifted Full Bridge (PFSB) DC-DC converter, which is powered from the Spellman ST2P36 power supply [19], [20]. The ST2P36 power supply DC output negative terminal is grounded internally, which is the same as the ground plane for CM EMI measurement. If the power supply is connected directly to the inverter, the DC negative LISN is bypassed/shorted out for low frequencies due to the lower impedance of LISN's inductance. To mitigate this, the PFSB converter stage is connected between the power supply and LISNs to isolate the power supply ground.

The control card and inverter's gate drivers are powered from an isolated auxiliary power supply with CM chokes

placed in the supply lines. The SPWM modulation index is set to 0.7 and the gate signals are transmitted to the gate driver over a fiber optic interface.

Lastly, the output of both LISNs is connected to a 0° power splitter from Mini-Circuits [21]. The output CM noise is then fed to the spectrum analyzer. The connections from LISNs to the power splitter and spectrum analyzer are made using RG223 50 Ω doubled shielded coaxial cable, which provides better shielding against external fields than RG58 [22].

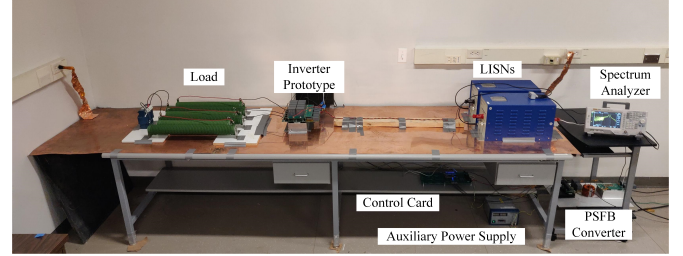


Fig. 5. CM EMI measurement experimental setup.

B. CM EMI Measurements

CM EMI tests are carried out on the inverter for various values of L_s (0 μH , 0.15 μH , 1 μH , 4.7 μH and 10 μH). The measurements are taken during the steady state operation of the inverter. It is pertinent to mention that $L_s = 0$ μH implies simple 2L topology, allowing fair comparison between CM emissions of 2L and 2L-SP inverter from the identical experimental setup and test conditions.

Fig. 6(a) shows the measured CM spectrum for all values of L_s in the interested 150 kHz–30 MHz range. The spectrum has the highest magnitude for 2L configuration ($L_s = 0$ μH), which decreases with an increase in L_s . For $L_s = 0.15$ μH , the reduction in CM noise is minimal, but it increases significantly as L_s goes beyond 1 μH . Further, there are two parallel (≈ 5 MHz and ≈ 7 MHz) and one series (≈ 6.2 MHz) resonance points in the spectrum for all values of L_s . As the value of L_s increases, the resonance points move slightly to left and the peak and trough values of parallel and series resonances reduce. A maximum reduction 9.75 dB is observed for the first resonance point with an increase in L_s as evident in Fig. 6(b), which compares the CM spectrum for $L_s = 0$ μH and $L_s = 10$ μH . Similarly, maximum 18 dB and 17.85 dB reduction is achieved in 150 kHz–1 MHz and in 10–30 MHz frequency ranges, respectively. Lastly, from the EMI filter perspective, the reduction in CM spectrum throughout the 150 kHz–30 MHz range is beneficial for shrinking the size of the CM filter.

TABLE II
SLEW RATE COMPARISON

L_s (μH)	Maximum dV/dt (V/ns)		
	P_A	O_A	N_A
0	7.6	7.6	7.6
10	17.1	6.0	1.9

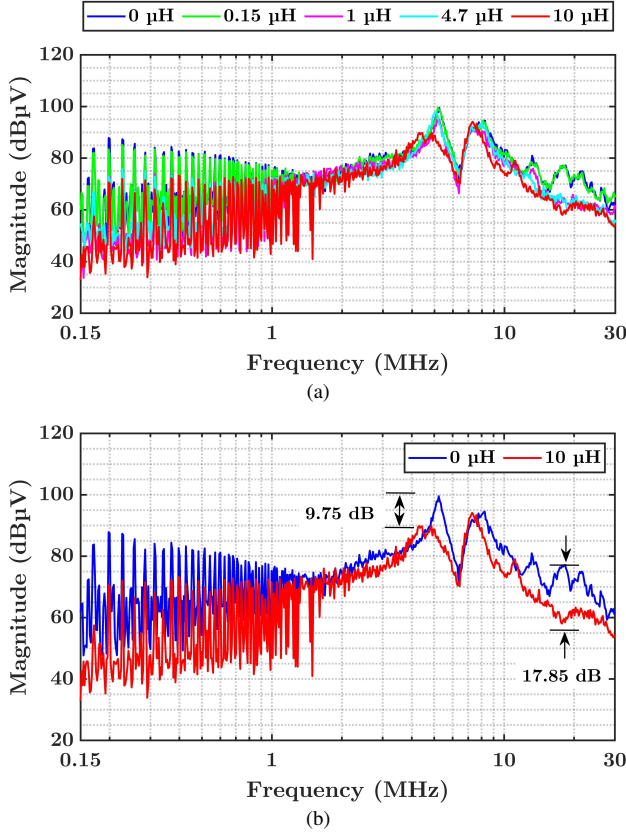


Fig. 6. Comparison of CM EMI measurements. (a) All values of L_s . (b) $L_s = 0$ μH and $L_s = 10$ μH.

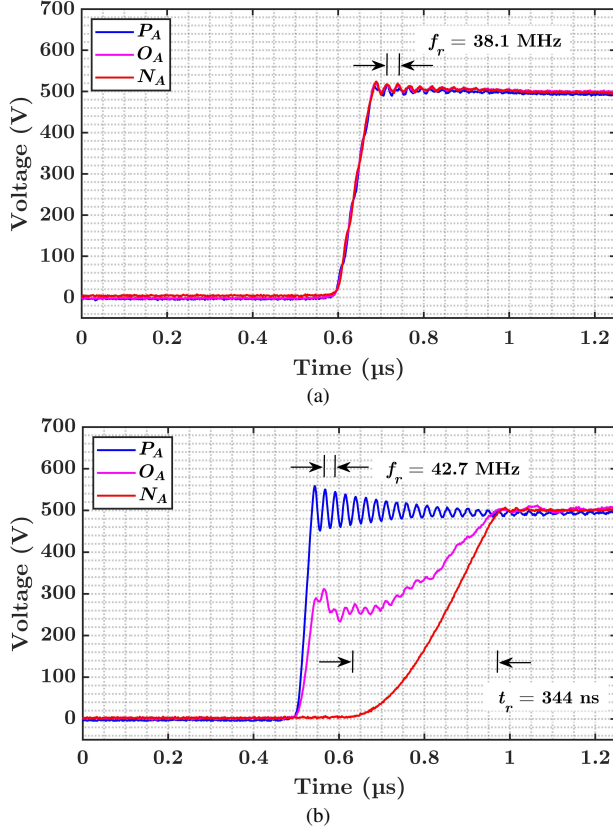


Fig. 7. Waveforms for phase A s_{1A} OFF → ON and s_{2A} ON → OFF switching transition. (a) $L_s = 0$ μH. (b) $L_s = 10$ μH.

The significant reduction in CM spectrum can be justified by gradual rise of AC output node and mid-point voltage of complementary switching cell due to L_s and increase in noise path impedance towards LISN due to L_s as shown in Fig. 2(d). To exemplify this, Fig. 7 shows the voltages of node P_A , O_A and N_A of phase A during s_{1A} OFF → ON and s_{2A} ON → OFF switching transition for two values of L_s (0 μH and 10 μH). For $L_s = 0$ μH, all three node voltages rise at the same rate. The parasitic ground capacitances C_P , C_O and C_N are excited with the same dV/dt. However, for $L_s = 10$ μH, the node O_A and N_A voltages gradually rise with lower dV/dt, reducing the excitation of parasitic capacitances C_O and C_N .

The maximum dV/dt observed during the switching transition for all three nodes is tabulated in Table II. The dV/dt of node P_A is increased with the inclusion of L_s due to the decoupling of N-cell device's output capacitance (C_{OSS} and C_J) from the P-cell [9]. This is also justified by an increase in overshoot ringing frequency in node P_A from 38.1 MHz to 42.7 MHz with addition of L_s as evident in Fig. 7(b). Despite the increase in dV/dt of node P_A , the cumulative CM noise appearing at LISNs is lower due to increased noise path impedance offered by the L_s as well have lower dV/dt of nodes O_A and N_A .

Lastly, the effect of low dV/dt due to L_s on CM emission can also be explained by comparing CMVs for both cases with and without L_s . Fig. 8 compares the measured CMV v_{CM} for $L_s = 0$ μH and $L_s = 10$ μH. The CMV voltage is measured between the load neutral point and the nearest point on the ground plane. Compared with the symbolic CMV waveform in Fig. 3, the measured v_{CM} has overshoot with ringing during voltage transition for both cases. However, the peak overshoot and decay time of oscillations for $L_s = 10$ μH is considerably lower than for 2L configuration ($L_s = 0$ μH). The ringing overshoot is due to the interaction between stray inductance and ground parasitic capacitance [14].

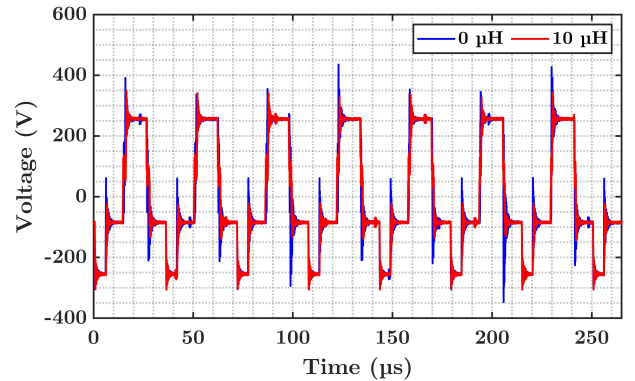


Fig. 8. CMV voltage comparison.

C. Split Inductor L_s Optimal Sizing

Although increasing L_s lowers the CM emissions of 2L-SP, as evident in Fig. 6, it is imperative to select an optimum value of L_s to meet performance and compliance targets.

From the inverter design and performance perspective, optimal selection of L_s is directly related to current spikes

through split inductors during the switching transition. As concluded in [8], [11], split inductors in 2L-SP experience current spikes with amplitude Δi_s during the switching transition, incurring core losses. During the switching transition, the output capacitances of the MOSFET C_{OSS} and diode C_J interact with L_s , resulting in transient voltage, which leads to a current spike. The cause of transient voltage is the delay in the rise of P and N-cell node voltages, as shown in Fig. 7(b) for $L_s = 10 \mu\text{H}$.

Increasing the value of L_s lowers the magnitude of spikes but at the cost of bulkier magnetic design and increases copper losses [11]. Hence for finding the optimal L_s , it is important to visualize the variation of Δi_s with L_s for given system parameters, which are DC link voltage V_{DC} , C_{OSS} and C_J . Fig. 9 shows the variation of Δi_s with L_s , based on the expressions derived in [11], for the developed prototype. Δi_s follows an inverse relation with L_s with a knee point at $L_s \approx 5 \mu\text{H}$. For lower values of split inductance ($L_s < 5 \mu\text{H}$), Δi_s falls steeply as L_s increases. However, for larger values ($L_s > 5 \mu\text{H}$), the reduction in Δi_s with increasing L_s is minimal. This implies that selecting L_s with a value above the knee point might not be optimum, as the minimal reduction in Δi_s is overshadowed by the increase in copper loss due to the increase in the number of turns and core dimension. Lastly, a high value of L_s , above the knee point, is also infeasible as it would cause a significant voltage drop across L_s , leading to lower output voltage across the load.

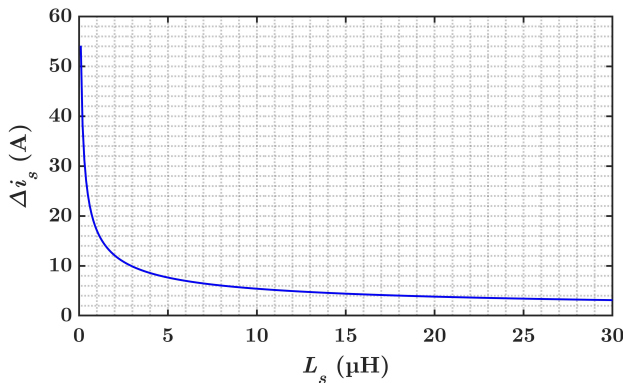


Fig. 9. Variation of Δi_s with L_s .

Further, from the CM emission perspective, the variables of interest are dV/dt and rise time t_r of the mid-point and output AC node voltages. According to Fig. 7(b), increasing L_s lowers dV/dt and increases t_r of the output and complementary cell's mid-point voltages, leading to lower CM emissions as evident in the CM EMI plots in the manuscript. Based on the expressions in [11], t_r depends on the same system parameters as for Δi_s , which are V_{DC} , C_{OSS} and C_J . Fig. 10 presents the variation of t_r with L_s for the developed prototype. Contrary to Δi_s , t_r follows a non-linear increasing relationship ($t_r \propto \sqrt{L_s}$) with L_s .

From the t_r vs L_s plot, it can be concluded that increasing L_s aids in lowering the CM emissions of the 2L-SP inverter

due to large t_r . However, relying solely on t_r vs L_s characteristics for finding the optimal L_s is infeasible due to non-linear increasing relationship ($t_r \propto \sqrt{L_s}$), resulting in the optimal point ($dt_r/dL_s \rightarrow 0$) at $L_s = \infty$. Hence, optimal selection of L_s can be made based on the inverse relationship between Δi_s and L_s , where the optimal value is the knee point of the Δi_s vs L_s curve.

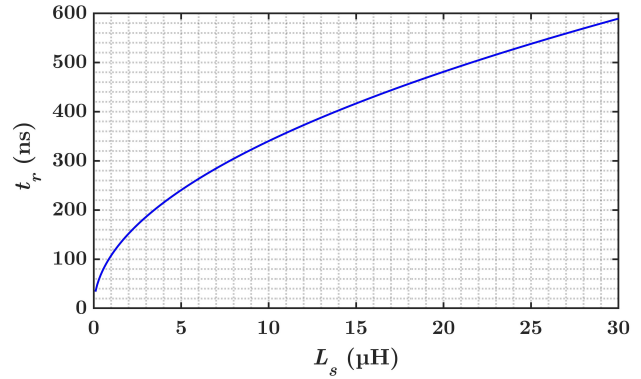


Fig. 10. Variation of t_r with L_s .

IV. CONCLUSION

2L-SP topology can alleviate the increased losses and CM EMI emission incurred in standard 2L topology with WBG devices, switching at high frequency. Split inductors lower the rise and fall profile of the AC output node and complementary switching cell's mid-point voltage and add impedance in the CM noise path, potentially leading to lower CM emissions. This paper examines the EMI benefit of 2L-SP. A CM equivalent circuit modeling is performed in the frequency domain. It is concluded that due to the insertion of split inductors, the mid-point voltages of P and N-cell have different rise and fall profiles, resulting in two CM voltage sources in the CM equivalent model. This is contrary to the simple 2L inverter topology, which has one CM voltage source, as proposed in the existing literature. Further, a comparative study of CM emission of 2L-SP and 2L three-phase inverter on a hardware prototype for different values of split inductance is performed. The results show that increasing split inductance impacts the high-frequency spectrum and shifts the resonance points to the left due to interaction between the split inductors and ground parasitic capacitances.

ACKNOWLEDGMENT

This work was supported by Oak Ridge National Laboratory (ORNL) funded through the Department of Energy (DOE) - Office of Electricity's (OE), Transformer Resilience and Advanced Components (TRAC) program led by the program manager Andre Pereira. The authors would also like to acknowledge the Office of Naval Research (Project F2-20) and the National Science Foundation (NSF Award No. 1846917) for lending financial support for this work.

REFERENCES

- [1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014.
- [2] D. Han, W. Lee, S. Li, and B. Sarlioglu, "Comparative performance evaluation of common mode voltage reduction three-phase inverter topologies," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2625–2629.
- [3] M. L. Heldwein and J. W. Kolar, "Impact of emc filters on the power density of modern three-phase pwm converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1577–1588, 2009.
- [4] H. Kim, A. Anurag, S. Acharya, and S. Bhattacharya, "Analytical study of sic mosfet based inverter output dv/dt mitigation and loss comparison with a passive dv/dt filter for high frequency motor drive applications," *IEEE Access*, vol. 9, pp. 15 228–15 238, 2021.
- [5] S. S. Vala, A. B. Mirza, and F. Luo, "A review on partial discharge phenomenon in rotating machines operated using wbg motor drives," in *2022 IEEE Transportation Electrification Conference Expo (ITEC)*, 2022, pp. 523–528.
- [6] S. S. Vala, K. Choksi, A. B. Mirza, and F. Luo, "Exploring interactions between reflected wave and partial discharge in wbg motor drives," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, pp. 1–5.
- [7] S. Li, "Packaging design of igbt power module using novel switching cells," Ph.D. dissertation, 2011.
- [8] Q. Yan, X. Yuan, Y. Geng, A. Charalambous, and X. Wu, "Performance evaluation of split output converters with sic mosfets and sic schottky diodes," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 406–422, 2017.
- [9] F. Yang, Z. Wang, Z. Zhang, S. L. Campbell, and F. Wang, "Analysis and experimental evaluation of middle-point inductance's effect on switching transients for multiple-chip power module package," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6613–6627, 2019.
- [10] H. Li, S. Munk-Nielsen, S. Beczkowski, and X. Wang, "Sic mosfets based split output half bridge inverter: Current commutation mechanism and efficiency analysis," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 1581–1588.
- [11] A. B. Mirza, A. I. Emon, S. S. Vala, and F. Luo, "A comprehensive analysis of current spikes in a split-phase inverter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1580–1585.
- [12] Q. Liu, W. Shen, F. Wang, D. Boroyevich, V. Stefanovic, and M. Arpilliere, "Experimental evaluation of igbts for characterizing and modeling conducted emi emission in pwm inverters," in *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, vol. 4, 2003, pp. 1951–1956 vol.4.
- [13] J.-S. Lai, X. Huang, E. Pepa, S. Chen, and T. Nehl, "Inverter emi modeling and simulation methodologies," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 3, pp. 736–744, 2006.
- [14] H. Zhang, L. Yang, S. Wang, and J. Puukko, "Common-mode emi noise modeling and reduction with balance technique for three-level neutral point clamped topology," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7563–7573, 2017.
- [15] M. Mahmoudian, M. Gitizadeh, A. H. Rajaei, and V. M. Tehrani, "Common mode voltage suppression in three-phase voltage source inverters with dynamic load," *IET Power Electronics*, vol. 12, no. 12, pp. 3141–3148, 2019. [Online]. Available: <https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-pel.2018.6290>
- [16] C. T. Morris, D. Han, and B. Sarlioglu, "Reduction of common mode voltage and conducted emi through three-phase inverter topology," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1720–1724, 2017.
- [17] A. B. Mirza, A. I. Emon, K. Choksi, S. S. Vala, F. Luo, R. K. Moorthy, and M. S. Chinthavali, "Hardware design and implementation of a 75 kva 3-d integrated intelligent power stage," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023.
- [18] M. Didat, C. D. New, S. Choi, and A. Lemmon, "Improved methodology for conducted emi assessment of wide band-gap power electronics," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 731–740, 2022.
- [19] D.-W. Lee, H.-S. Youn, and J.-K. Kim, "Development of phase shift full bridge converter with integrated winding planar two transformer for ldc," *IEEE Transactions on Transportation Electrification*, pp. 1–1, 2022.
- [20] "Spellman st 12kw high voltage power supplies." [Online]. Available: <https://www.spellmanhv.com/en/high-voltage-power-supplies/ST>
- [21] "2 ways power splitter, 0.002 - 60 mhz." [Online]. Available: <https://www.minicircuits.com/WebStore/dashboard.html?model=ZSC-2-2%2B>
- [22] J. E. D. B. Å. Wisten, S. Niska and J. Delsing, "Experimental investigation of em noise environment surrounding detector systems in swedish railways," *IEE Proceedings - Electric Power Applications*, vol. 153, pp. 191–196(5), March 2006.