

A Figure of Merit for SiC MOSFET Power Modules to Achieve High-Power-Density Energy Conversion

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Abstract—Power modules are the core components for energy conversion in motor drive, renewable energy application, and battery electric vehicle (EV) and have a significant impact on system performance and reliability. A variety of packaging structures are proposed for a number of applications, and however, there is no clear guideline for their performance comparison. To help in selection of wide bandgap MOSFET-based power modules for high-power-density energy conversion system, a new power module figure of merit (PMFOM) is proposed in this article. The PMFOM is derived based on device switching behavior, considering the conduction and switching loss, parasitics from package layout, thermal resistance, and package area. Finally, the validation of the proposed PMFOM is verified with a practical design example using commercially available 1.2-kV power modules.

Index Terms—Figure of merit (FOM), high-power-density design, power converter, power module.

I. INTRODUCTION

TO ACHIEVE carbon neutrality and to fight global warming, automotive and aviation industry is focused on shifting from traditional internal combustion engine toward more electrified future [1]. Inclusion of distributed greener energy resources into modern power grids is becoming a commonplace. Power electronics converters are at the heart of these efforts. The size of these converters is dominated by the cooling arrangement and the size of passive filter requirements. Power converters comprised of power devices operating at higher efficiency and increased switching frequency often require smaller heatsinks and lesser filtering

components [2]. Selection of power devices for high-density power converters requires careful consideration as different device characteristics may lead to conflicting outcomes. For example, power devices with larger footprints often have lower conduction loss but higher switching loss, restricting high-frequency operation [3]. Model-based optimization and simulation-aided paper-based designs are often used by designers to choose the ideal device for the specific converter with the highest achievable power density [4]. An alternative and popular approach for device selection is based on device figure of merit (FOM). FOM for semiconductor devices or materials indicates their performance limit and is often used as a tool to compare among a pool of options [5].

For high-power applications, multiple power devices are often packaged together as power modules, and its outline is tailored for specific applications. The layout and packaging technology largely influences the performance of the power devices housed inside the module [6]. For example, stray inductances and capacitance from package layout and interconnect technologies influence the switching characteristics and impact the switching loss. Equivalent junction-to-case thermal resistance is also determined by material selection and layout of the power module. There have been many materials and device FOM (D-FOM) developed; however, no FOM is dedicatedly developed for power modules. Since the performance of an individual semiconductor device significantly relies on its packaging technology, extended FOM linking package parameters with the device parameter would be more pertinent in modern power electronics applications.

This article proposes an extended version of FOM combining the device behavior and package parameters that will aid to down select a power module package to deliver maximum power density and efficiency. The FOM is derived based on device theory and switching characteristics that would help in power module selection for efficient high-power-density converter design. The proposed FOM is applied on several commercially available 1.2-kV power modules and results are compared and verified for a converter design. Its validity for other voltage classes is subject to further verification.

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TABLE I
SEMICONDUCTOR MATERIAL FOM REVIEW

Figure of Merit	Definition	Related Physical Entity	Significance
JFOM [7]	$\frac{E_c v_s}{2\pi}$	Critical electric field (E_c) and saturated drift velocity (v_s)	Relates operating frequency and power gain of the transistor
KFOM [8]	$\frac{\lambda c v_s}{4\pi \epsilon_r}$	Thermal conductivity (λ), saturated drift velocity (v_s), speed of light (c), and relative permittivity (ϵ_r)	Thermal limitation on transistors switching speed
BFOM [9]	$\epsilon \mu E_g^3$	Permittivity (ϵ), mobility (μ), and bandgap energy (E_g)	Compares conduction loss
HMFOM [10]	$E_c \sqrt{\mu}$	Critical electric field (E_c) and mobility (μ)	Compares total loss (both conduction and switching) for different materials
HCAFOM [10]	$\epsilon E_c^2 \sqrt{\mu}$	Permittivity (ϵ), critical electric field (E_c), and mobility (μ)	Chip area comparison for similar operating condition for different materials
HTFOM [10]	$\frac{\sigma_{th}}{\epsilon E_c}$	Thermal conductivity (σ_{th}), permittivity (ϵ), and critical electric field (E_c)	Thermal comparison for different materials when chip area and losses are optimized

TABLE II
SEMICONDUCTOR D-FOM REVIEW

Figure of Merit	Definition	Physical entity related	Significance
BHFOM [3]	$\frac{1}{R_{On,sp} C_{in,sp}}$	Specific on resistance ($R_{On,sp}$) and input capacitance ($C_{in,sp}$)	Compares conduction loss and switching loss (dominated by input capacitance)
NHFOM [11]	$\frac{1}{R_{On,sp} C_{oss,sp}}$	Specific on resistance ($R_{On,sp}$) and output capacitance ($C_{in,sp}$)	Compares conduction loss and switching loss (dominated by output capacitance)
HDFOM [10]	$\sqrt{R_{On} Q_{GD}}$	On resistance (R_{On}) and miller charge (Q_{GD})	Compares conduction loss and switching loss (represented by gate to drain charge)
PDFOM [12]	$\frac{1}{\sqrt{R_{On} Q_{GD} A_{pack} R_{th}}}$	On resistance (R_{On}) and miller charge (Q_{GD}), package area (A_{pack}) and thermal resistance (R_{th})	High power density FOM, relating power loss with package thermal parameter

II. REVIEW OF EXISTING FOM FOR POWER DEVICES

The performance of the power devices is primarily determined by the semiconductor materials. Several FOMs are derived so far demonstrating impact of the semiconductor material on the performance of MOSFETs. Material-based FOM (M-FOM) compares the material properties and has defined the path for research, development, and commercialization of new material-based power semiconductor devices such as SiC and GaN.

Johnson [7] proposed an M-FOM for transistors based on the material property (Table I). Here, it has been shown that the product of E_c (critical electric field for breakdown in semiconductor) and v_s (saturated drift velocity of the carrier) is the ultimate measure of a transistor's volt-ampere, power gain, and frequency performance. In 1972, Keyes [8] proposed a new M-FOM, incorporating thermal consideration, λ (thermal conductivity). He asserted that the thermal property sets a limitation on the speed of the semiconductor logic devices. Later, Baliga [9] proposed an M-FOM, which concentrates on material parameters that contribute to the conduction loss in power FETs. The limitation of this FOM is the assumption that the power losses are solely contributed by the conduction loss. Thus, it can only be applied to systems operating at lower frequencies where the conduction losses are dominant. This FOM relates E_g (bandgap energy), ϵ (permittivity), and μ (mobility) of the semiconductor materials. Huang [10] proposed several M-FOMs concentrating on different aspects of unipolar devices in recent times. Huang's material FOM (HMFOM) considers both switching and conduction losses and is expressed in terms of E_c and μ .

Subsequently, a chip area FOM (HCAFOM) and thermal FOM (HTFOM) are also provided based on material characteristics [10]. The expression of all these material FOMs is listed in Table II.

However, device structure and manufacturing process also influence the performance of the transistors. Combining M-FOM with process technology results in D-FOM that is usually expressed using higher level device parameters such as conduction resistance, gate charge, equivalent input and output capacitance, and thermal resistance. Baliga [3] proposed a D-FOM in 1989 considering both conduction and switching losses. Baliga used specific input capacitance to represent the switching loss, considering that switching loss is due to the charging and discharging of it. However, in the practical application of power MOSFETs with inductive or capacitive load, the output capacitance of the device contributes more to the switching loss compared to the input capacitance. Considering it, Il-Jung et al. [11] proposed new high-frequency D-FOM, relating conduction resistance and output capacitance of the device. In 2004, Huang [10] provided D-FOM for unipolar devices (JFET, MOSFET, and MESFET). It relates the switching loss to the gate charge waveform, and the D-FOM is a relation between conduction resistance and Miller charge. All these D-FOMs for power devices are from efficiency or loss point of view but do not consider any package parameter. Wang et al. [12] incorporated the package thermal resistance and area with power loss and derived a power density FOM (PDFOM) in 2008; however, it does not consider any impact of layout parameters on device operation. The expression of all these D-FOMs is listed in Table III.

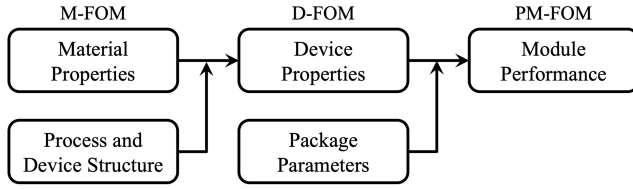


Fig. 1. PMFOM derivation combining material and device property.

To improve the switching performance of WBG devices to deliver efficient and high-density power conversion, layout and packaging technologies of power modules are of utmost importance. This work proposes a unified FOM for power module FOM (PMFOM) combining the device parameters and package parameters. It is focused on high efficiency and maximum power density; hence, the designer can be benefited by choosing the right power module for their application.

III. DERIVATION OF NEW PMFOM

Power module package is all about efficient and reliable utilization of semiconductor chips; therefore, the device loss is considered a critical parameter while deriving the new PMFOM. The process of obtaining PMFOM by combining D-FOM with package parameters is shown in Fig. 1. To determine the D-FOM, both conduction loss and switching loss of the semiconductor dies need to be considered. When a die comes with large area, the conduction resistance usually decreases, but it often leads to increased input and output capacitances, resulting in higher switching loss. On the contrary, a smaller die area would come with higher conduction and thermal resistance. To determine the D-FOM, it is more accurate to link the switching loss to the gate charge waveform instead of parasitic capacitances (C_{GS} , C_{GD} , and C_{DS}), as these capacitances are not constant [12]. Here, the device is assumed as ideal during loss calculation for the simplification and several factors, such as reverse recovery loss from body diodes during dead time operation, are not considered.

Determination of conduction loss is straightforward compared to switching loss, as it depends on current and the conduction resistance of the device. Switching loss determination requires careful observation of switching characteristics of the device. The ideal turn-on and turn-off process of a unipolar device (MOSFET and JFET) is shown in Fig. 2. Here, V_D is the switching voltage, I_D is the switching current, Q_{GS} and Q_{GD} are gate charges at switching intervals, t_{CR} and t_{VR} are current and voltage rise time, and t_{CF} and t_{VF} are current and voltage fall time during switching transition. Switching loss is also dependent on the gate resistance (R_G) and current supplied by the driver. For simplicity, we are considering that average gate current supplied by the driver is $i_{g(av)}$, in the arrangement shown in Fig. 3. It is evident from the waveform of V_D and I_D that the switching loss is comprised of loss during voltage transition (P_{vt}) and loss during the current transition (P_{ct}). For example, during turn on, the loss due to device switching action for a switching frequency f_{sw} can be determined by the following equation:

$$P_{sw(ON)} = P_{ct(ON)} + P_{vt(ON)}. \quad (1)$$

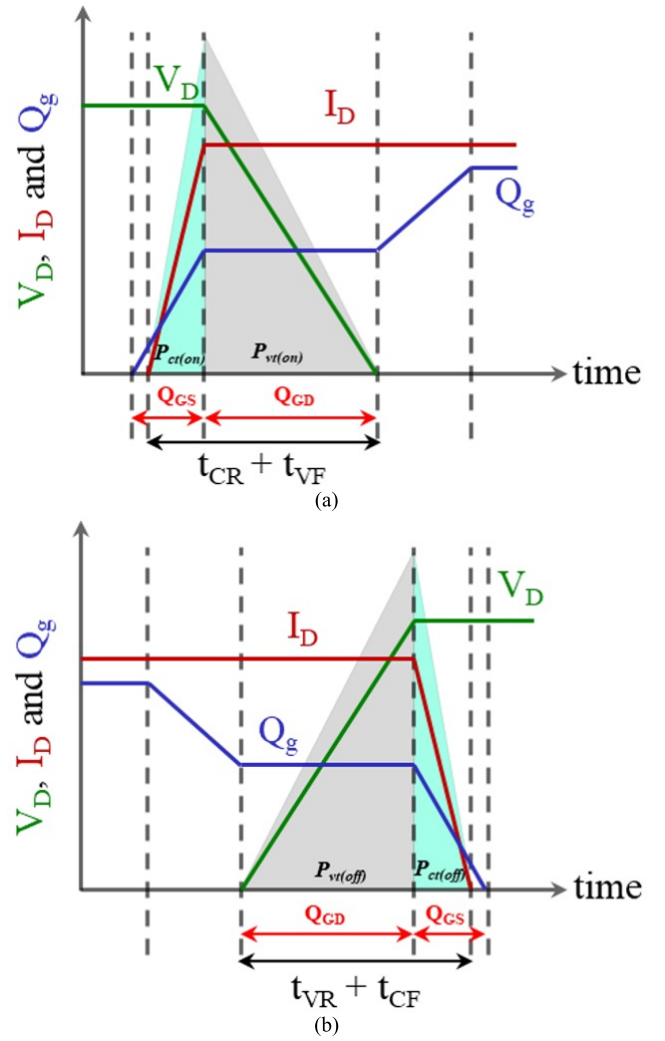


Fig. 2. Switching transition of MOSFET. (a) Turn-on transition of MOSFET. (b) Turn-off transition of MOSFET.

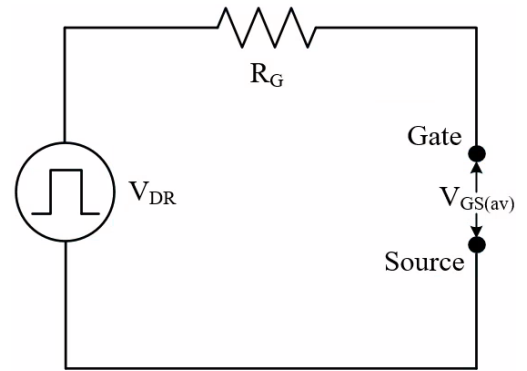


Fig. 3. Simplified arrangement to drive power MOSFET.

The power loss during the current transition when the device is turning on can be calculated as shown in the following equation, where t_{CR} is the current rise time estimated from Fig. 2(a):

$$P_{ct(ON)} = \frac{1}{2} V_D I_D t_{CR} f_{sw}$$

$$\begin{aligned}
&= \frac{1}{2} V_D I_D \frac{Q_{GS}}{i_{g(av)}} f_{sw} \\
&= \frac{1}{2} V_D I_D \frac{Q_{GS}}{\frac{V_{DR} - V_{GS(av)}}{R_G}} f_{sw} \\
&= \frac{1}{2} V_D I_D \frac{Q_{GS} R_G}{V_{DR} - V_{GS(av)}} f_{sw}. \quad (2)
\end{aligned}$$

Similarly, power loss during voltage transition when the device is turning on can be expressed (3), where t_{VF} is the voltage fall time estimated from Fig. 2(a). Now, we can plug these expressions in (1) and find the expression for the entire switching-ON loss, as shown in (4)

$$\begin{aligned}
P_{vt(ON)} &= \frac{1}{2} V_D I_D t_{VF} f_{sw} \\
&= \frac{1}{2} V_D I_D \frac{Q_{GD}}{i_{g(av)}} f_{sw} \\
&= \frac{1}{2} V_D I_D \frac{Q_{GD}}{\frac{V_{DR} - V_{GS(av)}}{R_G}} f_{sw} \\
&= \frac{1}{2} V_D I_D \frac{Q_{GD} R_G}{V_{DR} - V_{GS(av)}} f_{sw} \quad (3)
\end{aligned}$$

$$P_{sw(ON)} = \frac{1}{2} V_D I_D \frac{(Q_{GS} + Q_{GD}) R_G}{V_{DR} - V_{GS(av)}} f_{sw}. \quad (4)$$

The expression for switching OFF loss is also comprised of voltage and current transition loss and can be estimated from Fig. 2(b), which can be expressed as shown in (5) and (6). Equation (7) combines both current and voltage transition losses during turn off and expresses the total turn-off loss for the device. By combining (4) and (7), the total switching loss can be expressed using (8)

$$P_{vt(OFF)} = \frac{1}{2} V_D I_D \frac{Q_{GD} R_G}{V_{DR} - V_{GS(av)}} f_{sw} \quad (5)$$

$$P_{ct(OFF)} = \frac{1}{2} V_D I_D \frac{Q_{GS} R_G}{V_{DR} - V_{GS(av)}} f_{sw} \quad (6)$$

$$P_{sw(OFF)} = P_{vt(OFF)} + P_{ct(OFF)} \quad (7)$$

$$P_{sw(total)} = V_D I_D \frac{(Q_{GS} + Q_{GD}) R_G}{V_{DR} - V_{GS(av)}} f_{sw}. \quad (8)$$

When a unipolar power device operates, the total loss is a combination of conduction and switching loss, as shown in (9). Here, R_{ON} is the channel or conduction resistance of the device and I_{RMS} is the rms value of channel current. Loss associated with the nonideality/linearity and parasitic is neglected for the sake of simplicity:

$$\begin{aligned}
P_{loss(total)} &= P_{cond} + P_{sw(total)} \\
&= I_{rms}^2 R_{ON} + V_D I_D \frac{(Q_{GS} + Q_{GD}) R_G}{V_{DR} - V_{GS(av)}} f_{sw} \quad (9)
\end{aligned}$$

$$= I_{rms}^2 \frac{R_{ON(sp)}}{A_{die}} + V_D I_D \frac{(Q_{GS(sp)} + Q_{GD(sp)}) R_G A_{die}}{V_{DR} - V_{GS(av)}} f_{sw}. \quad (10)$$

The conduction resistance and gate charges are substituted with specific conduction resistance and specific gate charges in (10), as shown in [3]. During bare die manufacturing, die area (A_{die}) is often optimized to achieve a minimum power loss. The optimum die area, which will provide minimum

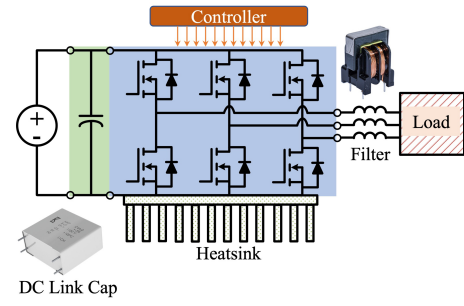


Fig. 4. Configuration of the inverter and its components.

power loss, can be found by setting $dP_{loss(total)}/dA_{die}$ equal to 0. The expression for optimized die area for a power device [$A_{die(opt)}$] is shown in (11). The value of $A_{die(opt)}$ from (11) can be plugged in (10) to find the minimum power loss [$P_{loss(total,min)}$] for a bare die of power MOSFET. The expression for $P_{loss(total,min)}$ is shown in (12)

$$A_{die(opt)} = I_{rms} \sqrt{\frac{R_{ON(sp)} (V_{DR} - V_{GS(av)})}{V_D I_D (Q_{GS(sp)} + Q_{GD(sp)}) R_G f_{sw}}} \quad (11)$$

$$\begin{aligned}
P_{loss(total,min)} &= 2 I_{rms} \sqrt{\frac{V_D I_D R_G f_{sw}}{(V_{DR} - V_{GS(av)})}} \\
&\quad \times \sqrt{R_{ON} (Q_{GD} + Q_{GS})} \\
&= K_a \times \sqrt{R_{ON} (Q_{GD} + Q_{GS})}. \quad (12)
\end{aligned}$$

In (12), only R_{ON} and $(Q_{GD} + Q_{GS})$ are the device parameters, and the rest are related to the operating condition/mission profile and are represented using K_a . The power conversion stage designed with power device with lower total loss will be more efficient. Hence, the preliminary D-FOM for our case is inversely proportional to $(R_{ON} (Q_{GD} + Q_{GS}))^{1/2}$.

As mentioned earlier, the device layout has a significant impact on the switching performance. Power loop inductance (L_s) is a critical parameter that causes overvoltage and voltage oscillations across device terminal during turn-off switching transition. The overvoltage across device terminal is due to switching speed (di/dt) and stray inductance, L_s . It is a customary practice to keep the % overshoot less than a certain percentage ($x\%$) of the dc-link voltage, V_D . The relationship of allowable % overshoot, stray inductance (L_s), and switching speed (di/dt) is shown in (13).

From Fig. 2, it is evident that, during the turn-off event, the current transition is from I_D to 0, and the time required for it is t_{CF} . The expression for t_{CF} can be formulated by relating gate charge and current supplied by the gate driver, as shown in (13)

$$\text{allowable \% OV} = x\% \text{ of } V_D = L_s \frac{di}{dt}$$

$$\text{Therefore, } \frac{x \times V_D}{100} = L_s \frac{I_D}{t_{CF}} \quad (13)$$

$$t_{CF} = \frac{L_s \times I_D \times 100}{x \times V_D}. \quad (14)$$

The requirement of gate resistance is relatable to the maximum allowable voltage overshoot during turn-off, as gate resistance is often employed to control the switching speed (di/dt).

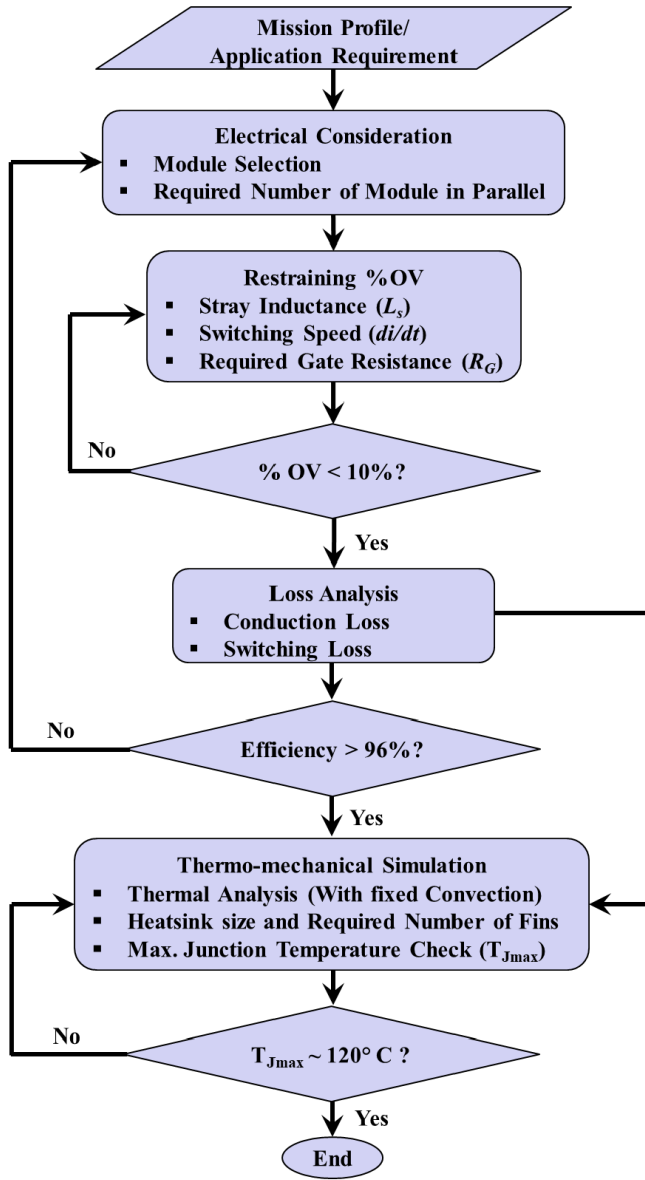


Fig. 5. Model-based multiobjective optimization design flow.

A new expression of t_{CF} can be derived from Figs. 2 and 3 relating gate resistance, gate charge, and current supplied by the gate driver and gate voltage. Here, R_G is the gate resistance, $i_{g(av)}$ is the average gate current supplied by the driver, V_{DR} is the voltage supplied by the driver, and $V_{GS(av)}$ is the average voltage appearing at the device gate

$$t_{CF} = \frac{Q_{GS}}{i_{g(av)}} = \frac{Q_{GS} \times R_G}{V_{DR} - V_{GS(av)}}. \quad (15)$$

Comparing (14) and (15), an expression to estimate the required gate resistance can be derived to keep the %OV across the device terminal to a fixed proportion of dc-link voltage, V_D

$$R_G = \frac{L_s \times I_D \times (V_{DR} - V_{GS(av)}) \times 100}{x \times Q_{GS} \times V_D}. \quad (16)$$

After we plug in the value of R_G in (12), we can find the new expression for $P_{loss(total,min)}$, as shown in (17). Here,

we have included the layout parameter L_s in the expression for total power loss for a given package.

In (17), R_{ON} , Q_{GD} , and Q_{GS} are device parameters, L_s is the package parameter, and the rest are related to the operating condition/mission profile and are represented using K_b . Therefore, the efficiency of D-FOM considering package parameter for our case is inversely proportional to $(R_{ON} \times L_s (1 + \frac{Q_{GD}}{Q_{GS}}))^{1/2}$

$$\begin{aligned} P_{loss(total,min)} &= 2I_{rms} \sqrt{\frac{I_D^2 \times L_s \times f_{sw} \times 100}{x \times Q_{GS}}} \times \sqrt{R_{ON}(Q_{GD} + Q_{GS})} \\ &= 2I_{rms} \sqrt{\frac{I_D^2 \times f_{sw} \times 100}{x}} \times \sqrt{R_{ON} \times L_s \left(1 + \frac{Q_{GD}}{Q_{GS}}\right)} \\ &= K_b \times \sqrt{R_{ON} \times L_s \left(1 + \frac{Q_{GD}}{Q_{GS}}\right)}. \end{aligned} \quad (17)$$

Power handling ability of a power module package is limited by the rise of junction temperature of the semiconductor dies inside the package. Junction temperature rise is dependent on the device loss and thermoelectrical parameter of the package. For example, in the case of a package with junction-to-case thermal resistance R_{th} and package area A_{pack} , the temperature rise (ΔT_{max}) for a specific power loss $P_{loss(total)}$ is expressed using the following equation:

$$\Delta T_{max} = P_{loss(total)} \times R_{th} \quad (18)$$

The power density of a power conversion stage will go down with high ΔT_{max} as it will require more cooling to handle certain amount of power. The power density achievable by a power module package is also inversely proportional to the package area A_{pack} . A_{pack} can be introduced to both sides of (18), as shown in (19), at the bottom of the next page, [12]. A minimum quantity of this number will yield the maximum achievable power density for a power conversion stage using a given power module package and can be realized using (20), as shown at the bottom of the next page. Here, the value of K_c is determined by the operating conditions. The rest are related to the total loss incurred during device operation considering device and package parameters, package area, and thermal resistance of the package. From (21), as shown at the bottom of the next page, we can define the PMFOM that can be used to assess multiple packages for high-density power conversion applications. A higher PMFOM indicates a more efficient power module, likely to deliver higher power density.

IV. APPLICATION OF PMFOM

Several states of the art, commercially available SiC power modules are listed in Table IV. The calculated PMFOMs for different power modules from their datasheet information result in different values, and hence, the adoption of them in power converters will have different efficiencies and power density outcomes. As shown in the expression in (21), six parameters collectively determine the PMFOM. Some modules might have higher package area thermal resistance, but its overall PMFOM can be higher than other module choices,

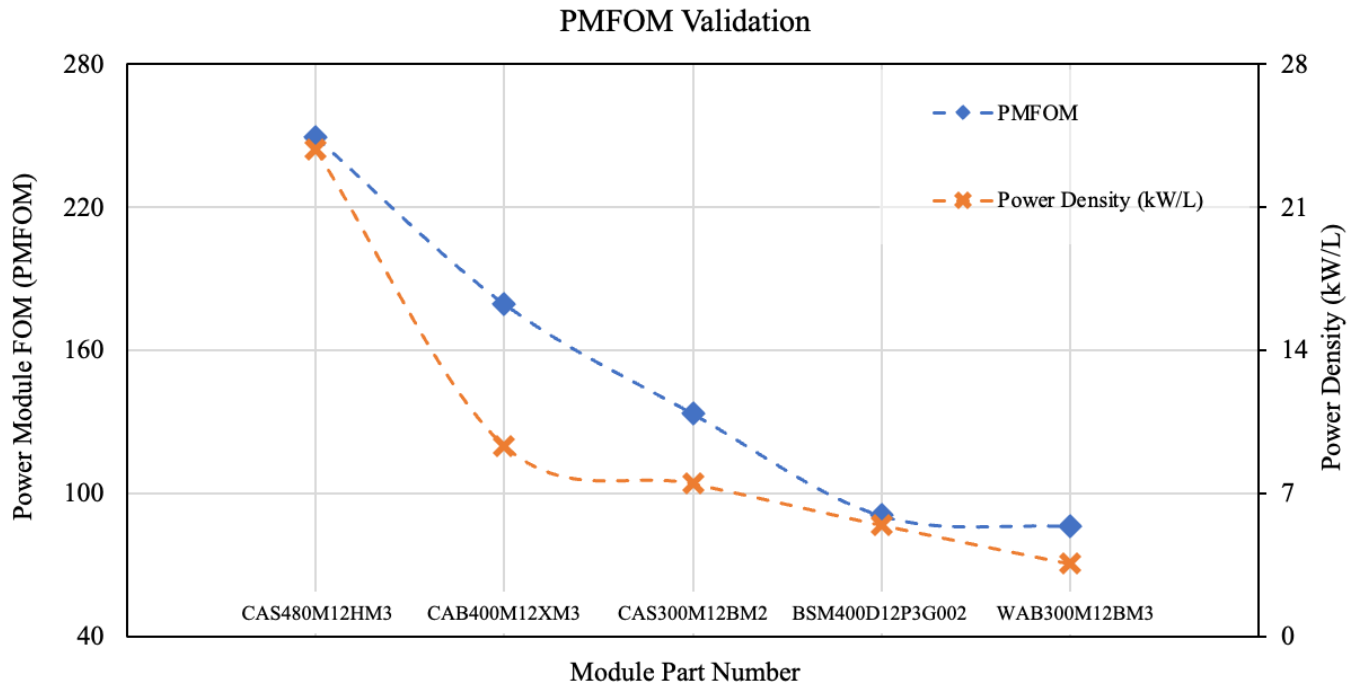


Fig. 6. PMFOM validation with practical design using model-based multiobjective optimization.

TABLE III
COMPARISON AMONG POWER MODULES USING PMFOM

Module Part No.	R_{ON} (m Ω)	L_s (nH)	Q_{GS} (nC)	Q_{GD} (nC)	R_{th} ($^{\circ}$ C/W)	A_{pack} (mm ²)	PMFOM
WAB300M12BM3	5.6	10.2	256	308	0.16	6457.5	86.3
CAS300M12BM2	6.26	11.1	166	475	0.07	6533.0	133.55
CAS480M12HM3	2.98	4.8	448	539	0.1	7150	249.27
CAB400M12XM3	5.2	6.7	256	308	0.15	4240	179.47
BSM400D12P3G002	4	10.5	400	540	0.096	9424	90.84

as shown in Table IV. Among the listed power modules, CAS480M12HM3 has the highest PMFOM value (224.8) and, therefore, should be the best candidate to choose for a high-density design.

To validate the suggestions provided by the proposed PMFOM, a three-phase, two-level voltage source inverter design is carried out using the listed power modules.

Fig. 4 shows the topology and associated components in the design.

Design of a power conversion stage is always a trade-off among efficiency, power density, weight, and cost. For instance, considering the system-level operation of the inverter, for a given topology, and mission profile (voltage and current rating), increased switching frequency will result in a reduced

$$\begin{aligned} \Delta T_{\max} \times A_{\text{pack}} &= P_{\text{loss}(\text{total})} \times R_{\text{th}} \times A_{\text{pack}} \\ (\Delta T_{\max} \times A_{\text{pack}})_{\min} &= P_{\text{loss}(\text{total}, \min)} \times R_{\text{th}} \times A_{\text{pack}} \end{aligned} \quad (19)$$

$$\begin{aligned} &= 2I_{\text{rms}} \sqrt{\frac{I_D^2 \times f_{\text{sw}} \times 100}{x}} \times \sqrt{R_{\text{ON}} \times L_s \left(1 + \frac{Q_{\text{GD}}}{Q_{\text{GS}}}\right)} \times R_{\text{th}} \times A_{\text{pack}} \\ &= K_c \sqrt{R_{\text{ON}} \times L_s \left(1 + \frac{Q_{\text{GD}}}{Q_{\text{GS}}}\right)} \times R_{\text{th}} \times A_{\text{pack}} \end{aligned} \quad (20)$$

$$\text{PMFOM} = \frac{1}{\sqrt{R_{\text{ON}} \times L_s \left(1 + \frac{Q_{\text{GD}}}{Q_{\text{GS}}}\right)} \times R_{\text{th}} \times A_{\text{pack}}} \quad (21)$$

TABLE IV
POWER DENSITY ESTIMATION OF 100-kW INVERTER

Design parameters	Module Part No.				
	WAB300M12BM3	CAS300M12BM2	CAS480M12HM3	CAB400M12XM3	BSM400D12P3G002
Rated Power (kW)	100	100	100	100	100
Number of Module	3	3	3	3	3
Switching Frequency (kHz)	70	70	70	70	70
Conduction Loss/Module (W)	265.85	406.45	123.31	166.4	503.89
Switching Loss/Module (W)	648.93	973.343	491.606	610.5	681.37
Heatsink Thermal Resistance ($^{\circ}\text{C}/\text{W}$)	0.0481	0.0677	0.2091	0.0948	0.0477
Junction Temperature ($^{\circ}\text{C}$)	120.18	120.05	120.03	120.08	120.06
Required Number of Fins	249	108	21	110	108
Heatsink and Module Volume (L)	26.08	11.37	2.20	2.85	16.35
Filter and Auxiliary Volume (L)	2	2	2	2	2
Entire Inverter Volume (L)	28.08	13.37	4.20	4.85	18.35
Power Density (kW/L)	3.56	7.48	23.81	9.33	5.45

volume and weight of passive components, such as the dc-link capacitor and passive output filters. However, the increased switching frequency will curtail the efficiency due to the increased switching loss and will require a higher volume of the heatsink [13], [14], [15]. To achieve the optimum design to fulfill the requirements of efficiency, power density, weight, temperature rise, and cost, it is necessary to closely observe the tradeoff among these parameters. Model-based multiobjective optimization is proved to be useful for tradeoff study and its accuracy to estimate the power density [15]; therefore, it is followed during the design of our destined power inverter. This optimization code uses the MATLAB platform and more information regarding it is available in [2] and [15].

The power rating and the switching frequency for the design were fixed at 100 kW and 70 kHz, respectively. To have an apple-to-apple comparison between the power stages with different choices of power module, first, the design goal is set as the allowed %OV was fixed to <10% of applied dc-link voltage. This design objective is ensured by varying the gate resistance.

To determine the efficiency of the designed power stage, device loss evaluation is required. The device loss is calculated based on the datasheet information. As these power modules come with dissimilar device and package parameters, the calculated power loss will be different. The second design goal was set to keep the efficiency >96%.

Now, the device power loss in conjunction with thermal resistance dictates the junction temperature of power devices, and it is supposed to be nonidentical across our five separate designs if the heat extraction/cooling solution is not tuned

accordingly. Keeping the max junction temperature constant of all five designs is the third design goal. To keep the junction temperature for the device's constant across all the designs, the cooling arrangement was adjusted. The maximum junction temperature rise for the devices in each design was kept around 120 $^{\circ}\text{C}$. Traditional rectangular finned heatsink made of aluminum was considered as the cooling solution. The fin width (3 mm), the distance between the fins (7 mm), and the height of the heatsink (75 mm) were kept constant in all the five designs. The dimension of heatsink and fin numbers is varied from design to design to achieve the design goal. The design flow is shown in Fig. 5. As the power rating and switching frequency is kept constant at 100 kW and 70 kHz, respectively, the required dc-link cap and harmonic filter volume did not change from design to design. The volume of the designs in our case is majorly dependent on the module dimension, loss number, and cooling requirement.

Table IV lists all the design variables for inverter using five different modules. During the estimation of heatsink size, the convection coefficient (h) was set to 20 $\text{W}\cdot\text{m}^{-2}\cdot\text{K}^{-1}$ for all the designs. CAS480M12HM3 shows the maximum power density of 23.81 kW/L, while WAB300M12BM3 achieves the lowest power density of 3.56 kW/L. These power density numbers are obtained from model-based multiobjective optimization using the MATLAB platform. During this calculation, we have considered high conductivity thermal interface material (TIM), SARCON GR80A 0.5T for all the cases presented.

Finally, the calculated power density for the two-level voltage source inverter using the power modules under

consideration is compared with the values obtained using PMFOM in Fig. 6. The trend of power density orders matches with the prediction provided by the proposed PMFOM.

V. CONCLUSION

In this article, a new PMFOM is developed and verified, which can be utilized to compare among the power module candidates housing unipolar devices of same voltage rating for designing energy conversion system with a focus on achieving higher efficiency and power density. The FOM is derived based on parameters impacting device power loss, stray inductance from module layout, thermal resistance, and package area. All the parameters used to construct PMFOM are easily achievable by reading the datasheet, and this PMFOM can be used as a handy tool for design engineers. The behavior of the body diode and antiparallel freewheeling diode is not considered in the proposed FOM. Further work is required here.

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