A Double-Sided Cooled Split-Phase SiC Power Module With Fuzz Button Interposer

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***Abstract*— Power modules are the core components of the powertrain of hybrid and battery electric vehicle (EV) and has a significant impact on system performance and reliability. Conventional single-sided cooled (SSC) wire-bonded power modules have limitation to utilize the benefits offered by new generations of silicon carbide (SiC) devices due to higher parasitic inductance and heat dissipation issues. Planar, low-profile, and double-sided cooled (DSC) power modules are emerging in inverters of EV powertrain to address the limitations of conventional SSC modules. However, there is a reliability concern introduced by the rigid interconnection between the device chips and two substrates of the DSC power module. In this article, the design and development of a DSC, 1200-V/150-A SiC half-bridge split-phase power module have been presented, where flexible compressible pins called "fuzz buttons" are used in a low-profile printed circuit board (PCB) to realize die top-side connection. Our simulation result shows a 45% reduction of thermomechanical stress at the interposer–dies interface with a total power loss of 1300 W (200-W/SiC MOSFET and 125-W/SiC Schottky diode). The feature of double-sided cooling helps to reduce the maximum junction temperature of the dies by 26%, compared to single-sided cooling. Moreover, the vertical commutation loop and utilization of copper layer in PCB-based fuzz button retainer board help to achieve a power loop inductance as low as 1.51 nH.**

***Index Terms*— Advanced packaging, GaN power module, high-speed switching.**

I. Introduction

IN THE fields of electrification of the transportation sector and renewable energy management, there is a growing demand for high-power-density energy conversion stages that utilize efficient and reliable power semiconductor devices [1], [2], [3], [4]. Wide bandgap devices, such as silicon carbide (SiC) and GaN, have been widely adopted to meet this demand as they can operate at higher switching frequencies and device junction temperatures compared to their Si counterparts [5], [6], [7]. To fully benefit from these advanced semiconductor devices, improved and advanced packaging structures and interconnect technologies are necessary. Furthermore, the demanding operating conditions in certain applications, such as electric vehicles (EVs), which involve vibration, humidity, and high temperatures, have presented notable obstacles in the packaging of power modules. The design of packaging structures, materials used, and mission profiles play a crucial role in determining the thermal, electrical, mechanical performance, and reliability of these modules, as highlighted in previous studies [8], [9]. The conventional power module packages are single-sided cooled (SSC) and wire-bonded structure, where the top side of the power semiconductor devices/dies is utilized for electrical connections using wire bonds, while the bottom side is typically attached to a metallized insulating substrate to conduct current and facilitate heat dissipation.

The standard interconnection approach for power modules has traditionally relied on wire bonding due to its ease of use, established maturity, and cost-effectiveness. However, wire bonding remains a weak point in terms of power module reliability, with failure modes such as bond wire liftoff and heel cracks resulting from thermomechanical stress during operation and power/thermal cycling [10]. In addition, wire bonding introduces challenges such as increased power loop inductance (L_{Stray}) ranging from 15 to 20 nH [12], leading to issues such as significant voltage overshoot [13], [14], high switching loss under high-frequency switching operation, and voltage oscillation resulting in electromagnetic interference (EMI) [15]. It also limits heat dissipation from the top side of power semiconductor devices, resulting in elevated thermal resistance (R_{th}) commonly ranging from 0.1 to 0.8 K/W [11]. Since the semiconductor device is operated up to their thermal limit by keeping the maximum junction temperature within a safe range, reduced R_{th} of the package will help to improve the power handling capacity of the dies, which will lead to reduced semiconductor footprint, smaller packaging size, and decreased material usage, thereby reducing overall costs. In this context, the utilization of double-sided cooled (DSC) modules, besides several other advantages, has been shown to significantly enhance the power density of power converters [16], [17], [18]. Enhanced thermal performance achieved through DSC can effectively reduce temperature fluctuations and thermal stress within power modules. As a result, DSC modules have demonstrated improved power cycling capability and reliability compared to SSC modules, leading to increased operational lifetime [19], [54], [55]. Researchers from both industry and academia have developed various DSC modules [20], [21], [22], [23], [24], [25], [26], [27], [28],

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[29], [30], [31], [32]. In many of these module structures, semiconductor dies are positioned between two metallized ceramic substrates, with one serving as the die attach substrate and the other for connections on the opposite side of the die with help of various interposers and interconnects. The resulting package offers improved thermal performance due to double-sided cooling. Moreover, these DSC modules typically have a smaller footprint and eliminate the need for wire bonding, resulting in lower power loop inductance compared to other designs. Nevertheless, it is worth noting that the DSC package tends to be structurally stiffer compared to the SSC wire-bonded package, which raises concerns regarding its thermomechanical reliability.

To achieve electrical connection from the top side of the dies, interconnects often come as metal brick, ball, or tube [33], [34], [35], where copper (Cu) remains the most used material. Studies [17], [36], [37], [38], [39], [40] have identified that the mismatch in coefficient of thermal expansion (CTE) between copper (Cu) and semiconductor materials, such as silicon (Si) or SiC, can result in higher levels of thermomechanical stresses at the interfaces between the dies and the interposer in DSC modules compared to wire-bonded ones. These increased stresses can potentially reduce the fatigue life of the attachment layer [55]. To address the thermomechanical reliability concerns of DSC modules, researchers have investigated the use of interposers made of molybdenum (Mo) [37], [38], [39] or Cu/Mo/Cu [40]. Mo has a CTE closer to that of semiconductor materials such Si and SiC compared to Cu, with CTE values of 4.8 ppm/K for Mo, 2.6 ppm/K for Si, and 3.7 ppm/K for SiC. However, Mo interposers require surface plating (e.g., Ti/Ni/Ag) to be compatible with soldering or silver sintering and have lower thermal conductivity compared to Cu. In a separate endeavor, a porous interposer made of low-temperature, pressure-less sintered silver was proposed, which requires pressure-assisted sintering during fabrication [41]. In addition, all these interposers necessitate a metallization layer to be attached from the top side of the dies. However, Al metallization is commonly used for SiC on the top side, which is not a good candidate for soldering or sintering. As a result, surface remetallization of the dies is required, adding additional steps and costs to the manufacturing process.

Alternatively, press-pack technologies have garnered interest due to their ability to eliminate wire bonding and soldering by utilizing pressure contact bonding for forming joints [42]. However, current press-pack approaches, such as direct pressure contacts and spring contacts, necessitate a larger die area and specialized die top-side metallization [43]. To overcome the challenges related to the specific requirements of press-packed SiC MOSFET, mentioned above, a feasible pressure contact interconnection solution using flexible and miniature press pins called "fuzz buttons" is proposed [44], [45]. These fuzz buttons are housed in a low-temperature co-fired ceramic (LTCC) interposer. However, it should be noted that LTCC has a relatively lower flexure strength (230 MPa) compared to other commonly used substrate materials such as FR4 (345 MPa), Al_2O_3 (317–345 MPa), and AlN (360 MPa) [46], making the reliability of the module a concern due to the fragility of LTCC material. Furthermore, due to the inclusion of heatsink in the power loop, the overall resulting inductance for this half-bridge module stack is 12 nH.

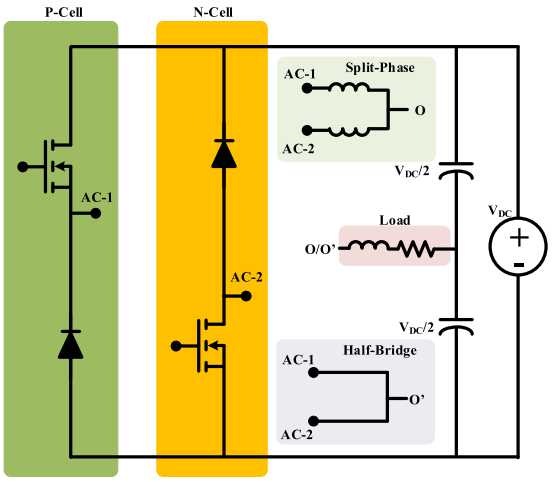

Fig. 1. Reconfigurable feature of the module as a half-bridge or split-phase topology (shown for single phase).

This article aims to propose feasible solutions for these challenges by leveraging the benefit of solderless pressure contact using fuzz button pins on the top-side interface of the dies. We have used printed circuit board (PCB) as interposer along with computer numerical control (CNC) machined copper block to house the fuzz buttons with necessary compression to establish a reliable pressure contact, which eliminates the requirement of external clamping block. Utilization of copper layer in the interposer PCB helps to form a vertical commutation loop, resulting power loop inductance as low as 1.51 nH through enhanced mutual inductance cancellation. The prototyped module shows excellent switching performance with less than 5% voltage overshoot during the turn-off at rated conditions when the recorded turn-off speed was 35 V/ns. The feature of double-sided cooling helps to reduce the maximum junction temperature of the dies by 26%, compared to single-sided cooling. The proposed module also reduces the stress at the top side of the die by 45% due to the introduction of fuzz button at dies–interposer interface. The module is laid out as a p-cell and n-cell with a provision of access to the midpoint of both the cells separately. It provides flexibility to the end users to configure the module as a half-bridge or a split-phase topology, as shown in Fig. 1. In addition to reducing switching losses, split-phase topology solves the inherent problems of traditional half-bridge-based voltage source inverter topologies, such as mistriggering and shoot-through due to crosstalk, as well as increased loss and waveform distortion due to required dead time [47], [48], [49]. In Sections II and III, we have described in detail the layout design of the module with electrical, thermal, and thermomechanical simulations to show the advantages of the DSC module with solderless pressure contact established by fuzz buttons. Then, we present the processes for fabricating the module, followed by the measurement results on the electrical performance of the module. Future work includes evaluation of these modules in applications and tests on their reliability.

II. DSC Module Layout With Fuzz Button Interconnects

A. Fuzz Buttons

The fuzz buttons are miniature interconnects made from numbers of fine strands of Au-plated beryllium copper (BeCu) wires that have been compressed into a cylindrical shape. Fuzz buttons are better interconnects compared to alternative contact technologies such as spring probes, pogo pins, hyperboloid contacts, and even soldering [61]. Fuzz button contacts demonstrate excellent durability and spring characteristics because of the high tensile strength of BeCu wire (1379 MPa). Individual fuzz buttons can survive <500 000 mating cycles when pressed with hardhat pins [51]. Fuzz buttons can retain their shape when compressed to 15%–30% without permanent deformation [52]. Due to the construction technique, the skin effect also becomes minimal. The significance of these factors becomes particularly apparent when considering requirements such as minimal signal distortion, optimal frequency response, effortless insertion, resilience to shock and vibration, lightweight design, and long-term durability [50].

The fuzz buttons are available in very small dimensions down to 10 mil in diameter and 40 mil in length. We have chosen a 20 mil diameter and 50 mil length for our application. Fuzz buttons are inserted into a grid of holes in a PCB interposer that is slightly taller than the button's length. Then, they are compressed by 16% by a specially designed CNC machined copper pillar with extrusion feature. It secures the position of fuzz button and ensures good contact with the die surface. The cross-sectional view of the interposer structure and the fuzz button layout on the diode die is shown in Fig. 2(b).

The value of self-inductance of individual fuzz button is reported to be lower than 0.19 nH. Each of them can carry 5 A of continuous current [53]. The resistance of the fuzz button depends on the compression ratio. The resistance and force versus deflection curve are shown in Fig. 3 [52]. Based on the curve with 16% deflection, the resistance is around 35 mΩ. We are using 15 fuzz buttons in each MOSFET, and hence, an additional 2.33-mΩ resistance is introduced per MOSFET dies. The SiC MOSFET die used in the prototype has an ON-state resistance of 20 mΩ at 75-A drain current and 100 °C junction temperature. The resistance introduced by the fuzz button for each die is about 11.5% of the ON-state resistance of the SiC MOSFET die.

B. Module Layout and Power Loop Optimization

Fig. 4 shows the layout design of the SiC split phase, half-bridge, double-side cooled power module using fuzz button as interconnect. The module consists of two 1.2-kV, 20-mΩ SiC MOSFETs and two 1.2-kV, 50-A Schottky diodes at each switching position. All the semiconductor chips and a 0.4-mm-thin PCB (interposer PCB-1) with grooves for the dies are directly attached to the bottom DBC. Then, the fuzz button retainer PCB (interposer PCB-2) is attached on interposer PCB-1. Fuzz buttons are placed in the plated through-hole vias located exactly on the top sides of semiconductor chip to access the contacts. Then, the fuzz buttons are pressed

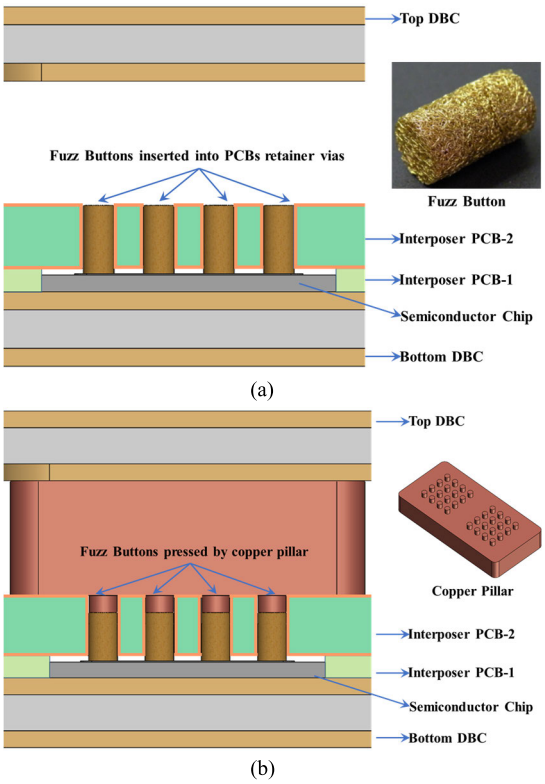

Fig. 2. Use of fuzz button to establish pressure contact from the topside of the die. (a) Fuzz button inserted in retainer PCB. (b) Fuzz button pressed and secured using copper pillar.

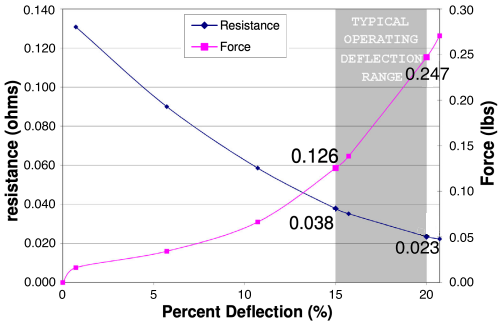

Fig. 3. Resistance and force versus deflection curve for fuzz button with 20 mil diameter [52].

using CNC machined copper pillars that have small, extruded features to go into the fuzz button holding vias. The power loop is completed by placing the top DBC and ac PCB from the top side. The overall module dimensions were 2.4 × 1.8 × 0.36 cm. All the power terminals are on one side, while the gate connectors are placed on the other side. The top view, isometric view, and exploded view of the module are shown in Fig. 4.

The half-bridge module is laid out as p-cell and n-cell. Under inductive load, current commutation happens between the top device and the bottom diode and vice versa depending on the current direction. Arrangement of power loop in p-cell and n-cell reduces the loop inductance compared to conventional antiparallel switching cell. Moreover, the midpoints of p-cell and n-cell in the designed module are not shorted

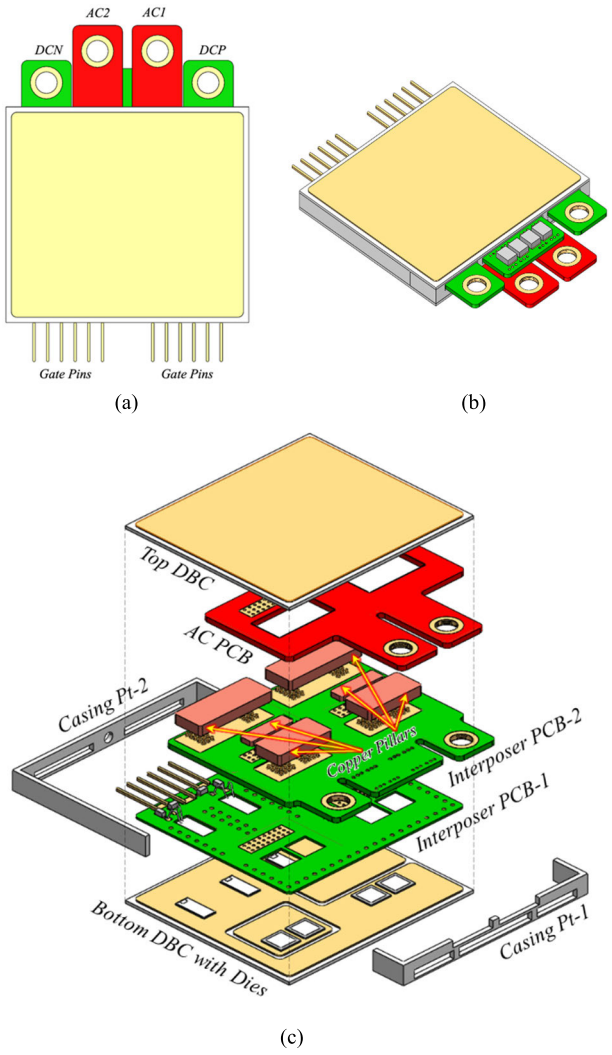

Fig. 4. Three-dimensional model of the designed DSC module. (a) Top view. (b) Isometric view. (c) Exploded view.

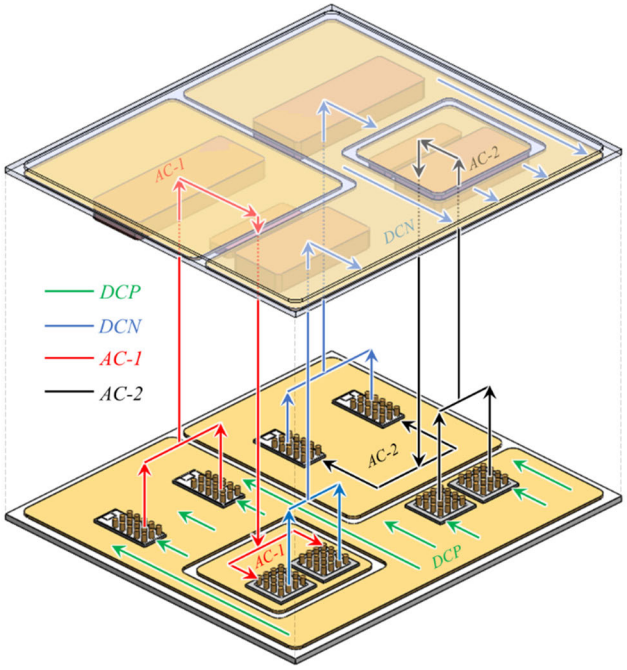

Fig. 5. Initial commutation loop in the designed module.

together internally. Midpoints can be accessed separately from outside and end user can configure the module as conventional half-bridge or split-phase topology.

The primary commutation loop is vertically spaced between the top and bottom DBCs. The power loop inductance was extracted using Ansys Q3D and the result is 5.6 nH for both p-cell and n-cell separately. The commutation loop is shown in Fig. 5. The reduction of power loop inductance in the vertical commutation loop is dependent on the mutual cancellation of magnetic flux. The mutual cancellation of magnetic flux between top and bottom DBCs is weak due to the added distance by the copper pillars. To further improve the coupling, 04 copper layer of the fuzz button retainer PCB (interposer PCB-2) is utilized. Current is flown in the opposite direction in adjacent layers in that PCB, as shown in Fig. 6.

As the distance between copper layers inside PCBs is relatively smaller, the coupling can be enhanced greatly. Moreover, the placement of ceramic decoupling capacitor in the same PCB reduces the size of the power loop. This arrangement reduces the power loop inductance as low as 1.51 and 1.56 nH for p-cell and n-cell, respectively. In the Q3D simulation, the solution frequency was set to 100 MHz, and the source and sink are assigned to the pads of decoupling capacitors. The final power loop inductance network with self-inductances and coupling coefficients is shown in Fig. 7. The process of total power loop inductance for p-cell is deduced using the following equations. Power loop inductance for n-cell can be calculated in a similar way

$$L_{\text{pcell}} = (4.7{+}1.7{+}2.94)\text{nH} + 2\left(M_{\text{p-n}} + M_{\text{p-ac1}} + M_{\text{ac1-n}}\right) \tag{1}$$

$$M_{\text{p-n}} = K_{\text{p-n}}\sqrt{4.7 \times 2.94}\ \text{nH} \tag{2}$$

$$M_{\text{p-ac1}} = K_{\text{p-ac1}}\sqrt{4.7 \times 1.7}\ \text{nH} \tag{3}$$

$$M_{\text{ac1-n}} = K_{\text{ac1-n}}\sqrt{1.7 \times 2.94}\ \text{nH}. \tag{4}$$

III. Thermomechanical Simulation and Fabrication

A. Thermal Simulation

To evaluate the thermal performance of the designed module, the finite element analysis (FEA) simulation is performed using Solidworks. To compare the performance of DSC module using fuzz button to regular DSC modules, two cases have been simulated: 1) using the designed module with fuzz button and 2) a DSC module where the extrusions of copper pillars are considered directly attached to the top surface of the die. During these case studies, each of the semiconductor dies is considered as a heat source dissipating power. A parametric sweep has been performed where power loss per die is varied from 20 to 300 W with a step of 20 W, at a bulk ambient temperature of 298.15 K. The convection coefficient for forced liquid cooling ranges between 100 and 15 000 W/m^{2}K [56]. Since all semiconductor dies are attached to the bottom substrate, for single-sided cooling, we have

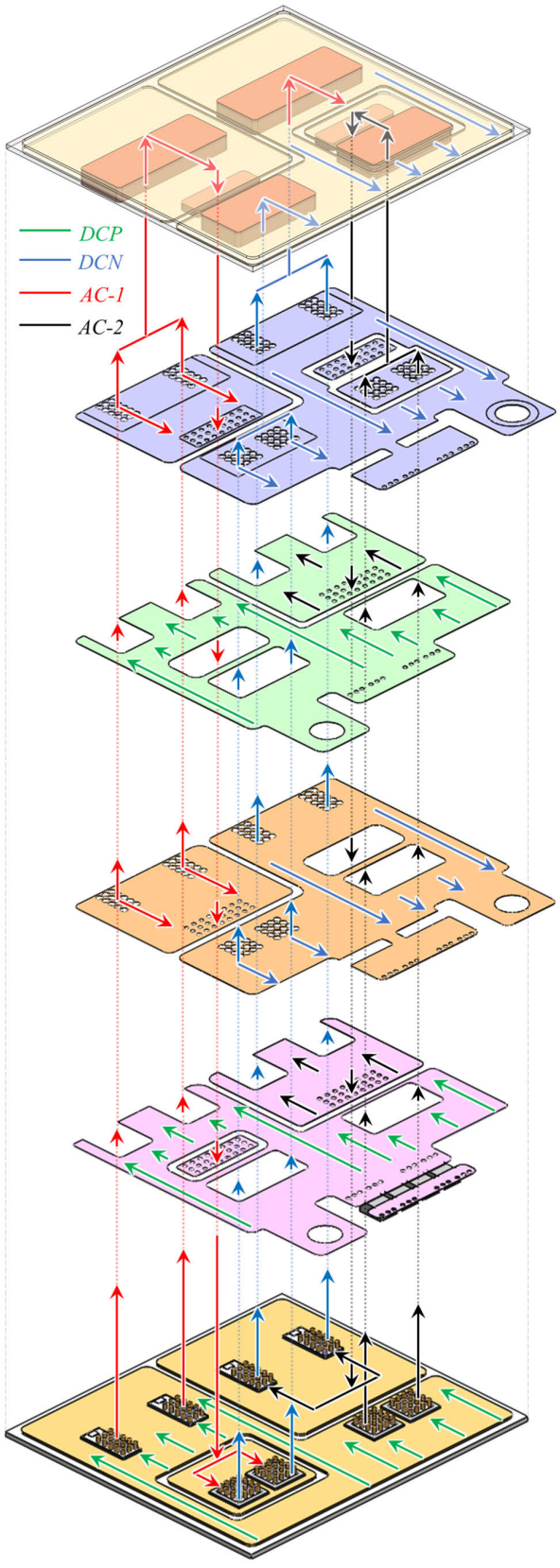

Fig. 6. Improved commutation loop utilizing the copper layers in interposer PCB.

applied a convection coefficient of 10 000 W/m^{2}K at the bottom substrate and 20 W/m^{2}K to emulate natural airflow at the top substrate.

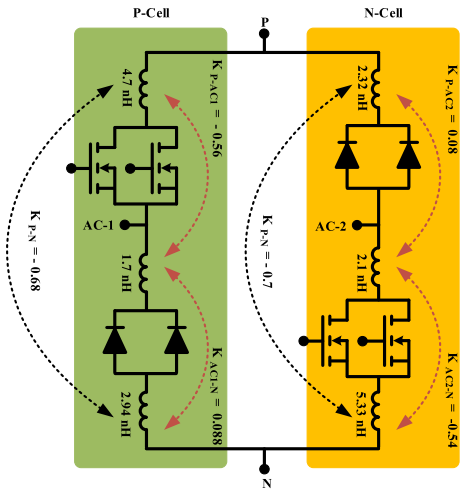

Fig. 7. Distributed inductance network of power loop in the designed module.

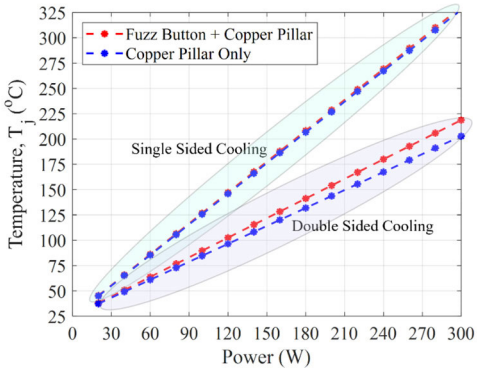

Fig. 8. Maximum junction temperature versus power loss for DSC and SSC solution with and without fuzz button.

For double-sided cooling, a convection coefficient of 10 000 W/m^{2}K was assumed at both the top and bottom substrates. It is worth mentioning that, in reality, it is tough to get good convection on both sides. It would depend on cold plate design and flow parameters. This simplified simulation establishes a baseline to compare the benefit of DSC over the SSC solution.

The simulated results of maximum device junction temperature (Tj) versus power loss are plotted in Fig. 8. A general trend of increasing Tj with power loss is visible in the plot. Although the solid copper interposer has a higher thermal conductivity (398 versus 130 W/mK) and mass density (8960 versus 2475 kg/m^3) than fuzz button, the differences in their Tj are small; less than 2% for single single-sided cooling and less than 7% for the double-sided cooling. This is because the major portion of the heat generated in the dies is dissipated through the bottom DBC, not through the interposers. However, the effect of double-side cooling is significant, and approximately 33% reduction of the junction temperature is achieved compared to the single-sided cooling solution, at 120-W power loss per die.

In another separate simulation, configuring the module as a 2-L voltage source inverter supplying 140-A rms current while operating at 70-kHz switching frequency with 800-V

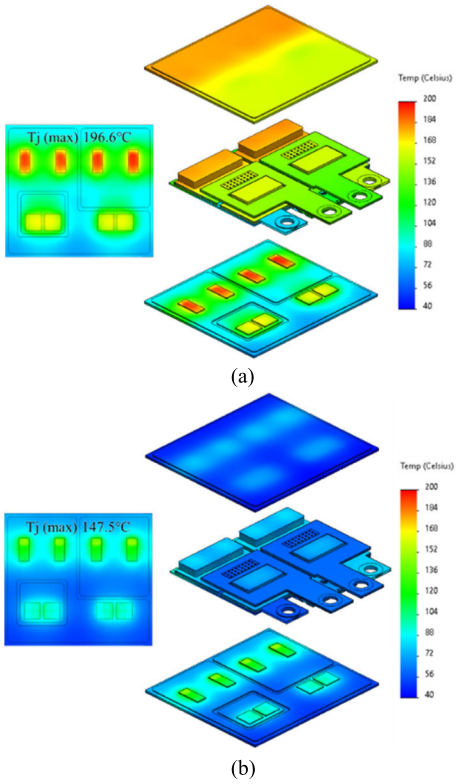

Fig. 9. Temperature distribution for DSC and SSC solution in a designed module using fuzz button. Temperature distribution in (a) SSC solution and (b) DSC solution.

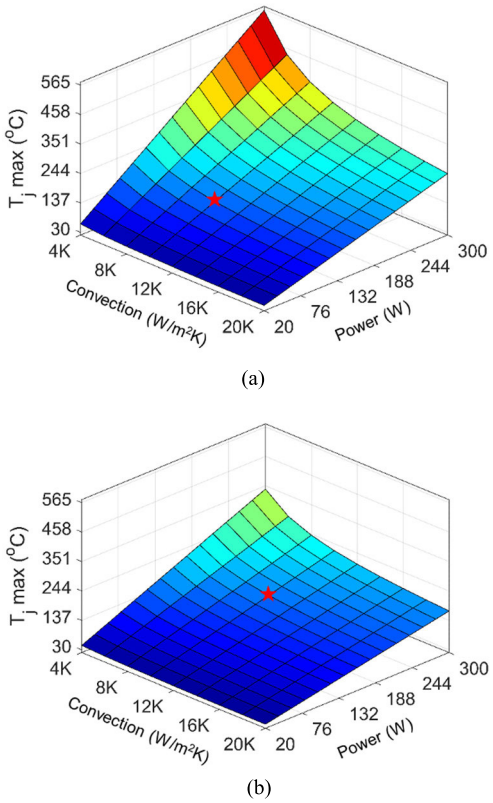

Fig. 10. Parametric analysis showing benefits of DSC solution over SSC solution. Parametric study for (a) SSC solution and (b) DSC solution.

dc link, a 200- and 125-W loss per MOSFET and diode die is calculated, respectively. Under this condition, Tj of the module with the fuzz button interposer and double-sided cooling shows a reduction of 25% (or 49.16 °C) compared to the single-sided cooling. Besides lowering the maximum junction temperature, the DSC module shows more uniform temperature distributions over the SSC solution, as shown in Fig. 9.

Finally, a parametric analysis is done by varying the convection coefficient from 4000 to 20 000 W/m^{2}K with a step of 2000 W/m^{2}K and power loss per die from 20 to 300 W with a step of 20 W. The parametric analysis compares 135 different scenarios, as shown in Fig. 10. This analysis provides useful information regarding the power handling capacity improvement in the DSC solution. For example, with 10 000-W/m^{2}K convection and a maximum junction temperature of 154 °C, the maximum power loss per die that can be supported by the designed module is 127 W when cooled from single side. On the other hand, the power handling capacity can be raised to 200 W if cooled from double side. This indicates a significant 57.5% increase of power handling capacity per dies.

B. Stress Simulation

The temperature changes that power modules experience during their operation (power cycling) result in stresses due to the difference in CTEs between materials. The information obtained from the steady-state thermal simulation for this DSC module was applied as thermal load in a static structural simulation to identify areas where this effect causes an increased likelihood of failure. The properties of different materials and fuzz buttons [51], [52], [53], [57] are extracted from their datasheet.

To predict the reliability of the power module, von Mises stresses in different points, specifically at the venerable joint locations, are widely used. It is reported that the number of cycles to failure is inversely proportional to the maximum von Mises stress [17]. To evaluate the performance of fuzz button, stress at the top side of the dies is plotted for two conditions in our designed DSC module. The first condition is when the extrusions of copper pillar are directly attached to the top side of the dies, while the second condition is when the connection to the top side of the die is established by pressure contact using fuzz buttons + copper pillars. The first condition outputs a maximum stress of 126.5 MPa at the interposer top side of die interface. The fuzz button shows a significant 45% reduction, resulting in 70.01 MPa at the same interface. The comparison is shown in Fig. 11.

The maximum stress was identified to be accumulated at the top side of copper pillar to the top DBC interface in both SSC and DSC conditions, as shown in Fig. 12.

C. Material Used in the Module

SiC MOSFET chips rated at 1.2 kV, 20 mΩ manufactured by GeneSiC semiconductors and 1.2-kV, 50-A Schottky diodes from CREE are used inside the module. The drain pad of

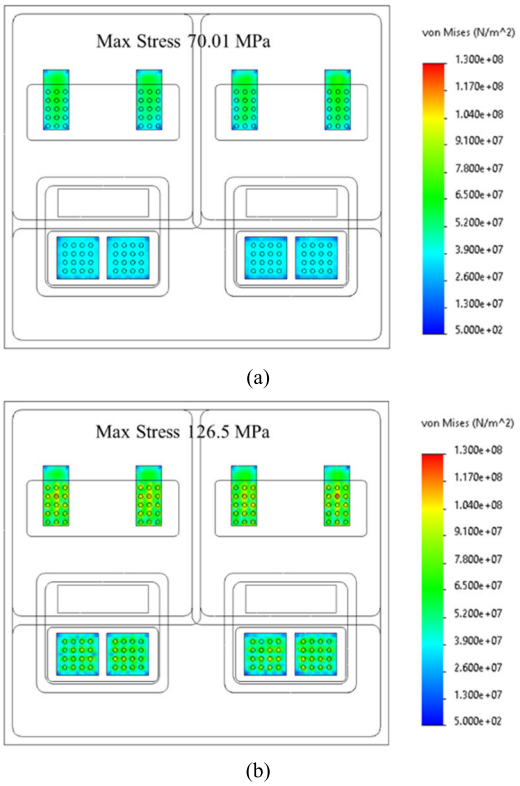

Fig. 11. Von Mises stress distribution at the interface between the topside of the die and interposer. Von Mises stress distribution at the top side of die for (a) fuzz button interconnect and (b) regular interconnect (only copper block).

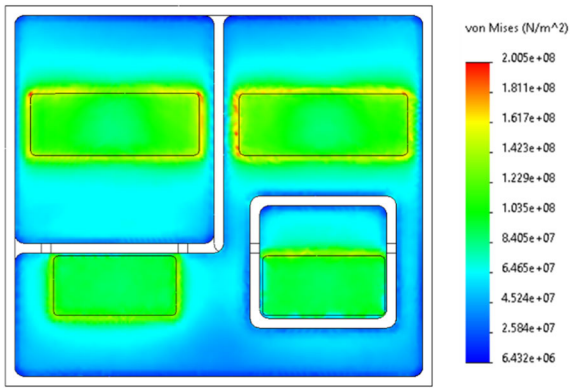

Fig. 12. Von Mises stress distribution at the interface between top DBC and copper pillars.

the device was metalized with a nickel–silver (Ni/Ag) surface finish, while the source and gate pads were aluminum (Al) metalized. The device is directly soldered from the drain terminal to the DBC substrate. The gate and Kevin-source pads were wire bonded using 5-mil-diameter Al wire. The DBC substrates are manufactured from AlN with electroless nickel immersion gold (ENIG) surface finish. Three distinct PCBs are used inside of the module. PCBs are used for retaining fuzz buttons and establishing input and output terminals. The first interposer PCB is 0.4 mm thick, while the second interposer PCB and ac PCB both come with 1 mm thickness. All the PCBs are made with FR4 material having a glass transition temperature of 175 °C. The copper pillars are manufactured using CNC machining. The fuzz button interposers each having 20 mil diameter and 40 mil length are purchased from custom interconnect. For attachment, SAC 305 and Pb37/Sn63 solder pastes are used. Table I shows a list of the materials used for making the proposed DSC module.

D. Assembly of Module

To fabricate the module, the designed DBCs, PCBs, and copper pillars are outsourced from suppliers. To assemble different parts together, SAC 305 and Pb37/Sn63 solder pastes are used. The fabrication process starts by applying SAC 305 solder paste on the bottom DBC with the help of stencil. Now, PCB-1 and the dies are mounted on the bottom DBC. Next, the assembly is heated up inside a reflow oven following the reflow temperature profile of SAC 305 solder paste. The gate and source Kelvin connection are established by 5-mil ultrasonic aluminum wire bonding from dies to PCB-1 after first reflow. Using the same SAC 305 solder paste, the top DBC is attached separately with ac PCB. Now, again using stencil, Pb37/Sn63 solder paste is applied on the dedicated solder pad of PCB-1 and PCB-2 (fuzz button retainer PCB) is placed on top of the previous assembly. Next, fuzz buttons are inserted on the designated holes (vias). These vias are placed exactly on top of the die locations. After inserting the fuzz buttons, CNC machined copper pillars are placed from top. These copper pillars have extrusion features from bottom sides. These extrusions are designed to go inside fuzz button holding vias and compress the fuzz buttons to establish a pressure contact. Silver epoxy (8330D) is used to attach the bottom sides of the copper pillars to PCB-2. The same Pb37/Sn63 solder paste is used on the top surfaces of the copper pillars and the combined top DBC and ac PCB is stacked on top of it. Finally, everything is held together using clamps and second reflow soldering is done. The casing for the module is made of acrylonitrile butadiene styrene (ABS) plastic and attached from the sides using RTV167 adhesive from Momentive. The ABS material used for the housing sidewalls has enough heat deflection temperature and glass transition temperature to sustain the adhesive curing and the subsequent encapsulant curing. Finally, silicone epoxy is filled inside the module and cured in place. The encapsulation material keeps oxygen and moisture away from the solder joints and interposers. Moreover, it strengthens the insulation and reduces the risk of partial discharge. A degassing of the encapsulant to remove bubbles before curing is a must. The gel curing takes place in a vacuum at 100 °C for 30 min. Fig. 13 summarizes the entire assembly process.

IV. Electrical Characterization of the Fabricated Module

The functionality and switching performance of the fabricated module are thoroughly evaluated after its successful fabrication. Switching loss is a function of switching speed and it is often dictated by the device characteristics, layout parasitics, and gate driver configuration [60]. To assess these aspects, a standard double pulse test (DPT) is conducted using the test setup shown in Fig. 14. In this setup, an air core inductor with a value of 53 μH serves as the load, which is

TABLE I
LIST OF MATERIALS USED INSIDE THE MODULE

Part	Material	Description
SiC MOSFETs	G3R20MT12 from GeneSiC	1.2 kV, 20 mΩ
Schottky Diodes	CPW5-1200-Z050B	1.2 kV, 50 A
DBC substrate	AlN-DBC with ENIG surface finish	Cu/AlN/Cu thickness: 0.3mm/0.63 mm/0.3 mm
PCB-1	FR4 PCB with copper layers	0.4 mm thick 2-layer PCB
PCB-2	FR4 PCB with copper layers	1 mm thick 4-layer PCB
AC PCB	FR4 PCB with copper layers	1 mm thick 4-layer PCB
Fuzz Button	BeCu with Au surface finish	20 mil diameter and 40 mil length
Copper Pillar	CNC machined copper pillar	Machined copper block of 2 mm and 1mm height
Attachment	SAC 305 Solder paste (96.5% tin, 3% silver, and 0.5% copper) for chip attach (1st reflow)	Melting temperature 220° C
Attachment	Pb37/Sn63 Solder paste (eutectic alloy of 37% Pb and 63% tin) for 2nd reflow	Melting temperature 183° C
Attachment	Silver Epoxy 8330D from MG Chemicals	Cure time 5 minute at 80° C
Casing	ABS plastic	Melting temperature: 200° C
Encapsulant	Silicone Gel (Semicosil 915 HT + Elastosil PT)	Two-part silicone gel

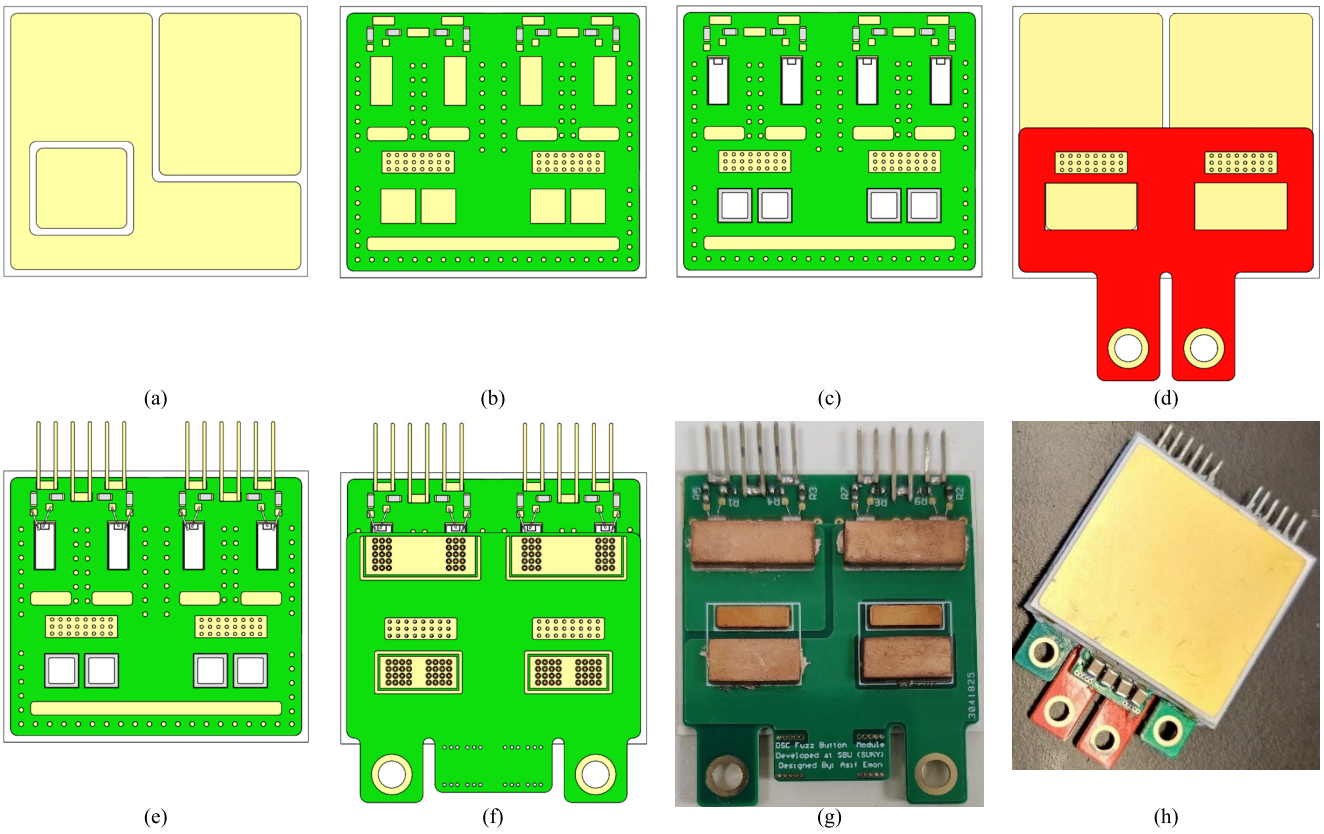

Fig. 13. Fabrication steps of DSC module using fuzz button. (a) DBC (both top and bottom DBC shares the same design). (b) DBC and interposer PCB-1 aligned for reflow. (c) Bottom DBC, PCB-1, and dies attached after the first reflow. (d) Top DBC and ac PCB attached during the first reflow. (e) Wire bonding to establish gate connection. (f) PCB-2 is placed, and fuzz button is inserted. (g) Copper pillars are placed on top of fuzz button. (h) Top DBC and ac PCB are placed on copper pillars and second reflow is done.

connected across the diode of the p-cell, while the MOSFET is being switched. For gate voltage provision, a custom gate driver is employed, which can provide +15/−5 V at the gate terminal referenced to the source. The logic signal at the input of the gate driver is provided using a DSP card from Texas Instruments. The test is carried out with an 800-V dc bus voltage and a load current of 150 A. To capture the high-speed transient events during the switching action, measurement devices are required to have enough frequency bandwidth. This is accomplished using a 1.5-kV differential probe (THDP0200) in conjunction with a six-channel oscilloscope (MSO56) from Tektronix. The oscilloscope has a bandwidth of 1 GHz, while the employed probe has a bandwidth of 200 MHz. The combined bandwidth of the probe and oscilloscope enables the

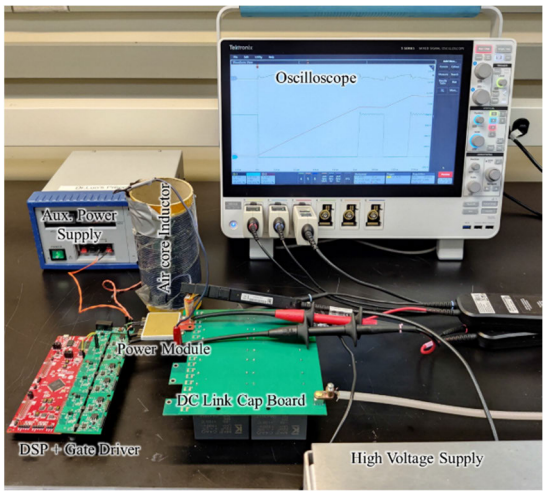

Fig. 14. Test setup for DPT test of designed module.

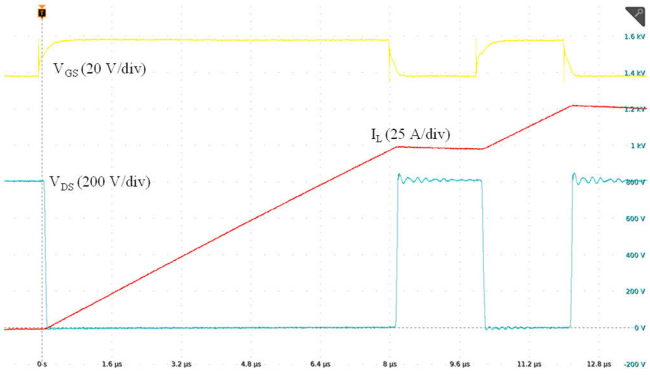

Fig. 15. Switching waveform obtained from the DPT test.

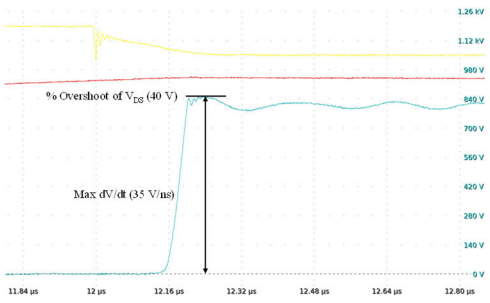

Fig. 16. Switching waveform during the turn-off event.

capture of switching speed and high-frequency oscillations that occur during switching events, ensuring accurate waveform analysis (see Figs. 15 and 16). The employed gate resistance at turn-on and turn-off path was 5 and 2 Ω, respectively. The maximum voltage slew rate (dV/dt) during the turn-off event was recorded around 35 V/ns, as shown in Fig. 16. During the test, no spurious mistriggering and insulation failure was observed.

The recorded overshoot on switching voltage (V_{DS}) during turn off was 40 V, which is 5% of the applied dc link voltage. The magnitude of this voltage overshoot is the product of di/dt and power loop inductance. The loop inductance can be verified by observing the ringing frequency in the switching waveform during device turn off [55]. According to the experimental waveform shown in Fig. 16, the equivalent L_{stray} is around 2.1 nH. The deviation is related to the effect of parasitic inductance from the decoupling capacitors and additional parasitic capacitance contributed from the module (mostly from the stacked PCB boards) that is coming parallel to C_{oss} of the dies. The captured switching waveforms indicate that the module is functional and shows coherence to the design analysis done by simulation studies in Section II.

V. Conclusion

This work provides the detailed design, analysis, and characterization of DSC split-phase module with fuzz button as interconnect. According to our analysis, the fuzz button shows a significant 45% reduction in thermomechanical stress in critical interface over solid copper interposer. The double-sided cooling feature shows around a 57.5% increase in power handling capacity per die compared to single-sided cooling for a fixed convection coefficient of 10 000 W/m^{2}K. The fabrication processes are described in detail and the assembled module is switched at the rated voltage and current. The module shows good switching performance with an overshoot of less than 5% of the dc link voltage.

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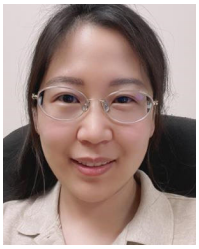

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