Converter-Level Packaging and Optimization for a SiC-Based Grid-Interface Converter Using Discrete Devices

Abdul Basit Mirza, *Graduate Student Member, IEEE*, Kushan Choksi, *Graduate Student Member, IEEE*, Austin Zhou, *Graduate Student Member, IEEE*, Sama Salehi Vala, *Graduate Student Member, IEEE*, and Fang Luo, *Senior Member, IEEE*

***Abstract*— Grid integration of renewables through power electronic grid-interface converters (GICs) is essential for achieving a sustainable grid. This mission involves developing compact, efficient converters with standardized interfaces to minimize redundancy. In line with this objective, this article presents an electromechanical–thermal design and packaging of two-stage silicon carbide (SiC)-based 75-kVA GIC using TO-247 discrete devices with two times lower cost-to-power ratio than power modules. The power stage is 3-D packaged on a cylindrical-hole-based three-face utilized heat sink to achieve 5.5-kW/L power density, including passive components. For the dc–ac stage, two-level split-phase (2L-SP) topology is employed, owing to its lower switching loss and output dv/dt and increased crosstalk immunity compared with simple two-level (2L) topology. An equivalent switching transition circuit is derived for optimal sizing of split inductors in 2L-SP. Furthermore, for device interconnection, an optimized printed circuit board (PCB) layout with flux cancellation and minimum board parasitic capacitance is developed for optimal device switching with minimum voltage overshoot. Moreover, for magnetics, the split-direct winding technique is employed to achieve minimum winding capacitance. Finally, the developed GIC is systematically tested at rated system voltage with an RL load at 10 kVA.**

***Index Terms*— 3-D converter-level packaging, grid-interface converter (GIC), printed circuit board (PCB) parasitic capacitance, silicon carbide (SiC), split-direct winding, split-phase topology (2L-SP), three-face utilized heat sink, TO-247 package, vector fitting (VF).**

I. Introduction

IN RECENT years, grid integration of renewables, energy storage, and electric vehicle (EV) charging systems has resulted in a significant surge in the utilization of bidirectional grid-interface converters (GICs). Typically, these converters consist of a two-stage configuration, consisting of a grid-interfaced dc–ac converter coupled with a dc–dc stage converter. Nevertheless, the emerging trend of employing GICs within future smart grids brings challenges from both performance and design perspectives. Addressing these challenges becomes paramount to ensure efficient and reliable operation within evolving grid infrastructures [1], [2].

To begin with, the dc side voltage varies depending on the application. For instance, renewable energy sources such as photovoltaic are intermittent and the output voltage varies depending on sunlight intensity [3]. Similarly, in a battery energy storage system, the voltage needs to be regulated to ensure efficient charging or discharging. This variability in voltage poses a constraint on the dc–dc stage, requiring it to have a wide input range. Furthermore, GICs must be fault-tolerant and reliable. The dc–ac converter stage is susceptible to various grid faults. In such scenarios, converter typologies that are fault tolerant are preferable as they can help in mitigating the rapid rise of fault current and keeping it within the device's current limit [4], [5].

Moreover, wide bandgap (WBG) devices, such as silicon carbide (SiC), have led a paradigm shift to make GICs compact and modular to lower manufacturing costs and increase interoperability among GICs. The rationale behind the trend is the fast switching capability of SiC devices, which allow high-frequency operation, leading to shrinkage of size passive components. However, from the device packaging perspective, the fast switching behavior of SiC devices also dictates a tight approach for interconnection between devices to limit voltage overshoot during switching transition due to the device's package parasitic inductance and capacitance. Furthermore, a design with high parasitics also increases conducted and radiated electromagnetic emissions [electromagnetic interference (EMI)] [6], [7]. Achieving low parasitics requires devices to be placed in proximity. However, this requirement brings the concern of positive thermal coupling between devices [8], [9]. Hence, power device layout is a multiobjective problem and requires electromechanical–thermal codesign.

Power modules offer smaller footprints with optimized loop inductance and thermal performance than discrete devices and are preferred for high-power applications [7], [10]. A power module packages semiconductor dies in a compact structure

Manuscript received 23 February 2024; revised 14 March 2024; accepted 19 March 2024. Date of publication 5 April 2024; date of current version 3 January 2025. This work was supported in part by the Oak Ridge National Laboratory (ORNL), funded through the Department of Energy (DOE)—Office of Electricity's (OE) Transformer Resilience and Advanced Components (TRAC) program, led by the program manager Andre Pereira; and in part by the National Science Foundation (NSF) under Award 1846917. Recommended for publication by Associate Editor S. Narumanchi upon evaluation of reviewers' comments. *(Corresponding author: Abdul Basit Mirza.)*

The authors are with the Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY 11790 USA (e-mail: abdulbasit.mirza@stonybrook.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCPMT.2024.3385398.

Digital Object Identifier 10.1109/TCPMT.2024.3385398

with an optimized layout, which is interconnected into various circuit configurations [11], [12], [13], [14], [15]. The most prevalent configurations include half-bridge, full-bridge, and three-phase, while less frequent configurations include three-level T-type neutral point clamped (3L-TNPC), three-level active neutral point clamped (3L-ANPC), buck, and boost with limited current and voltage ratings [16]. For power modules, the designer is only required to design the bus bar, controller, cooling, and gate driver. Nevertheless, power modules lack standardization as manufacturers have proprietary module designs, which drives up the system cost [17], [18].

In contrast, SiC devices in discrete packages are cheaper and offer a low cost-to-power ratio due to their well-established and standardized fabrication processes [19]. Besides this, they also offer greater flexibility for converter-level packaging than power modules, as they can be paralleled with flexibility in spaced-constrained applications [20], [21], [22]. For GIC applications, which typically have a dc link voltage of 800 V, 1200-V-rated SiC devices are predominantly used. Among the standard discrete device packages for 1200-V SiC devices, the TO-247 package is matured owing to its lower thermal resistance with current ratings exceeding 100 A [23], [24].

Numerous works related to GIC development using SiC devices in the TO-247 package have been reported in the literature to achieve a low cost-to-power ratio, high efficiency, and high density [17], [19], [25], [26], [27]. In [17] and [19], a power module based on the repackaging of TO-247 discrete SiC devices is proposed. To minimize the loop inductance, a decoupling capacitor board based on a vertical loop layout is embedded inside the package. Although the vertical loop layout minimizes the loop inductance due to flux cancellation [28], it increases the underlying parasitic capacitance of the board, which slows down the device and increases switching loss [29]. This is a challenge for the interconnection of discrete devices using printed circuit board (PCB) and has not been addressed in [17] and [19]. Besides this, the design claims to achieve 11-kW/L power density for 75 kVA, but the value is computed excluding magnetics.

Similarly, in [25] and [26], a design of 30-kW GIC using six-paralleled 80-mΩ SiC devices per position is presented with a comparatively lower power density of 2 kW/L, excluding passive components. The dc–ac stage is shown to achieve 99.07% efficiency at rated load, but no value is provided for the two-stage efficiency. Furthermore, no insight into PCB and passive component layout optimization, switching, and thermal performance is presented. Mookken et al. [27] present a design of a 50-kW two-stage GIC using second-generation SiC discrete devices from Wolfspeed. The dc–dc stage comprises a four-phase interleaved boost converter (IBC), and the dc–ac stage is based on a three-level T-type inverter. The dc–dc stage is shown to achieve a peak of 99.4% efficiency. However, no value is provided for the two-stage efficiency and power density. Besides this, no details on the power loop layout optimization, thermal management, and magnetics design are provided.

Furthermore, from the cooling perspective, the GICs in [17], [19], [25], [26], and [27] are arranged laterally and use a single-faced utilized heat sink, where the TO-247 devices are placed on one side (top) of the heat sink (3-D layout). This trend is also prevalent in SiC-based converters intended for transportation applications [30]. However, the single-faced utilized heat sink approach, albeit simpler, increases the overall volume and footprint of the converter as a larger surface area is required to arrange devices on one side of the heat sink. Furthermore, a large base plate area is usually left for heat spreading and the power devices cover a minor area of the heat sink base plate [31]. As a result, the benefit of SiC devices in increasing power density by shrinking the size of passive components is overshadowed by the significant volume of the heat sink. This limitation can be overcome through a multiface utilized heat sink geometry and converter-level packaging to achieve high power density while ensuring maximum thermal performance.

Besides this, from the passive component performance perspective, the fast switching capability of SiC devices mandates the design and packaging of passive components with minimum parasitics [32]. For instance, the distributed intrawinding and interlayer winding capacitances of an inductor interact with the distributed inductance, leading to multiple series and parallel resonances in the impedance at high frequencies [33], [34]. These resonances are more prone to be excited with WBG devices than silicon (Si) due to the relatively high amplitude of high-frequency harmonics due to fast switching (high dv/dt and dv/dt), leading to pronounced current or voltage ringing during switching. In other words, the inductor acts as a transmission line at high frequency, leading to voltage or current ringing depending upon the impedance mismatch [35], [36]. The voltage and current ringing increase switching loss and introduce unwanted near-field EMI [37].

This article presents 3-D converter-level packaging and passive component layout optimization of 75-kVA SiC-based GIC to achieve high power density and heat sink utilization. The GIC is electromechanically thermally designed and 3-D packaged on a cylindrical hole-based heat sink, where three faces (top and two sides) are utilized for cooling. The power stage is built using discrete SiC devices in a TO-247 package, offering a cost-to-power ratio two times lower than the power modules with equivalent ratings. For device interconnection, as opposed to [17] and [19], a comprehensive study is performed to design a noninterleaved vertical layout for the TO-247 device package with minimum parasitic capacitance to achieve fast switching.

Furthermore, from a performance perspective, 2L-SP topology is employed for the dc–ac stage, leveraging its inherent fault-tolerant capability and crosstalk immunity [38], over the standard 2L topology, predominantly employed in GICs [19], [39]. A detailed design procedure for sizing split inductors in 2L-SP, based on spike current minimization, is proposed and utilized. Moreover, for winding layout optimization for magnetics, the split-direct winding technique is employed to improve the high-frequency impedance response, resulting in a four times reduction in parasitic capacitance and 0.4% current overshoot during the switching transition. Finally, the GIC components are assembled together and tested at a rated voltage of 10 kVA.

This article is organized as follows. Section II presents the system architecture and discusses the topology and power device selection of the proposed GIC. A brief discussion and

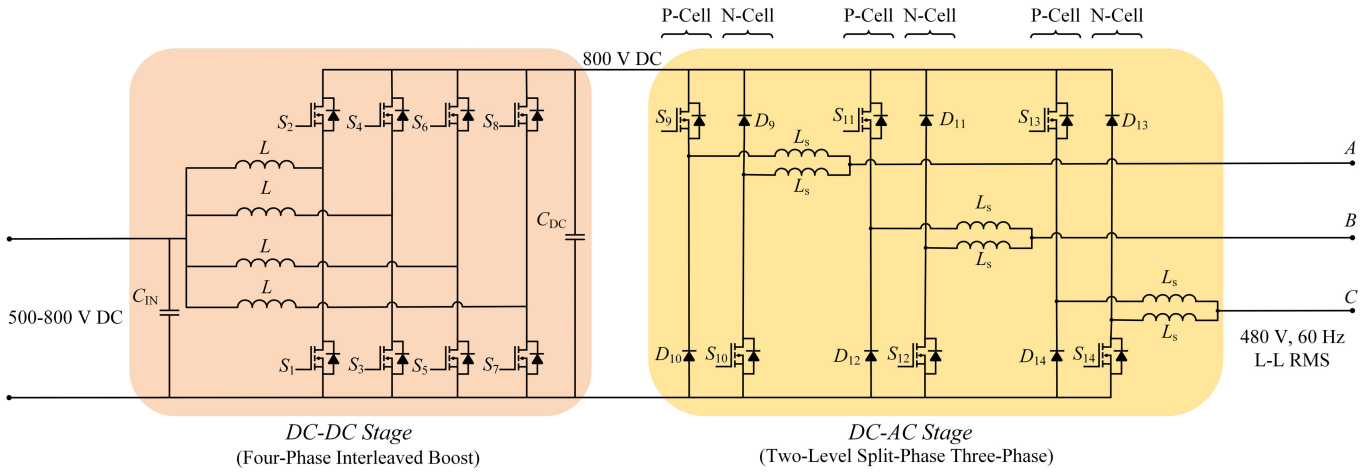


Fig. 1. Proposed GIC schematic.

TABLE I
GIC SPECIFICATIONS

Stage	DC-DC	DC-AC
Peak Power (kVA)	75	
DC Side Voltage (V)	500–800	-
AC Side Voltage (V)	-	480 L-L RMS
DC Link (V)	800	
Switching/Carrier Frequency (kHz)	70	30
Peak Device Current (A)	60	140

comparison of 2-D and 3-D converter packaging layouts in Section III follow this. Section IV–VI highlight the hardware development of major components of the GIC, which involves designing and optimizing the three-face utilized heat sink, power PCB, and magnetics winding layout. Section VII focuses on developed GIC hardware testing, where test results for standalone and two-stage testing are presented. Finally, Section VIII concludes this article.

II. GIC Structure and Power Device Selection

Fig. 1 shows the structure of the proposed GIC, comprising dc–dc and dc–ac converter stages. The corresponding specifications of the dc–dc and dc–ac converter stages are tabulated in Table I. The peak power handling capacity is 75 kVA. The dc side has a variable voltage range of 500–800 V, while the ac side is standard three-phase 480 L-L rms. The dc–dc and dc–ac stages are interfaced at an 800-V common dc link.

Sections II-A and II-B discuss topology and power device selection.

A. Topology Selection

1) DC–DC Stage: The GIC is intended to be interfaced with the grid through a line-frequency transformer, providing isolation between the grid and the dc side. In such configuration, the dc–dc stage can be nonisolated [40], [41]. Hence, popular isolated bidirectional topologies such as an LLC resonant converter [42] and dual active bridge (DAB) [43], are not considered.

The dc–dc stage needs to boost the voltage to the nominal dc link value when the dc side voltage is less than 800 V and power flow is from the dc side to the ac side. Conversely, when the power flow is opposite, the voltage needs to be lowered. For this purpose, among the traditional bidirectional nonisolated topologies, the synchronous IBC topology provides benefits such as simple design and control, smaller input current ripple Δi_{in} and inductor size, smaller output voltage ripple Δv_{out} and capacitor size, modularity, wide-range boost operation, and better thermal management [44]. Also, interleaving equally divides the current between phases and lowers the current ratings of the passive components and semiconductors [45]. Hence, the synchronous IBC topology is selected for the dc–dc stage.

For an IBC, the number of phases interleaved n directly impacts the phase current dc component I_{dc} and ripple quantities Δi_{in} and Δv_{out}. Therefore, it is imperative to select the optimum phases to achieve tradeoff between these performance metrics, component count, and cost. Fig. 2 plots the variation with n for I_{dc} and normalized Δi_{in} and Δv_{out}, with respect to single phase, for the maximum boosting scenario (500 V on the dc side). The expressions for normalized Δi_{in} and Δv_{out} are obtained from the analysis, as presented in [46]. The variation of Δi_{in} and Δv_{out} with n is identical, and all three metrics follow an inverse relation with n. For $n < 4$, the drop in all three quantities is significant, whereas, for $n > 4$, it is moderate. Therefore, for the given GIC parameters, $n = 4$ is deemed optimal and is finalized.

2) DC–AC Stage: In contrast to the standard two-level (2L) topology employed predominantly in GIC, such as in [17], 2L split-phase (2L-SP) topology with sinusoidal pulsewidth modulation (SPWM) is chosen for the dc–ac stage. 2L-SP topology comprises P- and N-cells, with split inductors L_s connected between the midpoint of these cells (see Fig. 1). The topology working principle is discussed in detail in [47].

Compared with the traditional 2L inverter, 2L-SP offers lower switching loss and mitigates risks of mistriggering under high dv/dt conditions [38], [47], [48], [49]. A comprehensive device loss analysis is conducted for a 2L-SP three-phase inverter with SPWM in [38]. The analysis covers device loss

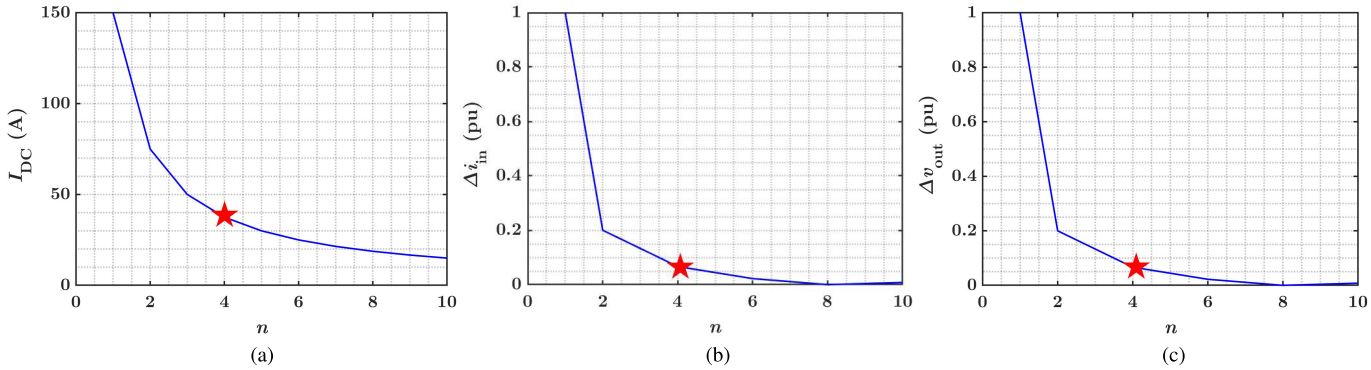


Fig. 2. Variation of IBC phase current and ripple quantities. (a) I_{dc}. (b) Δi_{in}. (c) Δv_{out}.

variation with key performance metrics, including SPWM modulation index (m), switching frequency (f), power factor angle (ϕ), and conduction current amplitude (I_{cm}). According to the results, the device loss variation with performance metrics (m, f, ϕ, and I_{cm}) for 2L-SP is always upper bounded by that of the 2L inverter. Furthermore, the experimental efficiency comparison plot for the 2L and 2L-SP prototypes shows that the efficiency of 2L-SP is higher than for 2L and the increase in efficiency increases with an increase in frequency. This trend makes 2L-SP more favorable for SiC devices.

Moreover, due to split inductors, dv/dt at midpoint/ac output of the phase leg is reduced [50]. From the EMI/electromagnetic compatibility (EMC) perspective, the lower dv/dt provides a potential benefit of lowering common-mode (CM) emissions. The CM EMI benefit has been investigated using the developed GIC hardware in [51], where a maximum of 17.85-dB reduction in the 10–30-MHz frequency range is achieved. Moreover, the slower voltage rise is beneficial for mitigating reflective wave phenomenon [51], [52]. Finally, the presence of split inductors also contributes to a lower rate of rise of current during switch short circuits or grid faults [5], [53].

B. Power Device Selection

For high-power applications, such as the proposed GIC, power device selection is critical as it directly impacts both the electrical and thermal performance of the system and the underlying EMI emissions. Power modules are preferred for high-power applications owing to their optimized layout and tight integration, resulting in minimum parasitics. However, compared with discrete devices, the cost-to-power ratio for power modules is higher. Moreover, at present, there are no commercially available power modules combining P- and N-cells in a single package for the 2L-SP topology for the dc–ac stage. Therefore, for building 2L-SP with power modules, separate power modules intended for the buck (P-cell) and boost (N-cell) applications are needed, which, compared with the standard half-bridge configuration, have limited options and commercial availability.

Another approach to address the commercial unavailability of power modules that combine P- and N-cells for 2L-SP is to replace these cells with half-bridge and employ synchronous rectification style modulation. This configuration offers abundant options with power modules as it can be built using six half-bridge or three full-bridge SiC power modules, which are widely available due to their extensive usage across various applications. However, the demerit of this configuration is that it requires six extra gate drivers and embedded system peripherals for the gate drive control, making it impractical and economically infeasible.

Table II compares key performance metrics between discrete TO-247 package and power module-based SiC device options screened for the proposed GIC. Commercial availability with lower lead time is the primary factor influencing the selection of power modules. For the dc–dc stage, ample options for the half-bridge configuration of each IBC phase are available, and CAB016M12FM3 from Wolfspeed is finalized owing to its smaller footprint and lower C_{OSS}. However, for the dc–ac stage, only one feasible buck (P-cell) and boost (N-cell) power module pair with an adequate current rating capacity from ROHM is identified [54], [55].

For the discrete version, several devices from different manufacturers are evaluated using an in-house developed model-based optimization (MBO) algorithm [56], [57], [58]. The algorithm takes the static and dynamic characteristics of the devices and the rated operating conditions of the converter as input to generate efficiency versus frequency and efficiency versus load plots for all the devices. Based on the results, the C3M0016120D SiC MOSFET from CREE and the FFSH50120A Schottky Diode from Onsemi are selected due to their performance and availability in stock.

The discrete option for the dc–ac stage has two times lower cost-to-power ratio and a smaller footprint per phase leg compared to the power module option. The cost-to-power ratio is based on the price during the device selection phase. Furthermore, the footprint per phase leg for the dc–ac stage with power modules is 470% higher than the discrete solution since two separate power modules in P- and N-cell configurations are required. Consequently, the footprint and heat sink size of the converter-level package using power modules are larger than with discrete devices, lowering power density with increased device cost. Besides this, from the electrical performance perspective, the power module version has a higher C_{OSS} per position than the discrete version, implying high switching loss and lower switching speed. Therefore, based on the metrics comparison, the discrete version is deemed viable and selected for the development of both the dc–dc and dc–ac converter stages.

TABLE II
SiC Discrete and Power Module Device Solutions for the Proposed GIC

Parameter	Discrete (TO-247) Solution		Power Module Solution	
	DC-DC	DC-AC	DC-DC	DC-AC
Manufacturer	CREE	CREE (MOSFET) Onsemi (Diode)	CREE	ROHM
Part	C3M0016120D (MOSFET)	C3M0016120D (MOSFET) FFSH50120A (Diode)	CAB016M12FM3	BSM300C12P3E301 (P-cell) BSM300C12P3E201 (N-cell)
Device Per Position/ Module Per Phase-leg	1	2	1	1
R_{ON} Per Position at T_J = 25 °C (mΩ)	16	8	16	7
Current Rating at T_J = 25 °C (A)	115	230	95	300
C_{OSS} at 800 V (pF)	230	460	300	660
Phase-leg Footprint (mm^2)	664	2656	1423	15128
Cost-to-power Ratio ($/kVA)	28		60	

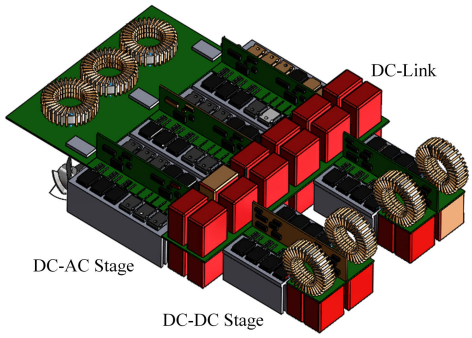


Fig. 3. 2-D converter-level packaging conceptual layout.

Sections III–VI discuss the design of major converter-level packaging-related components of the GIC.

III. Converter-Level Packaging

With discrete devices, one of the prime objectives is to increase the power density while ensuring optimum thermal performance, which relies on the heat sink. The heat sink design depends on the converter-level packaging, which is, in this case, determined by the packaging and assembly of dc–dc and dc–ac stages and the overall footprint of the GIC.

Fig. 3 shows a 2-D concept layout where the converter assembly is arranged laterally. For cooling, separate heat sinks are utilized for the dc–dc and dc–ac stages due to dc link capacitors in between. The 2-D design is more straightforward and allows easy access to components. However, this is achieved at the expense of low power density and a larger footprint, as only the top side of the heat sink is utilized for heat dissipation. Moreover, dc link capacitors between the dc–dc and dc–ac stages' heat sinks also impede the airflow, requiring a custom-designed airflow duct.

Recently, 3-D packaging for power converters has gained momentum. A half-bridge, three-sided cooled power module is proposed in [59], where the power devices are placed on top and side faces of the heat sink. Following this approach, a 3-D stacked concept layout is proposed where three faces (two sides and the top) of the heat sink are utilized for cooling, as shown in Fig. 4. The dc–dc stage is split into two boards, each comprising two phases, placed on the side faces of the heat sink. The dc–ac stage is arranged on the top side of the heat sink, with the dc link capacitor PCB sitting on top of it. The P- and N-cell midpoint terminals are taken out on dc–ac stage PCBs separately. This layout allows for the dc–ac stage to be configured as simple 2L or 2L-SP. The dc link board is interfaced with dc–dc and dc–ac PCBs using copper bus bars and tabs. Finally, on top of the dc link capacitor board, an interface board containing dc–dc stage inductors and capacitors is stacked.

From a power density perspective, the 3-D packaging concept, with identical PCB board dimensions and including passive components, provides an overall power density of 5.5 kW/L and a 35% reduction in heat sink volume compared with the 2-D concept layout. Hence, the 3-D layout in Fig. 4 is chosen for the converter-level packaging.

IV. Three-Face Utilized Heat Sink Design

Compared with the traditional fin-based heat sink design, the three-face utilized heat sink in the proposed 3-D packaged layout in Fig. 3(a) needs to dissipate heat from all three sides. Furthermore, it needs to provide mechanical support for PCB boards and passive components such as dc link capacitors. These heat sink performances depend on the fin design/geometry and device loss distribution for both converter stages.

The loss per device for the GIC is estimated using the MBO approach [56] for the maximum power output of 75 kVA. For MOSFETs (S_1–S_{14}), the ON and OFF gate resistances R_{Gon} and R_{Goff} are considered to be 5 and 2.4 Ω, respectively. The loss per device (S_1–S_8) for the dc–dc stage estimated is 68.75 W. Furthermore, the loss per device per position for the dc–ac stage with 10-μH split inductance is estimated to be 40.83 W for S_9–S_{14} and 17.5 W for D_9–D_{14}, respectively. The loss values constitute the two-stage power semiconductor efficiency value of 98.4%. In addition, for comparing 2L-SP

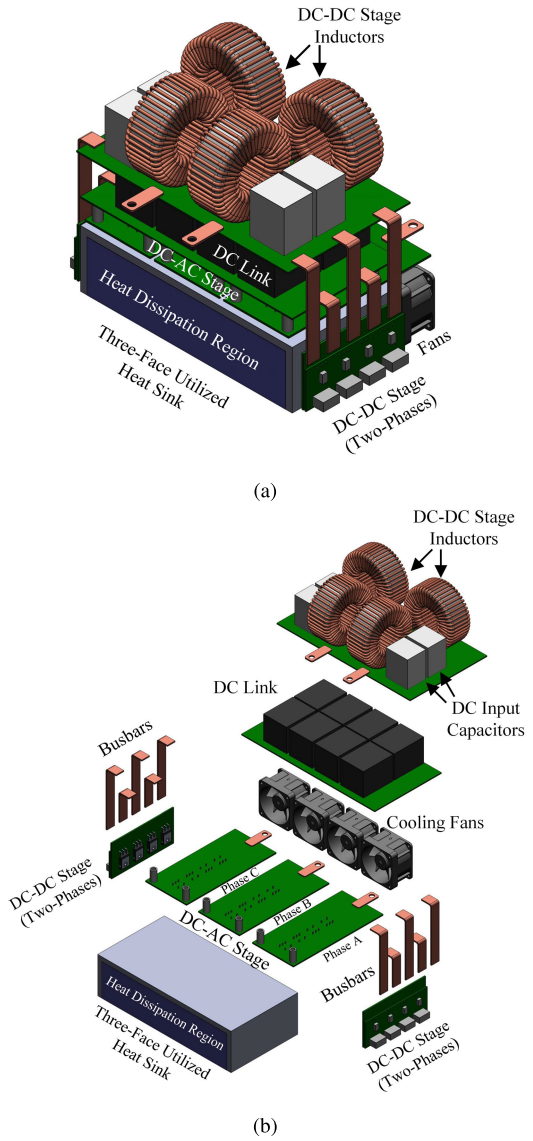


Fig. 4. 3-D converter-level packaging conceptual layout. (a) Trimetric view. (b) Exploded view.

with 2L, a loss calculation is also performed for traditional 2L topology for the dc–ac stage. The calculated loss for S_9–S_{14} and D_9–D_{14} is 65.5 and 4 W, respectively, resulting in a two-stage efficiency of 98.15%, which is 0.35% lower than with 2L-SP.

A. Heat Sink Geometries

Fig. 5 shows heat sink geometries, initially considered for the heat sink design [60]. The heat sink base thickness is kept at 8 mm on all sides to ensure optimum heat spreading and sufficient space for screws holding the power devices.

The vertical fin design has the drawback of only dissipating heat from the top side. According to the loss analysis, the dc–dc stage devices placed on the side faces have the highest power dissipation. Since there are no fins channeling heat from the sides, the vertical fin design brings concerns about overheating of dc–dc stage switches. The concern is overcome by the hybrid fin design in Fig. 5(b), with a lattice structure

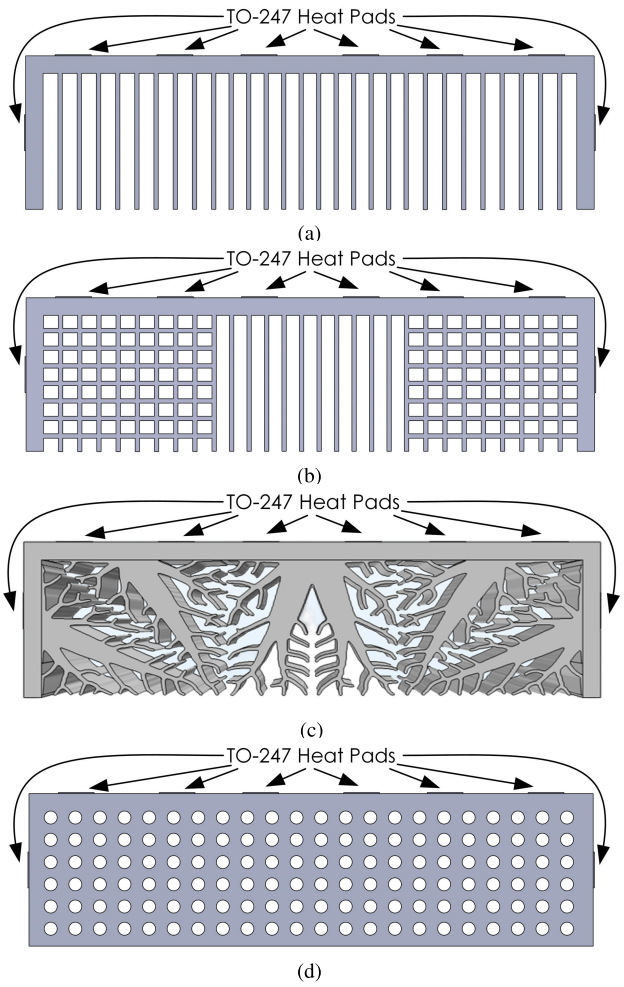


Fig. 5. Heat sink geometries. (a) Vertical fin. (b) Hybrid fin. (c) Tree structure. (d) Circular hole.

(combination of vertical and horizontal fins) for the side faces for channeling the heat toward the interior of the heat sink. However, the hybrid fin design suffers from high manufacturing costs due to cut extrusion for the lattice part. Furthermore, the room for optimization of fin spacing is limited due to the proximity of fins.

Fig. 5(c) presents a classic tree-like structure generated through topology optimization [61]. Topology optimization is devoted to finding the optimal material distribution for a desired performance. In this case, the objective of the topology optimization is to maximize the thermal compliance of the heat sink in consideration of heat conduction and convection effects. However, the fabrication of a tree-like structure is intricate with the conventional CNC process. Also, similar to the vertical fin design, the tensile strength of this structure is lower, especially in the middle of the heat sink.

The cylindrical hole-based design in Fig. 5 is cost-effective and provides optimal thermal performance. For instance, in [59], the approach is shown to keep the maximum temperature of the device to 94.4 °C. Besides this, the design provides better mechanical stability as the heat sink serves as the chassis for PCB boards and passive components. Deep threaded holes can be used to tight threaded rids to support

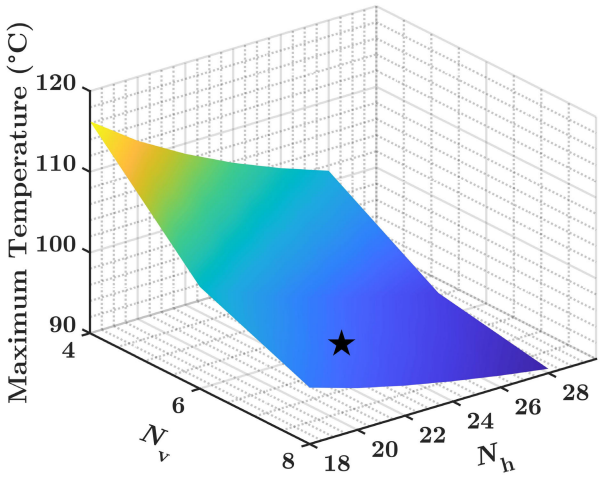


Fig. 6. Maximum junction temperature variation with N_h and N_v.

fans and passive components. Finally, the heat sink bottom base is solid, providing an additional provision for chassis mounting of the GIC to the NEMA box enclosure. Owing to these benefits, the cylindrical hole-based design is chosen for the proposed 3-D packaging.

B. Parametric Study for Optimal Design

The design of a cylindrical hole-based heat sink involves finding the optimal number of holes in the horizontal N_h and vertical N_v direction. For this purpose, a parametric thermal study (18 cases) is performed in SOLIDWORKS with N_h and N_v swept from 18 to 28 and 4 to 8, respectively.

The heat source for each device is simulated using a copper pad with dimensions equal to that of the TO-247 package. The heat sources are set to their respective power dissipation values estimated using MBO. Furthermore, a thermal interface is also inserted between the copper pad and heat sink with a thermal resistance of 0.3 °C/W. The thermal interface represents the aluminum oxide (Al_2O_3) heat pads, selected for the GIC for providing electrical insulation between the device and the heat sink. Finally, aluminum 6061 (T6) is chosen as the heat sink material for the study.

The heat sink design is based on forced air cooling, for which the heat convection coefficient is a crucial parameter, impacting the thermal performance. According to [62], the natural air convection coefficient ranges from 5- to 25-W/m^{2}K range, whereas the convection coefficient for forced air cooling lies within 25–250-W/m^{2}K range. The given study's ambient temperature is set to 25 °C. A natural convection coefficient of 15 W/m^{2}K is applied to the face of the heat sink, and a forced air convection coefficient of 150 W/m^{2}K is applied to inner hole surfaces.

Fig. 6 summarizes the results for all 18 cases. The maximum heat pad temperature falls exponentially with N_v and N_h. The maximum temperature values are below the maximum allowable junction temperature T_J for SiC devices (175 °C). The minimum temperature is reached for $N_h = 28$ and $N_v = 8$ with a value of 93.76 °C whereas the maximum junction temperature occurs for $N_h = 18$ and $N_v = 4$ with a temperature value of 116.5 °C. Although increasing the number of holes

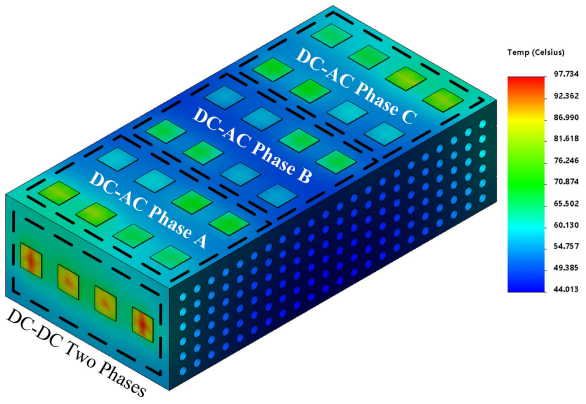


Fig. 7. Heat sink temperature heat map for $N_h = 22$ and $N_v = 6$.

effectively lowers the temperature (see Fig. 6), but the extent of reduction in temperature decreases as the number of holes is increased. Moreover, from a manufacturing perspective, drilling many closely spaced holes for a small gain in thermal performance is not viable. For instance, the horizontal and vertical hole edge spacing for $N_h = 28$ and $N_v = 8$ is 2.81 and 1.29 mm, respectively. With a heat sink depth of 130 mm, drilling holes with less spacing is costly and time-critical. The $N_h = 22$ and $N_v = 6$ configuration offers decent performance near to that of $N_h = 28$ and $N_v = 8$ with adequate 5.33- and 4.2-mm horizontal and vertical hole edge spacing. Owing to this, $N_h = 22$ and $N_v = 6$ layout is selected as the final design.

The thermal distribution for $N_h = 22$ and $N_v = 6$ configuration at 75-kVA power output is presented in Fig. 7. The average temperature levels at 57 °C and the maximum temperature (97.74 °C) are observed for the dc–dc stage devices, which is < 175 °C (maximum allowable T_J).

C. Experimental Validation

A thermal test bench is set up to validate the performance of the final heat sink design. The thermal camera is positioned to capture the trimetric thermal image at maximum power dissipation. Owing to the power supply limitation for testing the GIC at 75 kVA, the power devices are replaced with power resistors in the TO-247 package. The resistor values are chosen such that the power dissipation matches the estimated values from MBO at 75 kVA output. For electrical insulation, 3-mm Al_2O_3 ceramic-based thermal pads from Fischer Elektronik are placed between the device and the heat sink. The thermal pads provide excellent dielectric strength of 10 kV/mm with 0.3 °C/W thermal resistance. Furthermore, four fans from Sanyo Denki with 37.1 CFM airflow capacity are operated at full power for forced air cooling [63]. Fig. 8 shows the experimental setup and measured thermal image. The heat sink is painted with flat black spray paint to increase the emissivity. The average heat sink temperature levels at 65.5 °C, which is closer to the simulated value of 60 °C, justifying the efficacy of the proposed heat sink design.

V. Magnetics Design and Winding Layout Optimization

The boost and split-phase inductors are built using the high flux (HF) toroid as the core material from Magnetics, which

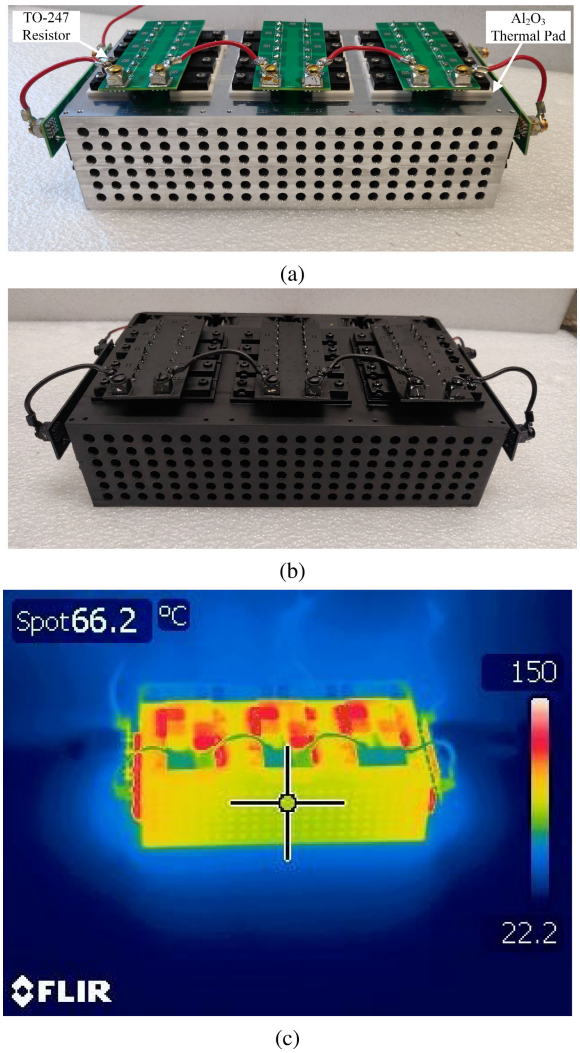


Fig. 8. Test results. (a) Developed heat sink with TO-247 power resistor boards. (b) Flat black painted heat sink (two coats). (c) Thermal distribution at 75 kVA (emulated).

provides an optimum balance between core loss and dc bias performance. The inductors are constructed using 18/18 Litz wire to alleviate the skin effect on ac resistance.

A. DC–DC Stage

For the four-phase IBC, the value of phase inductance L depends on the duty cycle D, input voltage V_g, switching frequency f_{SW}, and ripple Δi_L. Generally, Δi_L is chosen to 10% to 30% of the phase dc current I_{dc} component at maximum power P [64], [65], [66]. By expressing $\Delta i_L = \alpha I_{dc}$ where $I_{dc} = 0.25P/V_g$ for four-phase IBC, the following expression is obtained [64]:

$$L = \frac{2V_g^2 D}{f_{SW}\alpha P}. \tag{1}$$

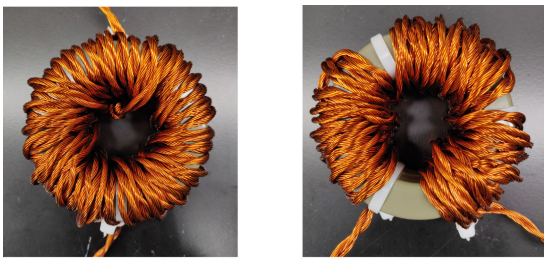
In (1), L varies inversely with α and the optimum value of L is the knee point of the L versus α curve. For the maximum boosting scenario for the proposed GIC (500 V on the dc side), the knee point using (1) is at $\alpha = 0.2$, with a corresponding L value of 180 μH. Therefore, this L value is finalized for the dc–dc stage. Furthermore, for the inductor core, two stacked 26-μ HF cores from Magnetics (0058908A2) are chosen to achieve 180 μH with 48 turns. The estimated maximum reduction in inductance due to dc bias at rated power is approximately 4%.

The performance of an inductor is contingent upon the winding layout, which determines the parasitic capacitance. The parasitic capacitance results from the turn-to-turn (intralayer and interlayer) and turn-to-core capacitances, which are distributed across the winding. The interlayer turn-to-turn capacitance exists in a multilayer winding, contributing significantly to the total capacitance due to nonadjacent turn-to-turn coupling [67]. However, for the chosen core, a minimum of two layers are required to wind 48 turns due to the limited inner circumference of the core. Hence, interlayer turn-to-turn is unavoidable, and the winding layout needs to be optimized to lower the parasitics.

Among various multilayer winding approaches, the direct winding technique has been proven effective in reducing parasitic capacitance due to its constant voltage gradient across turns and its simplicity of implementation [68]. Toroidal inductors inherently employ direct winding since each layer starts exactly above the previous one. However, even with direct winding, a significant amount of distributed parasitic capacitance remains, leading to multiple series and parallel resonance points in the impedance at lower frequencies (a few megahertz) [35]. To address this issue, a split-direct winding approach has been proposed in [35], which involves dividing the winding into multiple sections. This technique has shown to be promising in reducing the distributed capacitance of a medium-voltage (MV) transformer, shifting the series and parallel resonance points to higher frequencies [35].

Fig. 9 illustrates two inductor prototypes developed for the dc–dc stage using the direct and split-direct winding techniques in Fig. 9(a) and (b), respectively. The direct winding inductor consists of 48 turns across two layers, while the split-direct winding inductor has three sections, each with 16 turns, distributed over two layers. The impedance measurements and corresponding fit models for both inductors are presented in Fig. 10. The models are obtained using the vector fitting (VF) technique with enforced passivity [69], [70]. Although several inductor impedance models are proposed in the literature, their characterization process is complex and tedious [71], [72]. In contrast, the VF algorithm fits the measured impedance and generates a higher order rational function in the s-domain. This function can then be used to synthesize a high-fidelity two-terminal circuit model by using prescribed circuit building blocks [73]. The obtained model can be incorporated into a time-domain converter simulation in SPICE to quickly analyze the performance of the component without hardware prototyping, eventually speeding up the design process.

It is pertinent to mention that VF does not provide symbolic expression for inductor design purposes. This is because VF is data-driven and adjusts the number of poles/zeros in the rational function according to the provided frequency-domain response. For instance, for the direct winding prototype in Fig. 9(a), the fit rational function obtained through VF comprised one real pole and five complex pole pairs. The



(a) (b)

Fig. 9. Boost inductor winding approaches. (a) Direct (48 turns). (b) Split direct (three sections of 16 turns).

five complex pole pairs are used to model the resonances and antiresonances at high frequencies. In contrast, for the split-direct prototype in Fig. 9(b), the fit rational function comprised one real pole and one complex pole pair. Therefore, for an inductor, depending on the high-frequency response, VF yields different rational functions to accommodate the resonances at high frequencies due to winding parasitic capacitance.

Fig. 11 depicts the final equivalent circuits for the inductors, derived by translating the VF rational function using the circuit blocks proposed in [73]. The RL branch, in black, represents the primary inductance, while the $RLGC$ branches, in red, model the high-frequency behavior. The model for the direct winding prototype has multiple $RLGC$ branches, resulting in multiple series and parallel resonances. This is also evident in the impedance measurements of the direct winding inductor prototype, which exhibits resonances in the 1–50-MHz range. In contrast, the split-direct winding inductor prototype shows only one parallel resonance within the 1–50-MHz range.

During the switching transition, $\mathrm{d}v/\mathrm{d}t$ excites the series resonances, leading to ringing in the inductor current [74]. The oscillations contribute to the switching loss and bring concern about crosstalk in nearby control circuits and signal lines [75]. The ringing amplitude is related to the exciting harmonic amplitude [35], [74]. Assuming a trapezoidal approximation of the voltage pulse, the harmonic amplitude decreases with a slope of 20 dB/decade followed by 40 dB/decade. Hence, a series resonance at a high frequency will have a lower excitation than a resonance at a lower frequency.

The direct winding inductor prototype exhibits multiple series resonances, with the first series resonance occurring at a lower frequency of 6.8 MHz. Consequently, during the switching transition, the inductor current exhibits substantial modulated ringing, excited by the switching $\mathrm{d}v/\mathrm{d}t$. This modulated ringing pattern arises from the superposition of multiple series resonances as observed in the impedance response depicted in Fig. 10.

For assessing and comparing the extent of ringing under full rated power (75 kW), a SPICE simulation is performed for the dc–dc stage employing equivalent circuit models illustrated in Fig. 11. Fig. 12 presents an excerpt of the inductor current waveform for both inductor prototypes in the steady stage. The direct winding prototype exhibits pronounced, slowly decaying modulated ringing, with a 5.5% overshoot above the peak current. In contrast, the split-direct winding prototype shows

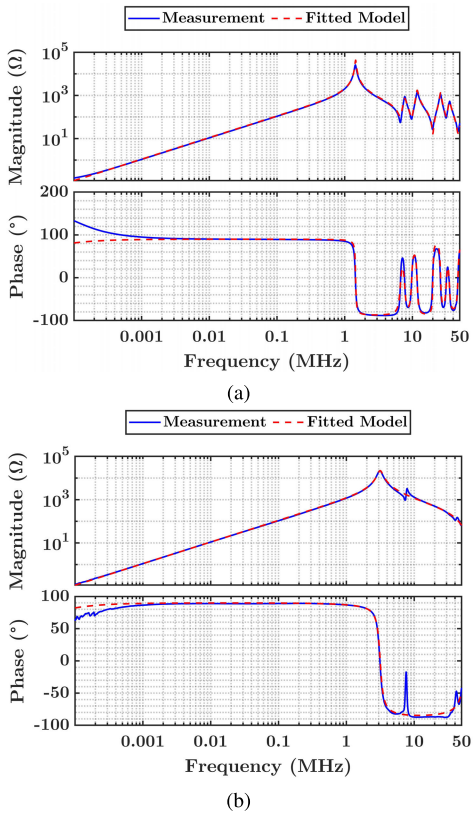


Fig. 10. Impedance measurement and fit models for the developed inductor prototypes. (a) Direct winding. (b) Split-direct winding.

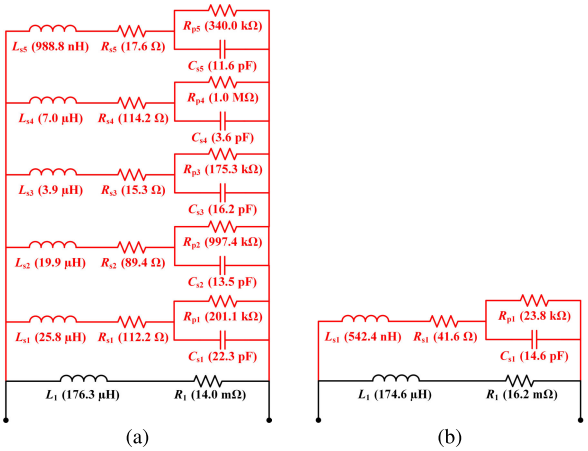


Fig. 11. Equivalent circuit models for the developed inductor prototypes. (a) Direct winding. (b) Split-direct winding.

a lower extent of ringing, with a single ringing frequency of 52 MHz and a mere 0.4% overshoot above the peak current.

Finally, based on simulation results in Fig. 12, the split-direct winding layout is selected as the final configuration for boost inductors in the dc–dc stage.

B. DC–AC Stage

The 2L-SP topology provides better device switching performance and efficiency than the 2L topology due to the decoupling of P- and N-cell parasitics by split inductors L_s [38]. However, there is currently no established guideline for designing split inductors in the literature. Hence, it is

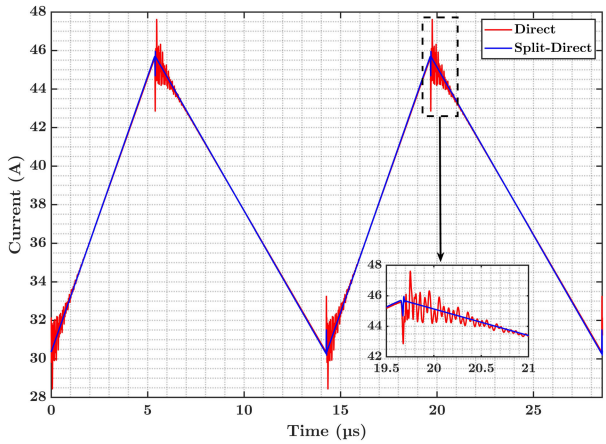


Fig. 12. Simulated inductor current comparison at 75-kW power.

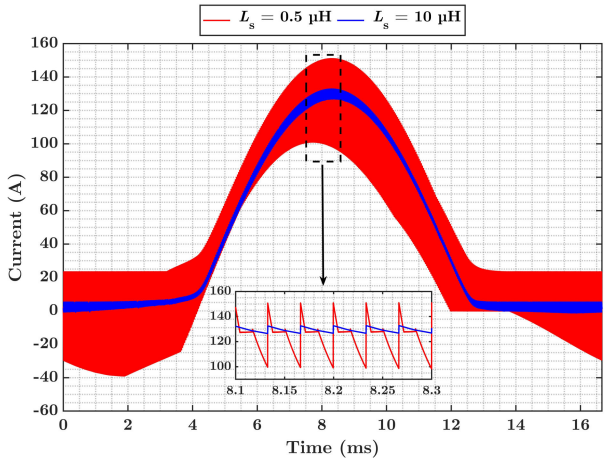


Fig. 13. P-cell L_s current comparison for $L_s = 0.5$ and 10 μH at 75-kVA output.

imperative to analyze the 2L-SP topology and develop an approach for optimal sizing of L_s.

The split inductors in 2L-SP experience current spikes Δi_s during the switching transition, incurring core losses [50]. During the switching transition, the output capacitances of the MOSFET (C_{OSS}) and diode (C_J) interact with split inductors L_s, resulting in transient voltage, which leads to a current spike. The cause of transient voltage is due to delay in the rise of node voltages due to L_s. For instance in Fig. 1, when S_{10} turns off and S_9 turns on, the voltage of midpoint of P-Cell (S_9-D_{10}) rises quickly with dv/dt of S_9, whereas the voltage of midpoint of N-Cell (S_{10}–D_9) rises with a delay t_r. The difference between these-midpoint voltages appears on L_s, leading to the current ramp-up.

Increasing the value of split inductors effectively lowers the magnitude of spikes but at the cost of bulkier magnetic design [50]. Fig. 13 compares the simulated current for one fundamental cycle (60 Hz) through P-cell's L_s for 75-kVA output for $L_s = 0.5$ and 10 μH. For $L_s = 0.5$ μH, Δi_s is considerably higher than for $L_s = 10$ μH. Furthermore, the spike magnitude Δi_s is evident to vary with the fundamental current, implying that the initial condition of L_s current $iL_s(0^-)$ affects Δi_s.

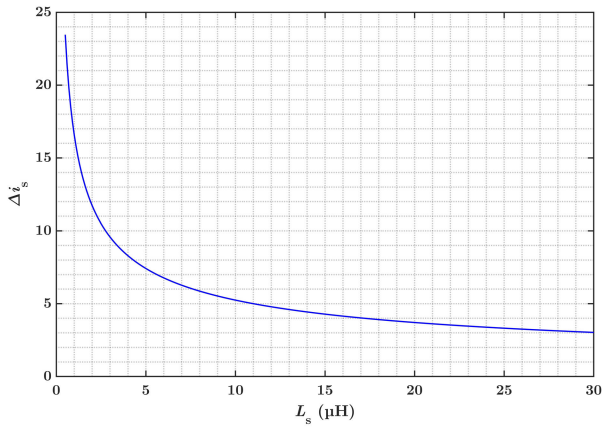


Fig. 14. Δi_s variation with L_s for $iL_s(0^-) = 0$.

A closed-form expression for Δi_s can be derived by extending and solving the equivalent circuit derived for the three-phase inverter in [50] (see the Appendix). The resulting expression for Δi_s and its associated components $v_L(t)$ and t_r are

$$v_L(t) = \frac{V_{dc}}{2}\cos\left(\frac{t}{\sqrt{2L_sC}}\right) - iL_s(0^-)\sqrt{\frac{L_s}{2C}}\sin\left(\frac{t}{\sqrt{2L_sC}}\right) \tag{2}$$

$$t_r = \sqrt{2L_sC}\tan^{-1}\left(\frac{V_{dc}}{iL_s(0^-)}\sqrt{\frac{C}{2L_s}}\right) \tag{3}$$

$$\Delta i_s = V_{dc}\sqrt{\frac{C}{2L_s}}\sin\left(\frac{t_r}{\sqrt{2L_sC}}\right) - 2iL_s(0^-)\sin^2\left(\frac{t_r}{2\sqrt{2L_sC}}\right). \tag{4}$$

$v_L(t)$ represents the transient voltage appearing across L_s until the voltage reaches the final value. t_r represents the time duration of the transient. V_{dc} is the dc link voltage, and C denotes the sum of MOSFET's C_{OSS} and diode's C_J ($C = C_{OSS}+C_J$). According to (4), the initial condition term $iL_s(0^-)$ aids in lowering Δi_s, implying that maximum Δi_s occurs for $iL_s(0^-) = 0$. Hence, from the L_s design perspective, $iL_s(0^-)$ can be set to zero to yield maximum value of Δi_s.

Fig. 14 shows the variation of maximum Δi_s with L_s for the proposed GIC converter (see Table I). The MOSFETs and diode capacitance C_{OSS} and C_J are extracted from the datasheet at 800 V. Δi_s follows an inverse relation with L_s. For lower values of split inductance ($L_s < 2$ μH), Δi_s falls steeply as L_s increases. However, for larger values ($L_s > 12$ μH), the reduction in Δi_s with increasing L_s is minimal. Therefore, increasing L_s above the knee point is not effective, as the minimal reduction in Δi_s is overshadowed by the increase in copper loss due to the increase in the number of turns required.

The selection of the optimal L_s value is contingent upon the core material, which determines the core losses P_{co} and copper losses P_{cu}. Owing to its smaller footprint and volume with optimum dc bias performance, the HF toroid core 0058191A2 from Magnetics is selected. Fig. 15 shows the variation of calculated P_{co}, P_{cu}, and the total loss $P_{Ls} = P_{co} + P_{cu}$ at 75 kVA. P_{co} is estimated using an algorithm based on iGSE, developed by authors in [76]. The algorithm splits the flux

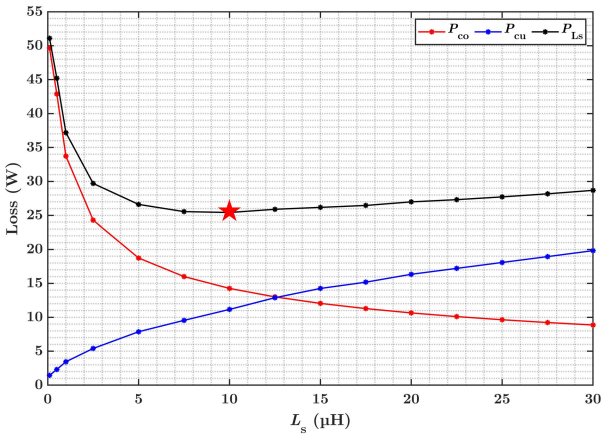


Fig. 15. Calculated P_{co}, P_{cu}, and P_{Ls} loss variation with L_s for the Magnetics 0058191A2 toroid.

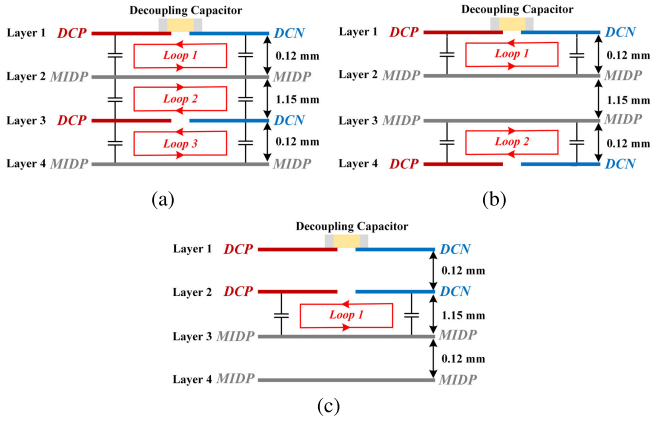


Fig. 16. Different four-layer PCB stack-up for the P-cell. (a) Layout 1. (b) Layout 2. (c) Layout 3.

density waveform into major and minor loops and sums them over the fundamental cycle.

For P_{cu} estimation, the skin effect is considered. The current through the split inductor comprises dc, fundamental frequency f_O (60 Hz), and switching/carrier frequency f_C (30 kHz) harmonics. Due to the skin effect, the ac resistance R_{ac} of the conductor is different for each frequency. For this purpose, R_{ac} of the conductor for each frequency is calculated using the formula for R_{ac} for conductors with circular cross section, as derived in [77]. The current amplitudes for different harmonics are obtained through SPICE simulation. Finally, P_{cu} is calculated by adding up the losses for dc and the first ten dominant harmonics of f_O and f_C.

P_{co}, similar to the relationship between Δi_s and L_s, exhibits an inverse relation with L_s. This inverse trend is attributed to the reduction in core losses of minor loops as L_s increases. During the switching transition, current spikes occur in L_s, forming minor loops. As L_s increases, the spike amplitude and the associated flux swing of minor loop decrease, lowering P_{co}. In contrast, P_{cu} follows a nonlinear increasing relationship ($P_{cu} \propto \sqrt{L_s}$) with L_s. This trend is attributed to an increase in the number of turns with an increase in L_s. Finally, the total underlying loss, P_{Ls}, exhibits a steep decrease for lower values of L_s. The minimum loss, with a value of 25.42 W, is achieved at $L_s = 10\ \mu$H. Beyond this minimum point, the increase in P_{Ls} is gradual. Therefore, $L_s = 10\ \mu$H is the optimal value for the given core, conductor thickness, and maximum rated current and is finalized for the dc–ac stage.

VI. Power PCB Layout Design and Optimization

Fast switching with SiC devices results in high dv/dt and di/dt during the switching transition, possibly resulting in significant voltage overshoot across the device. The extent of voltage overshoot is directly related to the power loop inductance, which comprises the device package's lead inductance and the PCB's parasitic inductance [16]. Hence, lowering the power loop inductance is desired to maximize the benefit of the fast switching capability of SiC devices. Since the device package's lead inductance is fixed and depends on the package type, the PCB inductance L_{PCB} is the only parameter that could be optimized in lowering the power loop inductance.

For PCBs, the power loop can be arranged laterally or vertically. Compared with lateral, the vertical loop layout uses a field self-cancellation method to reduce the loop inductance [28]. The PCB layers are stacked so that high-frequency current flows in opposite directions in layers, leading to flux cancellation. The extent of flux cancellation follows an inverse relation with the thickness of the board or interlayer spacing [16]. Considering the flux cancellation benefit of the vertical loop over the lateral loop, the former is chosen for the power PCB layout for both dc–dc and dc–ac stages.

Due to the high current carrying requirement and PCB cost, a 1.6-mm four-layer PCB layout with two 3-oz conductor layers per node is finalized. The conductor layer thickness is selected based on the temperature rise curves in the IPC-2221 standard [78]. The estimated temperature rise in still air at 75 kVA is around 8 °C for the dc–dc stage and 14.5 °C for the dc–ac stage PCBs. The temperature rise for the dc–dc stage is lower as each phase of the four-phase IBC carries one-fourth of the total current.

With four layers, there are three different layers stack-up possible. For instance, Fig. 16 shows the side view of three different layouts for the P-cell of the dc–ac stage phase leg. The interlayer spacing according to layer stack-up information obtained from the manufacturer for 1.6-mm total PCB thickness is also labeled. DCN, DCP, and MIDP represent the dc positive (V_{dc}), the dc negative (0), and the midpoint of the P-cell, respectively. The first PCB layout (Layout 1) employs interleaved layers, effectively creating three vertical loops that maximize flux cancellation. In contrast, Layout 2 involves interchanging the bottom two layers of Layout 1, resulting in two vertical loops. Likewise, the third Layout 3 interchanges the middle two layers of Layout 1, forming a single vertical loop.

From the perspective of L_{PCB}, it is evident that Layout 1 is optimal by achieving maximum flux cancellation due to low interlayer spacing for loops 1 and 3 and an additional small flux cancellation provided by the inner loop 2. However, it is important to consider that this layout also results in an increased overlap of layers at different potentials, introducing significant PCB parasitic capacitance C_{PCB}. The consequence of this capacitance is a potential slowdown

TABLE III
PCB PARASITICS COMPARISON

Layout	L_{PCB} (nH)	C_{PT} (pF)	C_{PB} (pF)
Layout 1	1.90	704.60	1310.35
Layout 2	2.05	638.36	1186.51
Layout 3	2.77	79.33	142.41

in device performance and an increase in switching losses, thereby negating the benefits of having a lower L_{PCB} [29].

To thoroughly analyze the influence of C_{PCB}, simulations are conducted for all three layouts (Layout 1, Layout 2, and Layout 3) using ANSYS Q3D with a solver frequency of 100 MHz. The layers are drawn according to the converter dimensions and positions of the devices finalized in the converter packaging phase. The DCP and DCN layers have vias around the decoupling capacitors to ensure that all vertical loops are effective in flux cancellation. Finally, the layers are stacked according to the respective layouts and interlayer spacing in Fig. 16.

Table III provides a comparison of extracted L_{PCB} and C_{PCB} for all layouts. C_{PT} and C_{PB} represent the total capacitance observed at the vias on the PCB where the top and bottom devices leads are soldered. Layout 1 exhibits the highest value of C_{PT} and C_{PB}, followed by Layouts 2 and 3. However compared with Layout 2, the reduction in capacitance for Layout 3 is maximum (90%). This is because, for Layout 3, the capacitance solely originates from the overlap of internal layers 2 and 3 with significantly large interlayer spacing. Furthermore, compared with C_{PT}, C_{PB} exhibits a higher value, which is primarily attributed to the increased overlap between node MIDP and DCN resulting from the symmetrical positioning of the output terminals for both P- and N-cells.

On the other hand, transitioning from Layout 1 to Layout 3 leads to an increase in L_{PCB}, but the increase in L_{PCB} is negligible compared to the lead inductance of the TO-247 package, which is approximately 9 nH [79], [80]. Therefore, Layout 3 with lowest C_{PT} and C_{PB} appears to be optimal. To corroborate this, a double-pulse test (DPT) simulation is performed in LTspice for the P-cell at rated conditions for all three layouts using the respective PCB parasitics in Table III and the selected discrete devices' SPICE model. The gate resistances R_{Gon} and R_{Goff} are set to 5and 2.47 Ω, respectively.

Fig. 17 compares the drain–source voltage $v_{DS}(t)$ and the device current $i_{DS}(t)$ for the ON and OFF transients of one device of the P-cell for all three layouts. As can be seen, $v_{DS}(t)$ for Layouts 1 and 2 falls with low dv/dt values of 15.82 and 16.75 V/ns, respectively. In contrast, $v_{DS}(t)$ for Layout 3 falls with roughly 1.8 times higher dv/dt than Layouts 1 and 2. This is attributed to the lower value of C_{PCB} (C_{PT} and C_{PB}). Furthermore, another consequence of large PCB capacitance can be seen in $i_{DS}(t)$ for Layouts 1 and 2, where the peak value for both layouts is around 1.4 times higher than for Layout 3. Likewise, for the turn-off transient in Fig. 17(b), $v_{DS}(t)$ for Layout 3 rises with a dv/dt of 37.46 V/ns, 2.1 times higher than Layouts 1 and 2. Furthermore, the difference in overvoltage amplitude between Layouts 1–3 is minimal as the

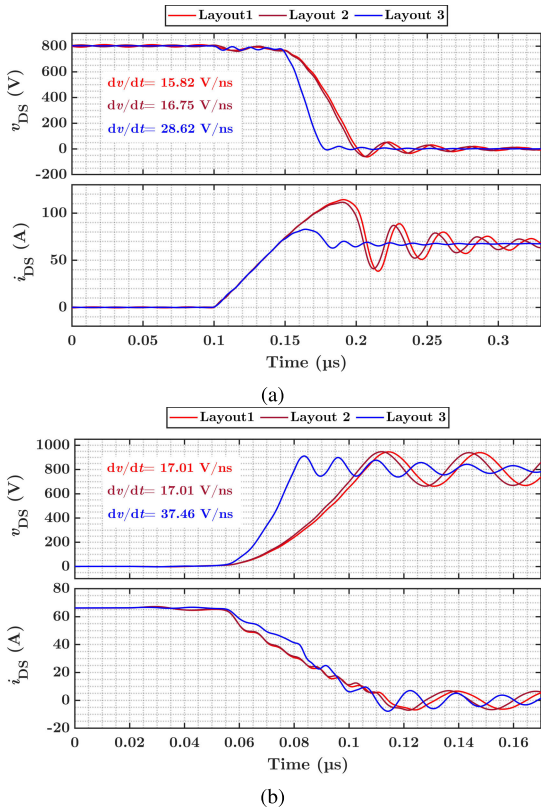


Fig. 17. Simulated comparison of $v_{DS}(t)$ and $i_{DS}(t)$ of one device of P-cell for all three layouts. (a) Turn-on transient. (b) Turn-off transient.

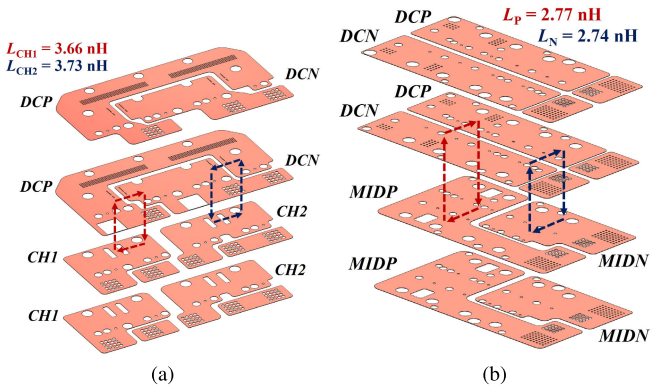
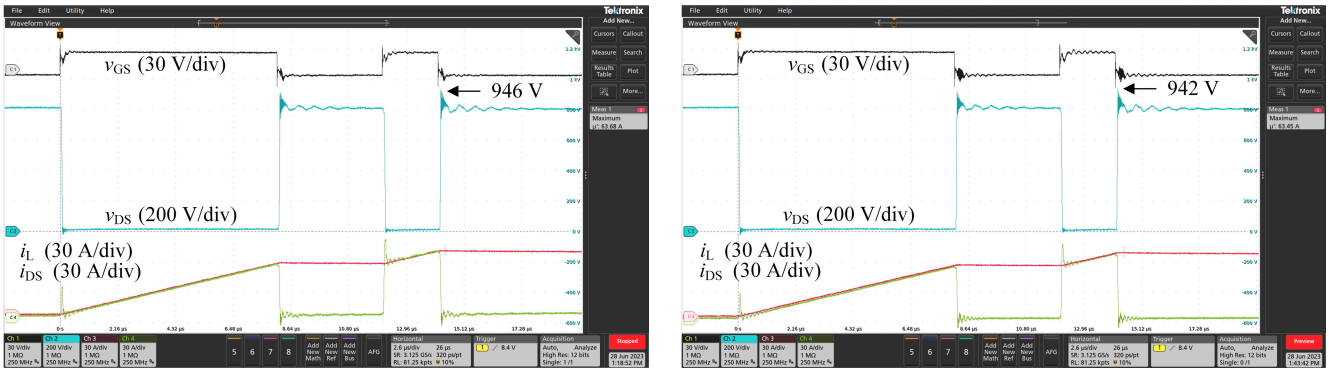


Fig. 18. Exploded view of developed PCB layouts (four layers): (a) dc–dc stage (two phases) and (b) dc–ac stage (phase leg).

increase in L_{PCB} (L_P) from Layouts 1 to 3 is smaller than the lead inductance of the TO-247 package. Moreover, in both ON and OFF transients, the waveforms for Layouts 1 and 2 are similar owing to small the difference between L_{PCB} (L_P) and C_{PCB} (C_{PT} and C_{PB}).

Based on the results in Fig. 17, it is evident that Layout 3 provides optimal switching performance and is, therefore, finalized for both dc–dc and dc–ac converter stages. Fig. 18 shows the designed PCB layout for dc–dc and dc–ac stages. For the dc–dc stage in Fig. 18(a), two phases (half-bridges) are combined in a single board with mid-points CH1 and CH2, respectively. Similarly, the dc–ac stage phase-leg PCB comprises P- and N-cells with their associated mid-points MIDP and MIDN. Due to the symmetry of the layer stack-up,



(a) (b)

Fig. 19. Bottom device DPT results for the dc–dc stage board. (a) Channel 1. (b) Channel 2.

the extracted inductance values for both phases for the dc–dc stage and P- and N-cells for the dc–ac stage are nearly equal.

Finally, the proceeding analysis suggests that if the PCB inductance for all possible layouts is smaller than the lead inductance of the TO-247 package, then the PCB layout with minimum PCB embedded capacitance is optimal.

A. Dynamic Characterization

To evaluate the dynamic performance of the designed layouts, DPTs are performed for both dc–dc and dc–ac stage boards at the rated dc link (800 V). The ON and OFF gate resistances R_{Gon} and R_{Goff} of the gate driver for both converter stages are set to 5 and 2.4 Ω, respectively. The gate resistance values are chosen to limit the percentage voltage overshoot within 20% of the device drain–source breakdown voltage V_{BR} [81], [82]. The drain–source voltage v_{DS} is measured by THDP0200 isolated differential probe from Tektronix. The device and inductor currents i_{DS} and i_L are measured using CWT Ultra Mini and CWT Mini Rogowski current probes from PEM.

For the dc–dc stage, the peak current through the device per phase is 46 A, as shown in Fig. 12. Owing to this, DPT is performed with a maximum current of 60 A at 800 V. The results for the bottom device DPT for Channels 1 and 2 with mid-points CH1 and CH2, respectively, are presented in Fig. 19. The voltage overshoot at turn-off observed for both channels is under 950 V with $\mathrm{d}v/\mathrm{d}t$ of 34 V/ns.

For the dc–ac stage, the peak current amplitude at 75 kVA is 128 A, for which two devices are paralleled per position (see Table I). Furthermore, from the switching transient perspective, split inductors L_{s} decouple the P- and N-cell parasitics during the switching transition as L_{s} is much larger than L_{PCB} and device package lead inductance. Hence, the P- and N-cell power loops are decoupled and can be characterized separately by performing DPT on each cell separately [83]. Fig. 20 shows the DPT results for both P- and N-cells at 800 V and 140 A. The voltage overshoot at turn-off observed for both channels is under 930 V with $\mathrm{d}v/\mathrm{d}t$ of 43 V/ns. Furthermore, the current among two paralleled devices is well balanced during the switching and conduction regions.

Compared with the N-cell, the device currents for the P-cell appear to have ringing. The ringing occurs because the Rogowski coil is looped around the source lead of the device instead of the drain lead. This positioning is necessary due to limitations on the bending radius of the Rogowski coil's loop wire. Consequently, the loop is vulnerable to high $\mathrm{d}v/\mathrm{d}t$ at the midpoint, as discussed in [84].

TABLE IV
CALCULATED SWITCHING LOSSES

Switching Loss	DC-DC		DC-AC	
	CH1	CH2	N-cell	P-cell
E_{ON} (mJ)	3.42	3.50	9.75	10.08
E_{OFF} (mJ)	0.79	0.83	2.61	2.84

The ON and OFF switching losses E_{ON} and E_{OFF} of the switching device are calculated from the measured DPT waveforms. To ensure V–I alignment, the procedure proposed in [85] is adopted. The switching energies are tabulated in Table IV. For N- and P-cells, the values are for the paralleled device pair. The switching loss values for both channels (CH1 and CH2) of the dc–dc stage and N- and P-cells for the dc–ac stage are nearly equal with small differences, which can be accounted for the slightly different PCB parasitics. For instance, for the P-cell layout in Fig. 18(b), the overlap between MIDP and DCN is larger than for the MIDN and DCP, leading to a slightly higher value of C_{PB}, which results in a higher E_{ON} for P-cell than N-cell.

VII. GIC HARDWARE TESTING

Fig. 21 shows the final 3-D packaged GIC converter hardware assembled on the heat sink with dc–dc and dc–ac stages. The L-shaped bus bars, connecting the dc link capacitor board and top inductor board to the side dc–dc stage boards, are 2.5 mm thick and 15 mm wide, achieving a current density of 1.33 A/mm^2. Similarly, the circular copper tabs for connecting the dc link capacitor board to dc–ac phase boards have a diameter of 10 mm, achieving a current density of 1.15 A/mm^2 at 75 kVA. For the copper bus bar, the general recommendation is to limit the current density to a maximum of 5 A/mm^2 [86]. For this value, the temperature rise of a bus bar in still air is around 20 °C [87] above ambient. The current density of the designed L-shaped bus bar and tab is much lower than 5 A/mm^2. Therefore, the expected temperature rise is much lower than 20 °C.

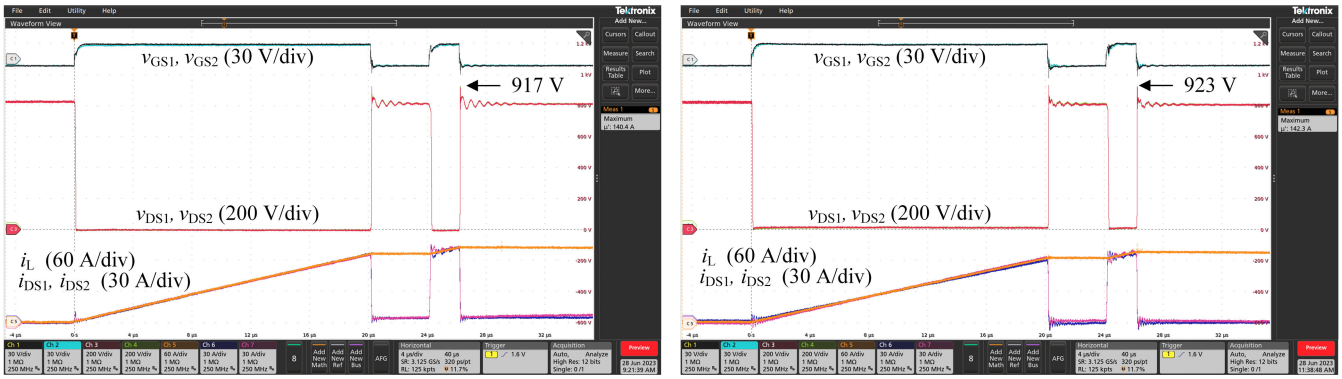


Fig. 20. DPT results for the dc–ac stage phase leg. (a) N-cell. (b) P-cell.

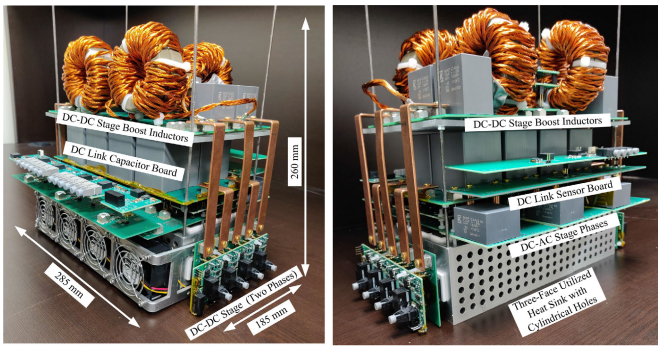


Fig. 21. GIC hardware prototype. (a) Trimetric view 1 (front). (b) Trimetric view 2 (back).

Furthermore, the heat sink is made of aluminum 6061 (T6) alloy. The alloy offers high-to-moderate strength, excellent corrosion resistance, and superior machinability and weldability. The 3-mm Al_2O_3 ceramic-based thermal pads from Fischer Elektronik are placed between the device and the heat sink. For forced cooling, four 60 × 60 mm fans with 37.5 CFM flow rate per fan are attached on the back side of the heat sink. Finally, four M3 threaded rods are tightened on the corners of the heat sink top face to provide mechanical support to the dc-Link PCB and the passive components.

The GIC converter assembly is mounted inside a National Electrical Manufacturers Association (NEMA) standard enclosure along with associated control and auxiliary components, as shown in Fig. 22. The NEMA box dimensions are $36''$ (L) × $24''$ (W) × $12''$ (H). The heat sink bottom side is mounted to the base plate through six M8 screws. The input and output power connections are drawn from a standardized connector plate, from Stäubli, attached to the bottom face of the NEMA box. For ventilation, 4×45 CFM fans are installed on the lower side wall on both sides of the NEMA box for channeling the air through the power stage components, from the top side. The control card is placed on the top side, further away from magnetics, to minimize coupling and prevent noise coupling with sensors. Furthermore, a fiber optic interface is utilized for PWM signal transmission to the gate driver to augment signal integrity. Finally, the base plate is meshed and grounded to all corners of the box enclosure.

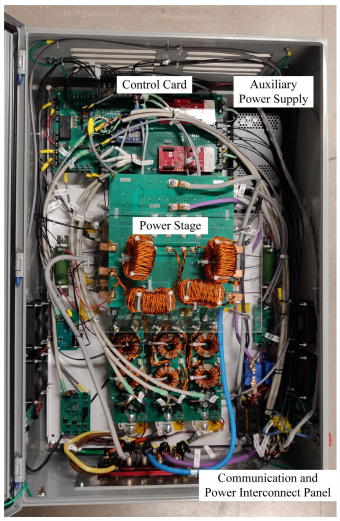


Fig. 22. GIC assembly inside NEMA box enclosure with auxiliary components.

A. Experimental Setup

A test bench is developed for testing the GIC converter and its advanced features. Fig. 23 shows the test setup. The GIC converter is supplied from the dc side at 500 V from the Spellman ST2P36 power supply capable of providing 12-kW peak power output at 800-V dc. For control, a dedicated central control terminal is setup that is interfaced to the GIC control card through the data and the control channels based on serial communication. The details about data and control channels are discussed in [88]. Through the data channel, control commands such as START/STOP sequences are sent while the control channel sends the dc–ac stage ac references at 30 kHz. For validation, SPWM is chosen for the dc–ac stage testing.

The GIC converter is systematically tested in three steps. First, the dc–dc stage is tested standalone with its control. Next, the dc–ac stage is tested. After successful independent testing of the dc–dc and dc–ac stages, the two stages are coupled and tested together.

B. DC–DC Stage Testing

For dc–dc stage control, the PI control technique is employed. The PI controller is discretized using the backward Euler technique and coded on the control card DSP with

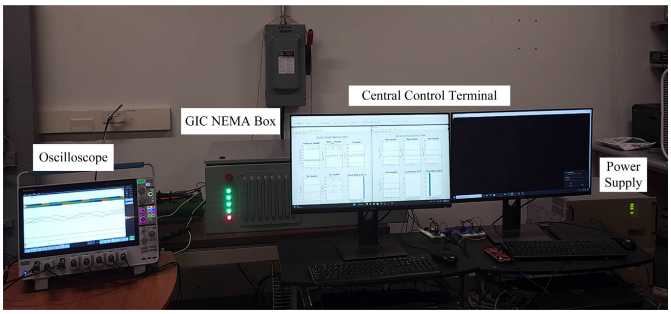
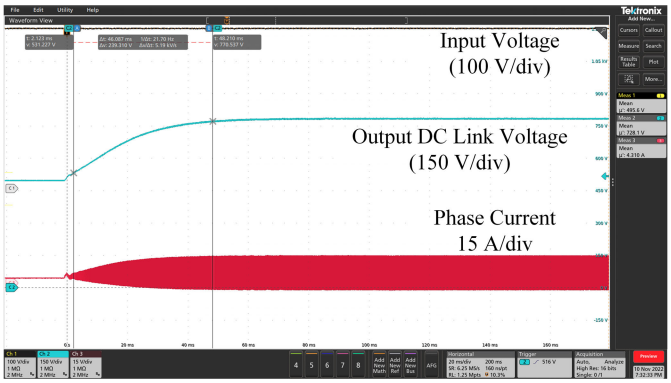
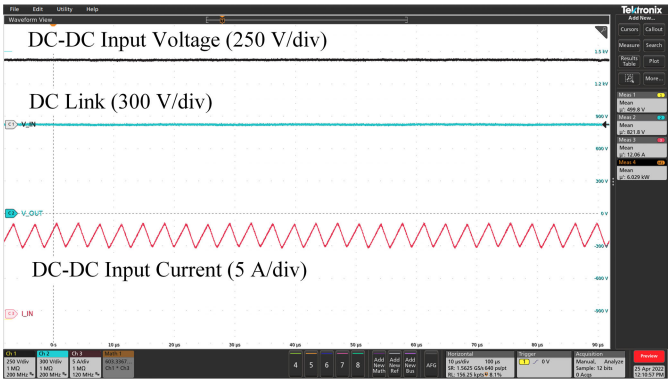


Fig. 23. Experimental setup.



(a)



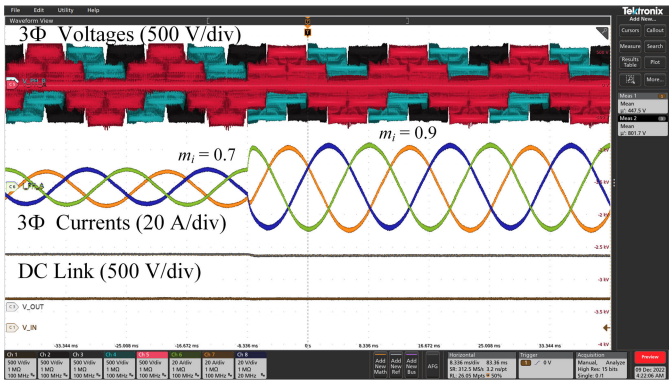
(b)

Fig. 24. DC–DC stage test results. (a) Startup. (b) Steady state.

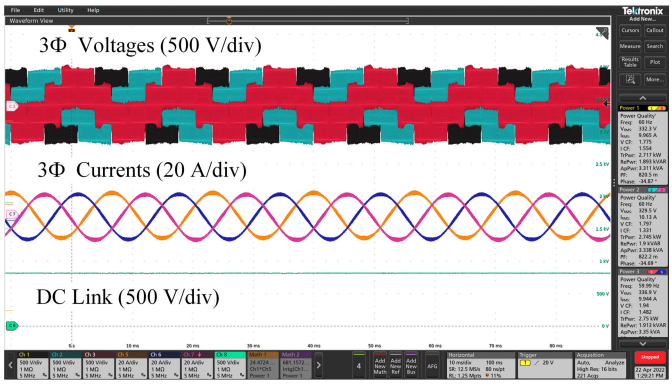
symmetric sampling [89]. The controller is first tuned on the Typhoon HIL 402 platform to determine the values of proportional K_{p} and integral K_{i} gains. The final values set are $K_{\mathrm{p}} = 0.00004$ and $K_{\mathrm{i}} = 50$. Although increasing K_p value aids in making response faster, it is kept small as increasing it causes the initial duty cycle to have an abrupt step at startup, leading to an overshoot in phase current. Fig. 24 shows the startup and steady-state waveforms. The dc link set point is set to 800 V with the input voltage V_{in} set to 500 V. The dc link voltage settles without overshoot to 800 V under 35 ms. Finally, with lower parasitics achieved by the split-winding technique, the input current is clean of current ringing, as evident in Fig. 24(b).

C. DC–AC Stage Testing

Two tests are performed to analyze the performance of dc–ac stage hardware. The corresponding test waveforms are shown in Fig. 25.



(a)



(b)

Fig. 25. DC–AC stage test results. (a) Modulation index step change. (b) Continuous at the rated output voltage.

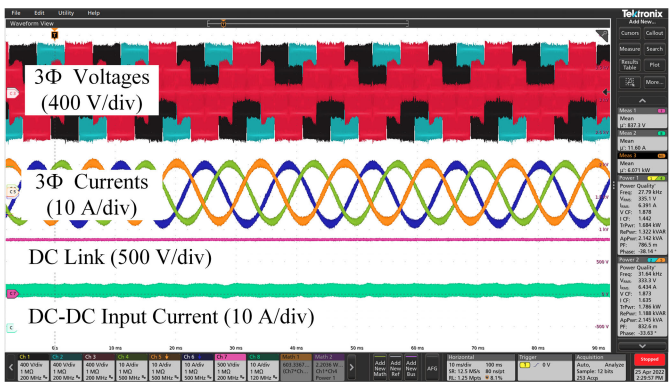


Fig. 26. Two-stage test results.

For the first test, the dynamic performance is tested [see Fig. 25(a)], where a step change in modulation index (0.7–0.9) is applied. The change can be reflected instantaneously with reduced output load current. This is followed by the second test, where the dc–ac stage is tested continuously with a 10-kVA RL load at the rated 480-V L-L rms output voltage with 800-V dc. The SPWM modulation index is set to 0.979 for the second test.

D. Two-Stage Testing

The dc–dc and dc–ac stages are coupled and tested at 10 kVA with RL load with 0.9 power factor, owing to limitations on load rating and power supply output power. The RL load is chosen because it allows active and reactive current components to flow. The active current component is

supplied from the dc–dc stage, while the reactive component flows back to the load through the dc link capacitors. Fig. 26 shows the two-stage test results. The two-stage experimental efficiency measured is 97.23%, which is higher than the reported efficiency at 10 kVA for the 75-kVA GIC developed in [17] and [19]. Furthermore, it is pertinent to mention that the measured efficiency is for the light load condition (13.3% loading) and is expected to increase at higher power.

VIII. Conclusion

With a vision to enhance efficiency and power density and address interoperability issues in WBG-based power converters for grid-interfaced applications, this article presents an electromechanical–thermal design and 3-D converter-level packaging of a SiC-based 75-kVA GIC. The GIC is a two-stage dc–dc–ac self-reliant, scalable, modular building block with standardized power interconnects. The dc–dc and dc–ac converter stages are 3-D packaged on a cylindrical hole-based heat sink to achieve optimal thermal performance and 5.5-kW/L power density, including passive components. The dc side has an input range of 500–800 V, while the ac side is a standard 480-V L-L rms. For better EMI, crosstalk immunity, and switching performance, 2L-SP topology is employed for the dc–ac stage. The power stages are built using discrete SiC devices in the TO-247 package with a two times lower cost-to-power ratio than power modules. The board layout is optimized to yield minimum board parasitic capacitance for ensuring maximum utilization of the fast switching capability of SiC. Likewise, for passive components, the split-direct winding layout is adopted for magnetics to lower distributed intralayer and interlayer winding capacitances, suppressing current ringing. Finally, the developed GIC is tested at the rated system voltage at 10 kVA. The light-load efficiency achieved at 10 kVA is 97.23%, which is expected to increase at high power.

As a part of future work, the authors' focus is on enhancing the magnetics design for both the dc–dc and dc–ac converter stages to increase power density and efficiency. For the dc–dc stage, an inverse-coupled planar inductor is being designed. Compared with the uncoupled configuration, inverse coupling between 180° phase-shifted channels lowers the channel current ripple in conjunction with the input current ripple. Furthermore, an improved core loss estimation model for split inductors is being developed for the dc–ac stage. The iGSE method employed in this article does not account for the impact of dc bias and the magnetic relaxation process resulting from constant flux. Furthermore, the authors also plan to investigate the conducted EMI performance of the developed GIC. The findings of these works will be shared in future publications.

Appendix
Derivation of Δi_s for 2L-SP Three-Phase Inverter

Fig. 27 shows the schematic of three-phase 2L-SP inverter. According to Mirza et al. [50], during switching transition, a transient voltage appears across L_s for time duration t_r leading to a current spike/ramp up. For any inverter modulation

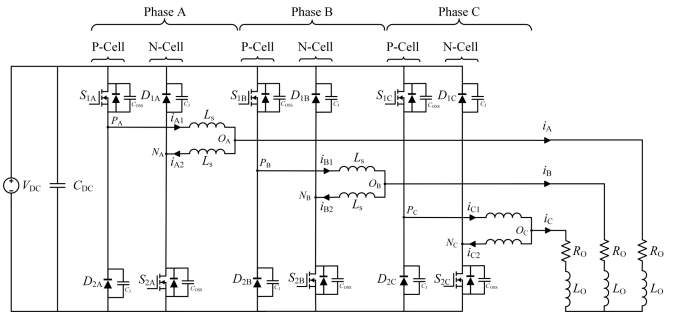


Fig. 27. 2L-SP three-phase inverter schematic.

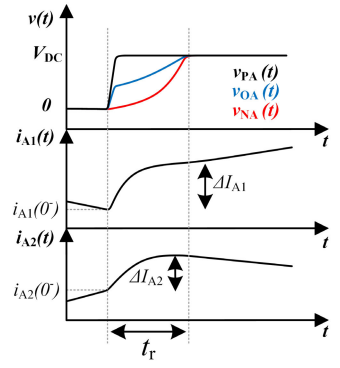


Fig. 28. S_{1A} OFF → ON and S_{2A} ON → OFF switching transition.

scheme, the switching transition happens in one phase leg at a time. The other phases are clamped to V_{dc}^+ or V_{dc}^- (power ground). Taking phase A as an example, the two switching transitions are S_{1A} OFF → ON and S_{2A} ON → OFF or S_{1A} ON → OFF and S_{2A} OFF → ON. The symbolic waveforms for S_{1A} OFF → ON and S_{2A} ON → OFF switching transition are shown in Fig. 28.

The equivalent circuit during the switching transition comprises L_s and complimentary cell's MOSFET and diode output capacitances C_{OSS} and C_J. The equivalent switching transiting circuit for phase A for S_{1A} OFF → ON and S_{2A} ON → OFF transition in the s-domain is shown in Fig. 29(a). The current sources represent the inductor currents or capacitor waveforms at the start of the switching transition. Assuming the balanced system ($i_A + i_B + i_C = 0$), the circuit can be reduced to equivalent circuit 1 [see Fig. 29(b)], where phase B and C parameters are lumped. This circuit representation can be further reduced assuming R_O and $L_O \gg L_s$, which is generally the case; otherwise, the significant output voltage will drop across L_s. Hence, the middle branch containing L_s, L_O, and R_O can be removed as its impedance is much higher than the right parallel branch containing L_s, C_{OSS}, and C_J. This yields the final reduced equivalent circuit model 2 in Fig. 29(c), which is load independent, incorporates L_s initial conditions, and is applicable for all phases.

For S_{1A} OFF → ON and S_{2A} ON → OFF, $v_s(t) = V_{dc}u(t)$ and $V_O = 0$, and for S_{1A} ON → OFF and S_{2A} OFF → ON, $v_s(t) = V_{dc}(1 - u(t))$ and $V_O = V_{dc}$ with nodes P_A and N_A swapped and I_{A2} replaced with $-I_{A1}$. $v_s(t)$ represents MOSFET's $v_{DS}(t)$, which is considered as a step voltage source.

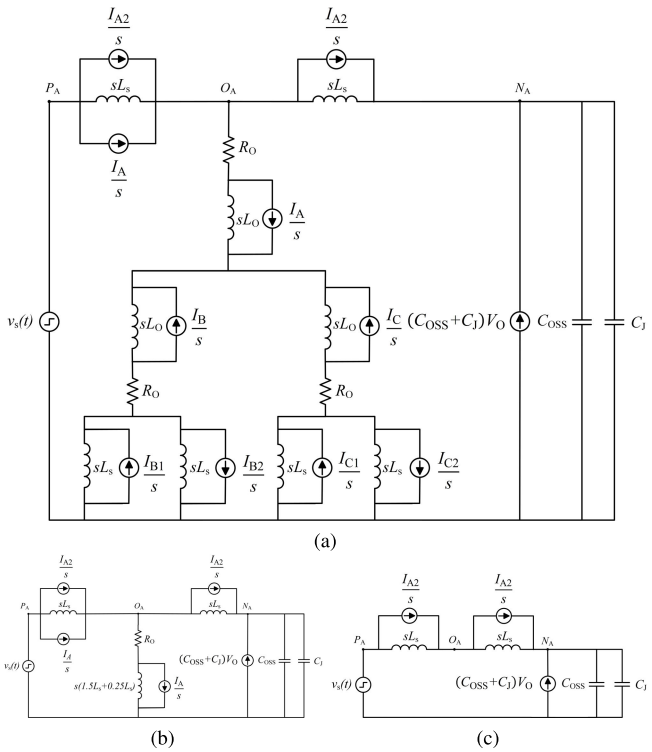


Fig. 29. Phase A S_{1A} OFF → ON and S_{2A} ON → OFF switching transition equivalent circuit model reduction. (a) Equivalent circuit 1. (b) Reduced equivalent circuit 2.

Solving final reduced circuit model with $C = C_{OSS} + C_J$ yields the expressions for $v_{OA}(t)$, $v_{NA}(t)/v_{PA}(t)$, time rise t_r, and $\Delta i_{A1} = \Delta i_{A1} = \Delta i_s$ [see (5) and (6)].

A. S_{1A} OFF → ON *and* S_{2A} ON → OFF

$$v_{NA}(t) = V_{dc}\left(1 - \cos\left(\frac{t}{\sqrt{2L_sC}}\right)\right) + I_{A2}\sqrt{\frac{2L_s}{C}}\sin\left(\frac{t}{\sqrt{2L_sC}}\right) \tag{5}$$

$$t_r = \sqrt{2L_sC}\tan^{-1}\left(\frac{V_{dc}}{I_{A2}}\sqrt{\frac{C}{2L_s}}\right) \tag{6}$$

$$v_{OA}(t) = V_{dc}\left(1 - \frac{1}{2}\cos\left(\frac{t}{\sqrt{2L_sC}}\right)\right) + \frac{I_{A2}}{2}\sqrt{\frac{2L_s}{C}}\sin\left(\frac{t}{\sqrt{2L_sC}}\right) \tag{7}$$

$$\Delta i_s = V_{dc}\sqrt{\frac{C}{2L_s}}\sin\left(\frac{t_r}{\sqrt{2L_sC}}\right) - 2I_{A2}\sin^2\left(\frac{t_r}{2\sqrt{2L_sC}}\right). \tag{8}$$

B. S_{1A} ON → OFF *and* S_{2A} OFF → ON

$$v_{PA}(t) = V_{dc}\cos\left(\frac{t}{\sqrt{2L_sC}}\right) - I_{A1}\sqrt{\frac{2L_s}{C}}\sin\left(\frac{t}{\sqrt{2L_sC}}\right) \tag{9}$$

$$t_r = \sqrt{2L_sC}\tan^{-1}\left(\frac{V_{dc}}{I_{A1}}\sqrt{\frac{C}{2L_s}}\right) \tag{10}$$

$$v_{OA}(t) = \frac{V_{dc}}{2}\cos\left(\frac{t}{\sqrt{2L_sC}}\right) - \frac{I_{A1}}{2}\sqrt{\frac{2L_s}{C}}\sin\left(\frac{t}{\sqrt{2L_sC}}\right) \tag{11}$$

$$\Delta i_s = -V_{dc}\sqrt{\frac{C}{2L_s}}\sin\left(\frac{t_r}{\sqrt{2L_sC}}\right) + 2I_{A1}\sin^2\left(\frac{t_r}{2\sqrt{2L_sC}}\right). \tag{12}$$

The expressions for t_r and Δi_s yield the same absolute value for both switching transitions. With $I_{A1} = I_{A2} = iL_s(0^-)$, the generalized expressions for t_r and Δi_s are

$$t_r = \sqrt{2L_sC}\tan^{-1}\left(\frac{V_{dc}}{iL_s(0^-)}\sqrt{\frac{C}{2L_s}}\right) \tag{13}$$

$$\Delta i_s = V_{dc}\sqrt{\frac{C}{2L_s}}\sin\left(\frac{t_r}{\sqrt{2L_sC}}\right) - 2iL_s(0^-)\sin^2\left(\frac{t_r}{2\sqrt{2L_sC}}\right). \tag{14}$$

ACKNOWLEDGMENT

The authors would like to thank Madhu Sudhan Chinthavali and Radha Krishna Moorthy from the Oak Ridge National Laboratory (ORNL) for their meticulous review and valuable feedback during the hardware development process. They would also like to acknowledge James Acquaviva, Center Director of the Advanced Energy Center (AERTC), Stony Brook University, for providing support during hardware testing.

REFERENCES

[1] M. Ahmadi, A. Shekhar, and P. Bauer, "Reconfigurability, modularity and redundancy trade-offs for grid connected power electronic systems," in *Proc. IEEE 20th Int. Power Electron. Motion Control Conf. (PEMC)*, Sep. 2022, pp. 35–41.

[2] S. Peyghami, P. Palensky, and F. Blaabjerg, "An overview on the reliability of modern power electronic based power systems," *IEEE Open J. Power Electron.*, vol. 1, pp. 34–50, 2020.

[3] D. Venkatramanan and V. John, "Dynamic modeling and analysis of buck converter based solar PV charge controller for improved MPPT performance," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 6234–6246, Nov. 2019.

[4] J. Jia, G. Yang, and A. H. Nielsen, "A review on grid-connected converter control for short-circuit power provision under grid unbalanced faults," *IEEE Trans. Power Del.*, vol. 33, no. 2, pp. 649–661, Apr. 2018.

[5] S. Belkhode, A. Shukla, and S. Doolla, "Split-output hybrid active neutral-point-clamped converter for MV applications," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 2, pp. 184–195, Apr. 2021.

[6] Q. Yang et al., "Analysis and optimization of high-frequency switching oscillation conducted CM current considering parasitic parameters based on a half-bridge power module," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12659–12674, Oct. 2023.

[7] X. Yuan, I. Laird, and S. Walder, "Opportunities, challenges, and potential solutions in the application of fast-switching SiC power devices and converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3925–3945, Apr. 2021.

[8] A. Hensler, T. Bigl, S. Neugebauer, and S. Pfefferlein, "Air cooled SiC three level inverter with high power density for industrial applications," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2017, pp. 1–8.

[9] B. Wrzecionko, D. Bortis, and J. W. Kolar, "A 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2345–2358, May 2014.

[10] R. Paul, R. Alizadeh, H. Chen, X. Li, Y. Chen, and H. A. Mantooth, "A novel integrated 1.2 kV double-sided cooled power module," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Orlando, FL, USA, Mar. 2023, pp. 372–377.

[11] H. Chen et al., "Design and optimization of SiC MOSFET wire bondless power modules," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf.*, Nov. 2020, pp. 725–728.

[12] H. Chen et al., "Feasibility design of tight integration of low inductance SiC power module with microchannel cooler," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2022, pp. 962–965.

[13] X. Li et al., "High voltage SiC power module optimized for low parasitics and compatible system interface," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2022, pp. 999–1003.

[14] X. Li et al., "EMI mitigation with stacking DBC substrate for high voltage power module," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2022, pp. 1–7.

[15] F. Diao, G. Zhu, Y. Wu, Y. Li, Z. Ma, and Y. Zhao, "A modular and performance-tunable silicon carbide half-bridge building block with digital gate driver," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2022, pp. 251–258.

[16] A. I. Emon, Z. Yuan, A. B. Mirza, A. Deshpande, M. U. Hassan, and F. Luo, "1200 V/650 V/160 a SiC+Si IGBT 3L hybrid T-type NPC power module with enhanced EMI shielding," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13660–13673, Dec. 2021.

[17] Z. Chen, C. Chen, H. S. Rizi, and A. Q. Huang, "A high power density 75kVA air-cooled SiC intelligent power stage (IPS) as a universal building block for grid applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2023, pp. 2299–2306.

[18] C. Chen, F. Luo, and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 170–186, Sep. 2017.

[19] Z. Chen and A. Q. Huang, "High performance SiC power module based on repackaging of discrete SiC devices," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9306–9310, Jun. 2023.

[20] Z. Zhang et al., "High-efficiency silicon carbide (SiC) converter using paralleled discrete devices in energy storage systems," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Jun. 2019, pp. 2471–2477.

[21] H. F. Blanchette and K. A. Haddad, "An efficient approach to design discrete packaging of BidirectionalResonant power switch for matrix converter applications," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2195–2200, Jul. 2008.

[22] S. Martin, T. Kayiranga, Y. Shi, and H. Li, "Comparative study of a 100kW PV WBG inverter using 1200 V SiC MOSFET and JFET cascode devices," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2018, pp. 399–405.

[23] (2020). *C3M0016120D SiC MOSFET—Wolfspeed*. [Online]. Available: https://assets.wolfspeed.com/uploads/2020/12/C3M0016120D.pdf

[24] Z. Chen, C. Chen, Q. Huang, and A. Q. Huang, "Design of high power converter with single low ron discrete SiC device," in *Proc. IEEE 9th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2022, pp. 209–214.

[25] H. Peng et al., "Practical design and evaluation of a high-efficiency 30-kVA grid-connected PV inverter with hybrid switch structure," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Dec. 2020, pp. 3670–3676.

[26] H. Peng, "Towards high efficiency and high power density converter: System level design, modulation, and active EMI filters," Ph.D. dissertation, Dept. Elect. Eng., Univ. Arkansas, Fayetteville, AR, USA, 2020.

[27] J. Mookken, B. Agrawal, and J. Liu, "Efficient and compact 50 kW Gen2 SiC device based PV string inverter," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2014, pp. 1–7.

[28] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2008–2015, Apr. 2014.

[29] W. Meng, F. Zhang, G. Dong, J. Wu, and L. Li, "Research on losses of PCB parasitic capacitance for GaN-based full bridge converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4287–4299, Apr. 2021.

[30] W. Taha et al., "Holistic design and development of a 100 kW SiC-based six-phase traction inverter for an electric vehicle application," *IEEE Trans. Transport. Electrific.*, early access, 2024. [Online]. Available: https://ieeexplore.ieee.org/document/10244063

[31] P. Ning, G. Lei, F. Wang, and K. D. T. Ngo, "Selection of heatsink and fan for high-temperature power modules under weight constraint," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2008, pp. 192–198.

[32] J. W. Kolar et al., "PWM converter power density barriers," in *Proc. Power Convers. Conf.*, Apr. 2007, pp. 9–29.

[33] H. Zhao et al., "Physics-based modeling of parasitic capacitance in medium-voltage filter inductors," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 829–843, Jan. 2021.

[34] J. Kotny, X. Margueron, and N. Idir, "High-frequency model of the coupled inductors used in EMI filters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2805–2812, Jun. 2012.

[35] R. A. G. Jimenez, G. G. Oggier, D. P. Fernandez, and J. C. Balda, "Analysis of current resonances due to winding parasitic capacitances in medium-voltage medium-frequency transformers," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2022, pp. 939–943.

[36] B. Narayanasamy, A. S. Sathyanarayanan, F. Luo, and C. Chen, "Reflected wave phenomenon in SiC motor drives: Consequences, boundaries, and mitigation," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10629–10642, Oct. 2020.

[37] S. Walder and X. Yuan, "Effect of load parasitics on the losses and ringing in high switching speed SiC MOSFET based power converters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2015, pp. 6161–6168.

[38] Q. Yan, X. Yuan, Y. Geng, A. Charalambous, and X. Wu, "Performance evaluation of split output converters with SiC MOSFETs and SiC Schottky diodes," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 406–422, Jan. 2017.

[39] Y. Zhao, F. Diao, Y. Wu, A. Kashyap, and S. Bontemps, "Design and demonstration of a 75 kW grid-tied inverter using low-inductance 1.7 kV silicon carbide modules," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2022, pp. 1–6.

[40] W. Xiao, M. S. El Moursi, O. Khan, and D. Infield, "Review of grid-tied converter topologies used in photovoltaic systems," *IET Renew. Power Gener.*, vol. 10, no. 10, pp. 1543–1551, Nov. 2016.

[41] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii, and I. Batarseh, "A comprehensive review of power converter topologies and control methods for electric vehicle fast charging applications," *IEEE Access*, vol. 10, pp. 40753–40793, 2022.

[42] C. Adragna, *LLC Resonant Converters: An Overview of Modeling, Control and Design Methods and Challenges*. Boston, MA, USA: Now, 2022.

[43] S. Shao et al., "Modeling and advanced control of dual-active-bridge DC–DC converters: A review," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1524–1547, Feb. 2022.

[44] C. Wang, "Investigation on interleaved boost converters and applications," Ph.D. dissertation, Bradley Dept. Elect. Comput. Eng., Virginia Tech, Blacksburg, VA, USA, 2009.

[45] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm^3 on-board power electronics for 50 kW/85 kHz automotive IPT system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 419–431, Mar. 2017.

[46] H.-B. Shin, J.-G. Park, S.-K. Chung, H.-W. Lee, and T. A. Lipo, "Generalised steady-state analysis of multiphase interleaved boost converter with coupled inductors," *IEE Proc.-Electr. Power Appl.*, vol. 152, no. 3, p. 584, 2005.

[47] H. Li, S. Munk-Nielsen, S. Beczkowski, and X. Wang, "SiC MOSFETs based split output half bridge inverter: Current commutation mechanism and efficiency analysis," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2014, pp. 1581–1588.

[48] S. Guo and A. Q. Huang, "Control and analysis of the high efficiency split phase PWM inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 2415–2420.

[49] P. Sun, C. Liu, J.-S. Lai, C.-L. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1159–1167, Mar. 2012.

[50] A. B. Mirza, A. I. Emon, S. S. Vala, and F. Luo, "A comprehensive analysis of current spikes in a split-phase inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2022, pp. 1580–1585.

[51] A. B. Mirza, A. Muneeb, S. S. Vala, and F. Luo, "Investigation of common-mode EMI in three-phase split-phase inverter," in *Proc. IEEE Symp. Electromagn. Compat. Signal/Power Integrity (EMC+SIPI)*, Jul. 2023, pp. 1–6.

[52] K. Choksi, Y. Wu, and F. Luo, "Evaluation of factors impacting reflected wave phenomenon in WBG based motor drives," in *Proc. Int. Power Electron. Conf.*, May 2022, pp. 736–740.

[53] S. Belkhode, R. Shahane, A. Shukla, and J. Wang, "A split-phase enhanced hybrid active NPC topology for PV applications with short-circuit fault tolerant capability," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Oct. 2022, pp. 1–7.

[54] *SiC Power Module BSM300C12P3E301*. Accessed: Nov. 10, 2023. [Online]. Available: https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/power_module/bsm300c12p3e301-e.pdf

[55] *SiC Power Module BSM300C12P3E201*. Accessed: Nov. 10, 2023. [Online]. Available: https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/power_module/bsm300c12p3e201-e.pdf

[56] Y. Chen, Z. Yuan, and F. Luo, "A model-based multi-objective optimization for high efficiency and high power density motor drive inverters for aircraft applications," in *Proc. IEEE Nat. Aerosp. Electron. Conf.*, Jul. 2018, pp. 36–42.

[57] Z. Yuan et al., "Design and evaluation of a 150 kVA SiC MOSFET based three level TNPC phase-leg PEBB for aircraft motor driving application," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2019, pp. 6569–6574.

[58] Z. Yuan, "Design and evaluation of high power, high efficiency and high power density motor drives for more electric aircrafts," Ph.D. dissertation, Dept. Elect. Eng., Univ. Arkansas, Fayetteville, AR, USA, 2020.

[59] C. Chen, Z. Huang, L. Chen, Y. Tan, Y. Kang, and F. Luo, "Flexible PCB-based 3-D integrated SiC half-bridge power module with three-sided cooling using ultralow inductive hybrid packaging structure," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5579–5593, Jun. 2019.

[60] A. B. Mirza, X. Xu, A. I. Emon, F. Luo, and S. Chen, "A three-face utilized heat sink design for 3-D integrated 75 kVA intelligent power stage (IPS)," in *Proc. ASME Int. Tech. Conf. Exhib. Packag. Integr. Electron. Photonic Microsyst.*, Oct. 2022. [Online]. Available: https://asmedigitalcollection.asme.org/InterPACK/proceedings-abstract/InterPACK2022/1153390

[61] X. Xu, A. B. Mirza, L. Gao, F. Luo, and S. Chen, "Topology optimization of heat sink for 3D integrated power converters," in *Proc. ASME Int. Tech. Conf. Exhib. Packag. Integr. Electron. Photonic Microsyst.*, Oct. 2022. [Online]. Available: https://asmedigitalcollection.asme.org/InterPACK/proceedings-abstract/InterPACK2022/86557/V001T09A008/1153345?redirectedFrom=PDF, doi: 10.1115/ipack2022-98066.

[62] T. L. Bergman, *Introduction to Heat Transfer: THRM 320*. Hoboken, NJ, USA: Wiley, 2015.

[63] *DC Fan DC 60 25—Sanyo Denki*. Accessed: Aug. 2, 2023. [Online]. Available: https://www.sanyodenki.com/archive/document/product/cooling/catalog_E_pdf/San_Ace_60R25_E.pdf

[64] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2001.

[65] A. B. Mirza, A. I. Emon, S. S. Vala, and F. Luo, "An integrated magnetic structure for bi-directional two-channel interleaved boost converter with coupled inductor," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2021, pp. 5466–5470.

[66] B. Hauke. (2022). *Basic Calculation of a Boost Converter's Power Stage*. Texas Instrum. [Online]. Available: https://www.ti.com/lit/an/slva372d/slva372d.pdf

[67] Q. Yu and T. W. Holmes, "A study on stray capacitance modeling of inductors by using the finite element method," *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 1, pp. 88–93, Feb. 2001.

[68] B. Liu, R. Ren, F. Wang, D. Costinett, and Z. Zhang, "Winding scheme with fractional layer for differential-mode toroidal inductor," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1592–1604, Feb. 2020.

[69] W. Tan, C. Cuellar, X. Margueron, and N. Idir, "A high frequency equivalent circuit and parameter extraction procedure for common mode choke in the EMI filter," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1157–1166, Mar. 2013.

[70] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *IEEE Trans. Power Del.*, vol. 14, no. 3, pp. 1052–1061, Jul. 1999.

[71] C. Cuellar, N. Idir, and A. Benabou, "High-frequency behavioral ring core inductor model," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3763–3772, May 2016.

[72] H. Zhao et al., "A comparative study on parasitic capacitance in inductors with series or parallel windings," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15140–15151, Dec. 2022.

[73] G. Antonini, "Spice equivalent circuits of frequency-domain responses," *IEEE Trans. Electromagn. Compat.*, vol. 45, no. 3, pp. 502–512, Aug. 2003.

[74] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Decoupling of interaction between WBG converter and motor load for switching performance improvement," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2016, pp. 1569–1576.

[75] J. Xu and S. Wang, "Investigating a guard trace ring to suppress the crosstalk due to a clock trace on a power electronics DSP control board," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 3, pp. 546–554, Jun. 2015.

[76] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, Jun. 2002, pp. 36–41.

[77] W. G. Hurley and W. H. Wölfle, *High Frequency Effects in the Windings*. Hoboken, NJ, USA: Wiley, 2013, ch. 6, pp. 159–195.

[78] IPC. (2023). *IPC-2221 Standard*. [Online]. Available: https://shop.ipc.org/ipc-2221/ipc-2221-standard-only

[79] L. Zhang, S. Guo, X. Li, Y. Lei, W. Yu, and A. Q. Huang, "Integrated SiC MOSFET module with ultra low parasitic inductance for noise free ultra high speed switching," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2015, pp. 224–229.

[80] F. Denk et al., "$R_{DS(on)}$ vs. inductance: Comparison of SiC MOSFETs in 7pin D2Pak and 4pin TO-247 and their benefits for high-power MHz inverters," *IET Power Electron.*, vol. 12, no. 6, pp. 1349–1356, May 2019, doi: 10.1049/iet-pel.2018.5838.

[81] Texas Instrum. (2011). *Ringing Reduction Techniques for NexFET High Performance MOSFETs*. [Online]. Available: https://www.ti.com/lit/an/slpa010/slpa010.pdf

[82] S. Havanur. (2017). *Power MOSFET Basics—Understanding Voltage Ratings*. Vishay. [Online]. Available: https://www.mouser.com/pdfdocs/Vishay-AN850.pdf

[83] F. Yang, Z. Wang, Z. Zhang, S. L. Campbell, and F. Wang, "Analysis and experimental evaluation of middle-point inductance's effect on switching transients for multiple-chip power module package," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6613–6627, Jul. 2019.

[84] H. Li, Z. Gao, R. Chen, and F. Wang, "Improved double pulse test for accurate dynamic characterization of medium voltage SiC devices," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1779–1790, Feb. 2023.

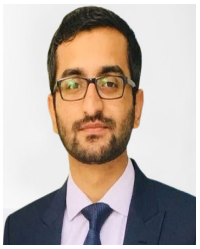
[85] E. A. Jones et al., "Characterization of an enhancement-mode 650-V GaN HFET," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2015, pp. 400–407.

[86] A. D. Callegaro et al., "Bus bar design for high-power inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2354–2367, Mar. 2018.

[87] J. M. Allocco, "Laminated bus bars for power system interconnects," in *Proc. Appl. Power Electron. Conf.*, vol. 2, 1997. [Online]. Available: https://ieeexplore.ieee.org/document/575624

[88] A. B. Mirza et al., "Hardware design and implementation of a 75 kVA 3-D integrated intelligent power stage," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2023, pp. 977–983.

[89] Y. Fong Chan, M. Moallem, and W. Wang, "Design and implementation of modular FPGA-based PID controllers," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1898–1906, Aug. 2007.

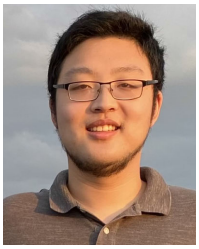


Abdul Basit Mirza (Graduate Student Member, IEEE) received the bachelor's degree (Hons.) in electrical engineering (power) from the University of Engineering and Technology, Lahore, Pakistan, in 2018, and the master's degree from Stony Brook University, Stony Brook, NY, USA, in 2022, concentrating on medium voltage direct current (MVdc) breakers using wide bandgap (WBG)-based power electronics, where he is currently pursuing the Ph.D. degree in electrical engineering.

In 2022, he was a Research Intern with GE Global Research, Niskayuna, NY, USA. He is currently a Graduate Research Assistant and is involved in research projects at the Oak Ridge National Laboratory (ORNL), Oak Ridge, TN, USA, and the Federal Aviation Administration (FAA), Washington, DC, USA. His research interests include system-level design and packaging of high-density and high-power converters; side effects (electromagnetic interference (EMI)/EMC, partial discharge, and high-frequency interactions) modeling and mitigation; and integrated magnetics design and noninvasive health monitoring of power converters using digital twin.

Kushan Choksi (Graduate Student Member, IEEE) received the B.Tech. degree in electrical engineering from Gujarat Technological University, Ahmedabad, Gujarat, in 2014, and the M.Tech. degree in power and control from the Indian Institute of Information Technology, Jabalpur, India, in 2017. He is currently pursuing the Ph.D. degree in electrical engineering with the Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY, USA.

He has 2 years of research experience at IIT Gandhinagar, Palaj, India, from 2017 to 2018, and IIT Bombay, Mumbai, India, from 2018 to 2019, as a Research Project Manager. He has recently completed an EMC internship at Tesla, Palo Alto, CA, USA, in 2022, working on system-level compliance and prognosis. His research interests include condition monitoring, diagnostics, prognostics, and control of electrical machine drives.



Austin Zhou (Graduate Student Member, IEEE) received the B.E. degree in electrical engineering from SUNY Stony Brook, Stony Brook, NY, USA, in 2020, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering.

His current research interests include the analysis, design, control, and modeling of power electronic converters. He has research experience in the domain of reliability studies, including health monitoring, fault diagnosis, and prognosis of power converters.

Sama Salehi Vala (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Tabriz, Tabriz, Iran, in 2014 and 2018, respectively. She is currently pursuing the Ph.D. degree in electrical engineering with Stony Brook University, Stony Brook, NY, USA.

She interned at Rivian, Carson, CA, USA, during the summer of 2022. In 2023, she interned at the Design Engineering Team, Tesla, Palo Alto, CA, USA. Her research focuses on the design and analysis of power electronics converters, motor drives, high-voltage power module packaging, renewable energy systems, reliability, and partial discharge mechanisms in medium-voltage motors driven by motor drives and semiconductor devices under diverse environmental conditions.

Fang Luo (Senior Member, IEEE) received the bachelor's and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, and jointly from Virginia Tech, Blacksburg, VA, USA, in 2003 and 2010, respectively.

He was an Assistant Professor with the Electrical Engineering Department, University of Arkansas, Fayetteville, AR, USA, from 2017 to 2020, and a Research Assistant Professor with The Ohio State University, Columbus, OH, USA, from 2014 to 2017. He was a Visiting Ph.D. Student and then a Post-Doctoral Researcher with Virginia Tech from 2007 to 2010 and 2010 to 2014, respectively. He is currently an Empire Innovation Associate Professor and the Director of the Spellman High Voltage Laboratory, Stony Brook University (SUNY Stony Brook), Stony Brook, NY, USA, with his background in power electronics. His research interests include high-power-density converter design, high-density electromagnetic interference (EMI) filter design and integration, and power module packaging/integration for wide bandgap devices.

Dr. Luo is also a member of the American Institute of Aeronautics and Astronautics (AIAA) and the American Society of Mechanical Engineers (ASME). He was a recipient of the NSF CAREER Award.