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First Demonstration of BEOL-Compatible 3D Vertical FeNOR

Yang Feng[1,2†], Dong Zhang[1†], Chen Sun[1], Zijie Zheng[1], Yue Chen[1], Qiwen Kong[1], Gan Liu[1], Yuye Kang[1], Kaizhen Han[1], Zuopu Zhou[1], Gengchiau Liang[1,3], Kai Ni[4], Jixuan Wu[2], Jiezhi Chen[2*], and Xiao Gong[1*]

[1]ECE, National University of Singapore, Singapore, Singapore; [2] School of Information Science and Engineering, Shandong University, Qingdao, China; [3]Industry Academia Innovation School, National Yang-Ming Chiao Tung University, Hsinchu City, Taiwan; [4]University of Notre Dame, IN, USA.

[†]Equally contributing authors; [*]Email: chen.jiezhi@sdu.edu.cn, elegong@nus.edu.sg

Abstract- In this work, we present and experimentally demonstrate the world's first back-end-of-line (BEOL) compatible vertical ferroelectric NOR (FeNOR) memory. The key highlights of this work are outlined below: (1) Side-fin structure has been meticulously designed and realized to enhance the ferroelectric switching and to suppress the cell-to-cell interference. (2) Outstanding I_{on}/I_{off} ratio (>10^6) and memory window (~4 V) has been achieved, surpassing the performance of other reported 3D FeFETs. (3) Leveraging the advantages of ferroelectric switching, low programming voltage, rapid programming speed, and good endurance have been achieved. The realization of our 3D FeNOR presents a compelling alternative for applications requiring low power consumption and high-speed operation.

1. Introduction

In the era of rapid advancements in artificial intelligence, computing-in-memory has emerged as a pivotal strategy to meet the burgeoning computational demands. Notably, non-volatile NOR type memories have garnered increasing attention in recent years for computing-in-memory applications. Nevertheless, traditional Flash NOR memories suffer from disadvantages such as high program/erase voltage, relatively low endurance, and slow program/erase speed. In contrast, HfO_2-based ferroelectric (FE) field-effect transistors (FeFETs) present an attractive alternative characterized by a low program/erase voltage, fast program/erase speed, and improved endurance characteristics. This positions them as promising candidates for NOR-type memory applications. However, the realization of 3D Ferroelectric NOR (FeNOR) has yet to be realized due to its intricate structure and the unsatisfactory ferroelectric switching dynamics within a three-dimensional architecture. This study, for the first time, realized 3D BEOL-compatible FeNOR type memories featuring a ZnO channel. Both the HfO_2 gate dielectric and ZnO channel were deposited with excellent conformality by ALD. Advanced side-fin structure was employed to enhance the ferroelectric switching and suppress the cell-to-cell interference. The experimental results showcase the fast and energy-efficient program operation of our 3D FeNOR, as well as a large memory, outstanding on/off ratio, and good endurance. All processes were performed with temperature <450 °C.

2. 3D FeNOR Device Fabrication

Key process steps for fabricating the 3D FeNOR, featuring a 3D side-fin structure and oxide semiconductor channel, are shown in Fig. 2, and detailed fabrication steps are shown in Fig. 3. Initially, a 200 nm SiO_2 layer is deposited on the Si substrate, followed by the deposition of a 100 nm-thick tungsten (W) layer and a 50 nm-thick SiO_2 layer through three cycles. Subsequently, separate gates and the channel region are etched to expose them. After this step, the sample undergoes immersion in tungsten etchant to form the side fin structure. Following this, a 7 nm HZO layer is deposited by ALD at 280 °C, followed by the ALD deposition of 7 nm TiN at 350 °C. A post-metal annealing process is conducted at 450 °C to crystallize the HZO layer. Subsequent dry etching is carried out to etch the side wall TiN, forming three separate cells. In sequence, a 10 nm HfO_2 and a 6 nm ZnO channel layers are deposited through ALD. Following this, 100 nm Ti is deposited and lifted off to form the source/drain metal. Finally, to activate the ZnO channel, forming gas at 300 °C is applied for 3 minutes. The maximum processing temperature is 450 °C during the fabrication process, affirming its back-end-of-line (BEOL) compatibility. SEM figures after critical steps are illustrated to provide a more direct and visual perspective.

3. Structure of 3D FeNOR and Ferroelectric Characterization

Fig. 4 shows the zoom-in TEM of 'cell 1' in Fig. 3 and the corresponding EDX mapping of the main elements in the side-fin MFMIS structure. Fig. 5 shows the comparison of 3D side-fin structure with the traditional 3D FeFET, taking advantage of such structure, not only small area ratio ($A_{FE}/A_{Channel}$), which is beneficial for ferroelectric switching, can be obtained, but also the cell-to-cell interference can be avoided.

Before starting the fabrication of FeNOR, we conducted the thickness dependence of HZO to obtain the optimal ferroelectricity. The GIXRD analysis is conducted for the well-crystallized capacitor shown in Fig. 6 (a). It reveals that, after annealing at 450 °C, the o-phase is the dominant phase of the HZO film, contributing to the ferroelectricity. Fig. 6 (b) presents the P-V loops of a FE capacitor with 5/7/10 nm HZO layer, demonstrating clear polarization switching, and 7 nm HZO shows largest P_r. In addition, the 7 nm HZO shows good endurance under 3.5 MV/cm electrical field cycling. Therefore, the 7 nm HZO layer is adopted during fabricating the FeNOR.

4. 3D FeNOR Characterization

In Fig. 7(a), anti-clockwise I_D-V_G loops are measured with various sweeping voltages, indicating over 10^6 I_{on}/I_{off} ratio at V_D = 0.1 V. The relationship between the MW and the maximum applied voltage is abstracted and summarized in Fig. 7(b), suggesting that the increase of the maximum voltage makes an initial enhancement in MW and then results in saturation due to the reach of maximum ferroelectric switching. Fig. 8 indicates that relationship between the wet etching time and the memory window. With the increase of etching time, the memory window goes up owning to the decreased area ratio. Fig. 9 benchmarks on/off ratio for various 3D FeFETs and 3D NOR devices. It is clear that the proposed 3D FeNOR device achieves a good on/off ratio as well as excellent I_{on} and I_{off}, especially compared with FeNAND devices.

Fig. 10 (a) displays the contour plot by varying the programming pulse width and voltage, where the small programming voltage (~4 V) can be utilized for data programming, owning to the ferroelectric switching. The benchmark for programming time and voltage amplitude is summarized in Fig. 10 (b). Compared with the high programming voltage of 3D NOR relying on the mechanism of charge tunneling, 3D FeNOR shows much lower programming voltage. The endurance test for 3D FeNOR is illustrated in Fig. 11, where decent memory window can be observed after 10^7 cycles. The retention test carried out at 25 °C manifests the non-volatile characteristic of 3D FeNOR. The potentiation and depression curves of 3D FeNOR are tested by applying multiple pulses with increasing voltage to demonstrate multi-state characteristics, as shown in Fig. 12 (a). Both the potentiation and depression show decent linearity, unrevealing its promising potential in the computing in memory field. Fig. 12 (b) shows the small conductance variations between the target weight and the programmed states. Fig. 13 (a) shows the measured array level logic operations illustrated in Fig. 13 (b), where the output current is proportional to the number of FeNOR at on state. Finally, the benchmark table is given in Fig. 14. 3D FeNOR shows excellent performance in operation voltage, programming speed, on/off ratio, and endurance.

5. Conclusions

In this work, for the first time, we have realized oxide channel 3D FeNORs with excellent electrical performance. Our work is a milestone in advancing the NOR-type memories, demonstrating great potential for compute-in-memory.

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Reference [1] D. Ielmini, *et al., Adv. Intell. Syst.,* 2020; [2] S. H. Kuk, *et al.*, IEDM, 2021; [3] K. Florent *et al.,* IEDM, 2018. [4] Min-Kyu Kim *et al., Sci. Adv.,* 2021. [5] IJ. Kim, *et al., Nat Commun*., 2023. [6] H.-T. Lue, *et al.,* IEDM 2020. [7] M.-L. Wei, *et al.,* IEDM 2022.

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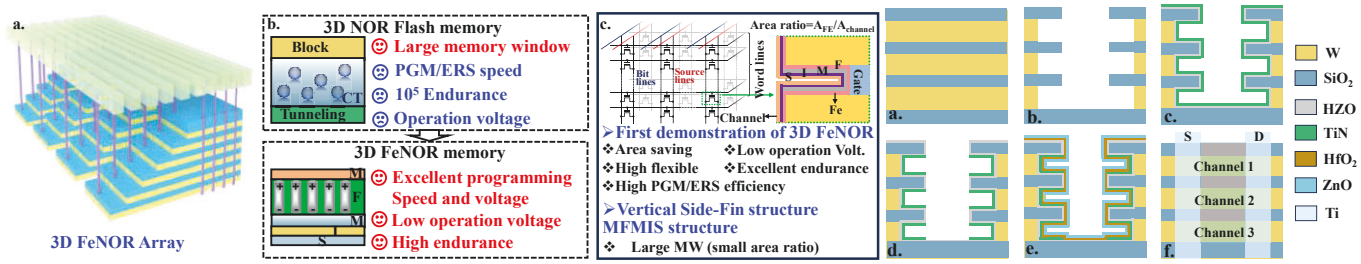


Fig. 1. (a) Schematics of the 3D FeNOR array. (b) Compared with 3D NOR Flash memory, our proposed 3D FeNOR enjoys the benefits in faster programming speed, lower power, and better reliability. (c) The key highlights of this work include: (1) The first demonstration of 3D FeNOR. (2) Oxide semiconductor as the channel. (3) A vertical side-fin MIFMIS structure with large memory window.

Fig. 2. Key process steps of fabricating the 3D FeNOR featuring a 3D side-fin structure and oxide semiconductor channel. The detailed fabrication process flow listed in Fig. 3.

a. Tungsten and SiO_2 deposition
b. Gates and holes patterning
c. 7 nm HZO deposition (ALD 280 ℃)
7 nm TiN deposition (ALD 350 ℃)
RTP annealing (450 ℃, 60 s, N_2)
d. Side wall TiN etching
e. 10 nm HfO_2 deposition (ALD 250 ℃)
5 nm ZnO deposition (ALD 150 ℃)
f. Source/Drain formation
Anneal (300 ℃, 3 min, forming gas)

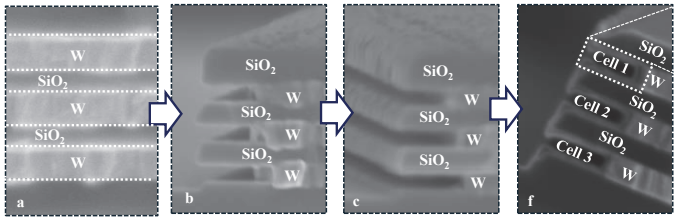


Fig. 3. Detailed fabrication steps of the proposed 3D Fe-NOR. Several key points of the process: (1) HZO, TiN, HfO_2, and ZnO were grown with good conformality using ALD. (2) The holes of side-Fin were formed with wet etching. (3) The TiN layer was etched using dry etching. (4) The highest thermal budget is 450 ℃ which is BEOL-compatible. SEM figures after critical steps are illustrated to provide a more direct and visual perspective.

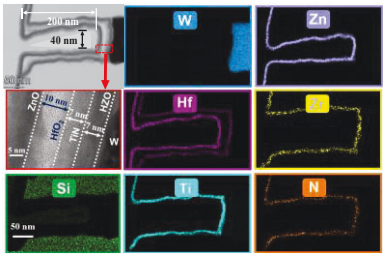


Fig. 4. Zoom-in TEM of 'cell 1' in Fig. 3 and the corresponding EDX mapping of the main elements in the side-fin MFMIS structure.

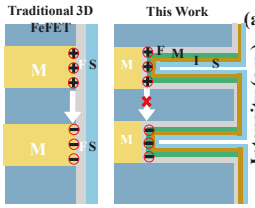


Fig. 5. MFMIS side-fin structure could reduce the cell-to-cell interference by shielding the electrical field with the SiO_2 layer.

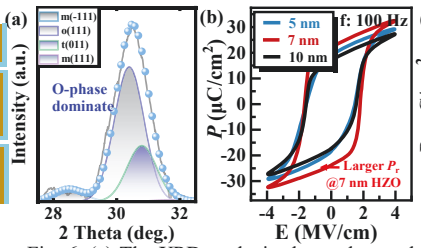


Fig. 6. (a) The XRD analysis shows that o-phase is the dominant phase in HZO. (b) The P-V loop of the Fe HZO capacitors. Among 5 nm, 7 nm and 10 nm HZO, 7 nm HZO exhibits the largest P_r. (c) Good endurance of the 7 nm HZO capacitor, under 3.5 MV/cm, is obtained.

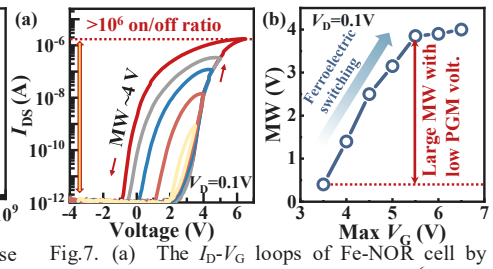


Fig.7. (a) The I_D-V_G loops of Fe-NOR cell by applying various V_G, showcasing over 10^6 on/off ratio at V_D = 0.1 V. (b) The MW manifests a pronounced increase with larger V_G, induced by more significant ferroelectric switching.

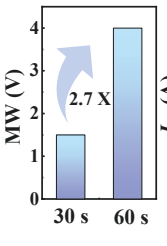


Fig. 8. The MW difference with different wet etching time.

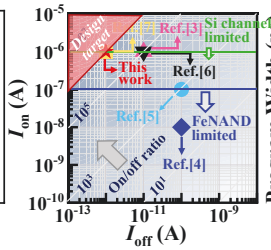


Fig. 9. Benchmark of 3D FeNOR with reported 3D FeFETs. 3D FeNOR shows higher I_{on} and I_{off} compared with reported works.

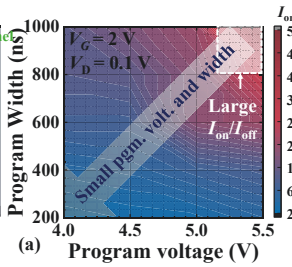
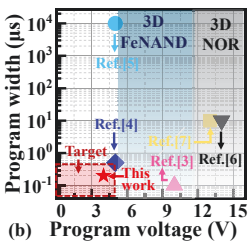
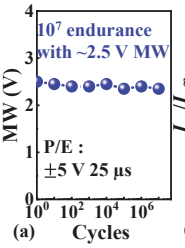


Fig. 10. (a) Contour plot showing the dependence of I_{on}/I_{off} on the program voltage amplitude and pulse width. (b) Compared with other reported device, 3D FeNOR shows high programming efficiency.





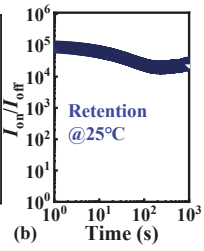


Fig. 11. (a) The device demonstrates an endurance of more than 10^7. (b) Retention test at 25°C indicates the non-volatile memory characteristics.

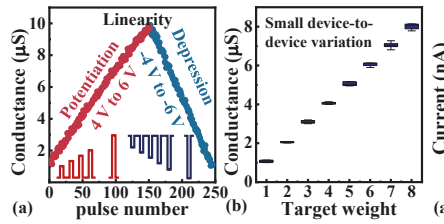


Fig. 12. (a) The potentiation and depression characteristics of the 3D FeNOR. (b) The conductance distribution suggests a small device-to-device variation of our devices.

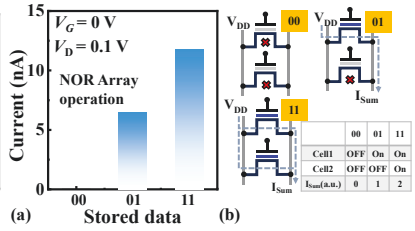


Fig. 13. (a) Measured array level logic operation of the 3D FeNOR with different storage values. (b) The schematic and the logic table of NOR arreay level operation.

	Memory	Material	MFMIS	Multibit	Oper. Volt.(V)	Pgm. Volt.(V)	Pgm. speed	MW (V)	I_{on}(A)	I_{off}(A)	On-off ratio	Endurance
This Work	3D FeNOR	ZnO	Yes	Yes	0.1	4V	200ns	4	>10^{-6}	10^{-12}	10^6	10^7
2018 IEDM[3]	3D FeNAND	Ploy-Si	No	No	1	10	100ns	2	10^{-6}	10^{-11}	10^5	10^4
2021 Sci. Adv.[4]	3D FeNAND	InZnOx	No	Yes	0.5	5	500ns	2	10^{-8}	10^{-10}	10^2	10^8
2023 Nat. Comm.[5]	3D FeNAND	InZnOx	No	Yes	0.1	5	10ms	1.5	10^{-7}	10^{-10}	10^3	10^6
2020 IEDM[6]	3D NOR	Poly-Si	No	Yes	1.8	14	10us	3	10^{-6}	10^{-11}	10^5	10^5
2022 IEDM[7]	3D NOR	Poly-Si	No	Yes	1	13	-	3	10^{-6}	10^{-12}	10^6	-

Fig. 14. The benchmark of our 3D FeNOR and other 3D devices with vertical channel. Our 3D device with ZnO channel exhibits outstanding programming speed, on-off ratio, and favorable endurance.

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