Compact Multiplexer Design with Multi-threshold Ferroelectric FETs

Sanwar Ahmed Ovy[1]*, Md Ashraful Islam Romel[1]*, Yi Xiao[2], Yixin Xu[2], Kai Ni[3], Sumitha George[1]
[1]North Dakota State University, Fargo, ND, USA, [2]Pennsylvania State University, State College, PA, USA
[3]University of Notre Dame, Notre Dame, IN, USA

***Abstract*—Ferroelectric FETs (FeFETs) are promising emerging nonvolatile memory devices due to their attractive features such as CMOS compatibility, non-volatility, multi-level cell (MLC) storage capability, and programmable threshold voltage. The majority of research efforts thus far have focused on exploring FeFETs for applications in memory and logic gates. In this work, we present a novel multiplexer design with FeFETs. Multiplexers control data flow in any integrated circuit (IC) and are major components in both ASICs and FPGAs. We leverage the programmable multi-threshold states of the FeFETs to design a compact multiplexer with a lesser number of transistors and with reduced intermediate stages compared with CMOS counterparts. The proposed design demonstrates that a significant reduction in number of transistors can be achieved by constructing a MUX utilizing multi-threshold transistors based on a pass-transistor configuration in the design. Our analysis shows, using 4 threshold voltages, the proposed design saves 2 transistors (14.29%) on 8:1 MUX, and 6 transistors (20%) on 16:1 MUX. The number of stages in the MUX tree decreases from 3 to 2 for 8:1 MUX, and from 4 to 2 for 16:1 MUX.**

***Index Terms*—Multiplexer, Multi-Level Threshold Voltages, Ferroelectric-FET, MLC.**

I. Introduction

Multiplexers (MUX) are one of the most frequently used components in processors, network switches, digital-signal-processors etc [1]. MUX is a combinational circuit that employs control signals to switch one of numerous input lines through a single regular output line. In Application Specific Integrated Circuits (ASICs), MUXes are employed in routing structures in Network on Chips(NoC), non-trivial logic implementations [2] and in peripheral circuits. In Field Programmable Gate Arrays (FPGAs), MUXes are crucial as they are the major part in Look-Up Tables [2]. For example, in the Altera Benchmark set of 120 real customer designs, it has been estimated that MUX typically accounts for over 25% of the area of an FPGA design [1]. Therefore, it is crucial to have efficient MUXes as they impact the design in terms of area, power and latency.

There are many varieties of MUX implementation including Pass Transistor (PT), Transmission gate and static logic based methods [2]. Due to implementation simplicity, low area-power consumption, minimal transistor count, pass transistor MUX designs are preferred in several applications over CMOS-based static designs [3]. Several CMOS-based arithmetic circuits such as multiplier, full-adder have been developed by leveraging PT-based MUX. There are algorithmic efforts to improve the MUX tree efficiently as well [1]. In this work we propose circuit level innovation for PT MUX trees using an emerging nonvolatile transistor, i.e., FeFETs.

*Equal contribution by 1st and 2nd authors.

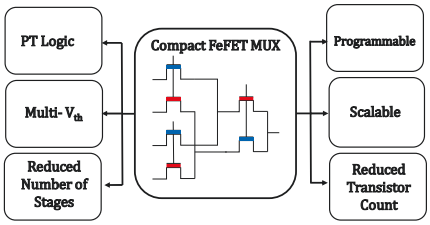

Figure 1: Features of proposed FeFET-based MUX

Ever since the discovery of ferroelectricity in doped hafnium-oxide (HfO_2), there has been increased momentum of utilizing HfO_2 based FeFET in energy-efficient logic and memory. This surge is attributed to the CMOS compatibility, scalability, retention performance, and energy efficiency observed during electric-field driven polarization switching in HfO_2-based FeFETs [4]. Additionally, by harnessing the partial polarization switching of ferroelectric thin films, multiple threshold voltage (V_{TH}) states can be achieved, presenting exciting prospects for implementing multi-level Cell (MLC) storage and multi-level logic systems based on FeFETs.

This paper addresses inherent issues with PT MUX trees, such as the exponential increase in the number of transistors and the need for more intermediate stages with larger MUX input size. The increased intermediate stages also necessitate level restorers. For the first time, this work utilizes the multi-level threshold voltages of FeFETs for a novel MUX circuit design. This results in a reduction in total transistors and intermediate stages compared to a traditional PT MUX. Our proposed designs are scalable with MUX size. As we expand the MUX size and increase the available threshold levels in transistors, proposed design leads to an increased savings in transistors and stages. Note that our proposed design methodology is not limited to FeFETs alone. It can also be applied to traditional NMOS PT designs with varying threshold levels. However, voltage controlled programmable threshold feature of FeFETs offers flexibility in tuning transistor threshold voltages, selecting operating voltage ranges, and enhanced control over noise margins. The major contributions of this paper are the following:

- Compact scalable MUX design utilizing multi-threshold voltage FeFETs.

2024 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) | 979-8-3503-5411-9/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISVLSI61997.2024.00142

2159-3477/24/$31.00 ©2024 IEEE
DOI 10.1109/ISVLSI61997.2024.00142

- Proposal for a design aimed at reducing the number of transistors and the selection chain of a MUX
- Introduction of 4:1 MUX design with 2 threshold voltage levels and 8:1 MUX design with 4 threshold voltage levels and functional verification through simulation.

The rest of the paper is organized as follows. Section II describes the background, Section III elaborates on our proposed multiplexers, Section IV discusses simulation verification and overheads and Section V presents conclusion.

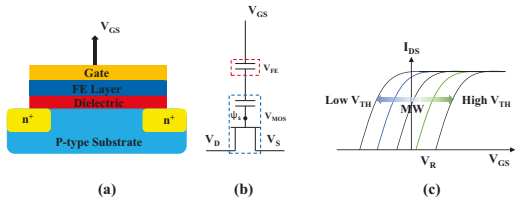

Figure 2: FeFET (a) Device [5] (b) Model [6], (c) $I_{DS} - V_{GS}$ Graph [7]

II. Background & Related Work

FeFETs integrate a ferroelectric layer into the gate stack of a MOSFET, as illustrated in Fig 2(a) [5]. Fig. 2(b) shows the equivalent circuit of the device. Ferroelectric polarization stores information which can be altered by the application of an external electric field and persists even after the removal of the external field, making it nonvolatile. Application of positive/negative write gate pulse sets the polarization pointing toward channel/gate metal, respectively, which attracts/depletes the channel electron concentration, thus setting the device to be in the low-V_{TH}/high-V_{TH} state, respectively [4]. Write pulses of different amplitudes or pulse widths can be used to access intermediate polarization states through partial polarization switching in a multi-domain ferroelectric thin film, leading to the realization of nonvolatile multi-bit storage, i.e., MLC FeFETs [8]. S. Dutta et al demonstrated multi-bit programming capability in FeFET with Tungsten(W) doped amorphous In_2O_3(IWO) channel on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$(HZO), demonstrating distinct conductance states realizing a 2-bits/cell storage [9]. T. Ali et al demonstrates multi-bit operation(1-3 bits/cell) in FeFET with HZO and HSO (Si-doped HfO_2) laminated layers and appropriate inter-layers [10]. Ni et al [11] also shows partial polarization of multi-domain ferroelectric film with write pulse width and amplitude variations. S. Deng et al [12] presents a model where ferroelectric films are composed of multiple independent domains. Fig.2(c) shows the I_d-V_g curve of a FeFET which has multi-V_{TH} programmability [7]. So far MLC FeFETs are used for memory, logic and peripherals. In this work, we specifically leverage the multi-V_{TH} characteristics of FeFET for efficiently designing pass transistor MUX tree.

Some previous works have explored FeFET for LUT and MUX design. X.Chen et al replaced the memory element with 1T-1FeFET in LUT, leaving the conventional PT-MUX tree as it is [13]. Y. Xu et al used FeFET as a routing switch [14]. Breyer et al [15] merged LUT with the first stage of the PT-MUX tree to reduce extra storage. Y. Huang et al proposed a CFeFET that serves as a 2:1 MUX with only one transistor's footprint [16]. The prime idea in this paper is the novel arrangement of FeFET transistors leveraging their multi-V_{TH} characteristics to reduce the number of devices in the MUX implementation. In the next section, we describe proposed FeFET-based MUXes.

III. Proposed Design

A. Proposed idea

In this section, to the best of our knowledge, for the first time we develop a method to reduce the number of stages and transistors in a pass transistor MUX tree by leveraging the multi-threshold voltage of the FeFETs. The core idea revolves around arranging transistors inside a block, based on their threshold voltage (V_{TH}). This arrangement enables efficient selection of MUX inputs using only two stages of transistors in series. The illustration of this arrangement and the resulting convergence of inputs is shown in Fig.3 considering 4 inputs and 4 V_{TH} levels.

First, we group the transistors into two blocks, where each block contains transistors with unique V_{TH}. Threshold voltage of transistors in the 1st stage (Block 00) follow the order: V_{TH1},V_{TH2},V_{TH3},V_{TH4} from top to bottom, while in second stage block (Block 01) follow the reverse order: V_{TH4},V_{TH3},V_{TH2},V_{TH1} from top to bottom. Transistors from first stage and second stage are connected in series in a one-to-one fashion following their placement order. Transistors in a block share a common gate biasing. Select lines to the block requires 4 unique read voltages (V_R) to control transistors with 4 V_{TH} levels. Proposed scheme maintain the following inequality ($0<V_{TH1}<V_{R1}<V_{TH2}<V_{R2}<V_{TH3}<V_{R3}<V_{TH4}<V_{R4}$)

To pass input A, gate signal of Block 00 (S_{00}) takes the value V_{R1} to turn ON the transistor (V_{TH1}) connected to A. In next stage, A goes through the transistor with threshold V_{TH4}. So, the gate voltage of this second-stage block has to be V_{R4}. V_{R4} is greater than all four V_{TH} in this block, making all transistors in 2^{nd} stage (Block 01) ON and pass their respective output from first stage. However, V_{R1} at first stage gate input won't allow any output except from V_{TH1} transistor, ensuring unique conduction path for A. Similarly, to pass input B, V_{R2} at first stage will switch on both V_{TH1} and V_{TH2} transistors, allowing both A and B to pass to next stage where they get connected to second stage V_{TH4} transistor and V_{TH3} transistor respectively. In second stage, S_{01} is biased with V_{R3} and it only turns on 3 transistors (upto V_{TH3}), thus passing only B to output. Similarly the conditions to pass input C and D is illustrated in Fig. 3 c-d. Thus,this reverse order arrangement of transistors based on V_{TH} in consecutive blocks ensures unique input selection.

Note that the traditional NMOS PTL design is an example of our design methodology with one threshold voltage and 2 selection lines at each stage. Next, we show the complete design examples of 4:1/8:1 MUX with 2/4 V_{TH} levels.

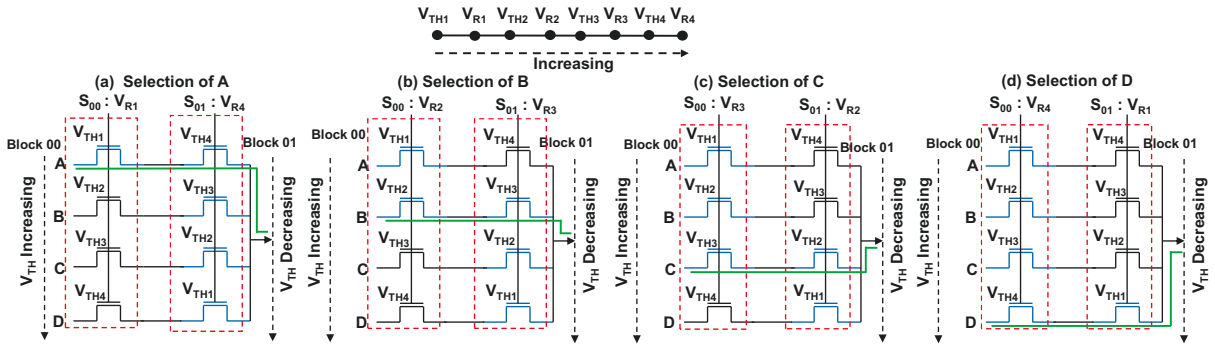

Figure 3: Basic unit of the proposed MUX scheme to illustrate unique input selection. Two stage transistor arrangement with multiple V_{TH} leads to distinctive input selection, shown with 4 inputs and 4 V_{TH} levels. Employing a reverse order of threshold voltages (V_{TH}) in successive stages facilitates the activation of a single input-output branch at a time, achieved through S_{00} and S_{01} biasing. (a-d)MUX conduction path (in green) and selection bias conditions (S_{00} and S_{01}) for transferring inputs A, B,C,D to output.

B. Design of 4:1 and 8:1 MUXes

1) Proposed 4:1 Design: Fig. 4 shows our proposed 4:1 MUX design utilizing 2 threshold levels, 2 select lines at 1^{st} stage, 1 at 2^{nd} stage. First stage consists of two blocks where each block has two transistors in placement order V_{TH1}, V_{TH2}.

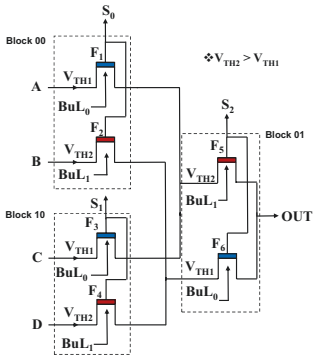

Figure 4: Proposed 4:1 MUX

Since each block has a separate select line at the first stage, we need just one block in the second stage and its inputs are shared by blocks from the first stage (Block 00 and Block 10). The transistors in the second stage follows the placement order V_{TH2},V_{TH1}. The output is taken by shorting all outgoing nodes from Block 01. The biasing voltages and threshold voltage follows the inequality: $0<V_{TH1}<V_{R1}<V_{TH2}<V_{R2}$. Compared to traditional PT-based NMOS MUX, we need a different biasing voltages on select signals to facilitate the ON/OFF of multi-threshold transistors, which is shown in Table I. Note we need to explicitly use body lines(BuLs) during the writing process to set correct V_{TH} for FeFETs. Although both NMOS based 4:1 PT MUX and proposed MUX take 6 transistors, the savings of transistors increase with MUX size and threshold voltage levels as we will see from the design of 8:1 MUX next.

2) Proposed 8:1 Design: In 8:1 MUX with 4 thresholds, transistors connecting all the inputs get divided into 2 blocks. In the first stage, each block has transistors in order V_{TH1},V_{TH2},V_{TH3},V_{TH4}. Since block 00 and block 10 have separate select lines S0 and S1, the final stage needs only 1 block. Final stage block 01 is connected to select line S2 and output nodes are shorted to get final MUX output. As shown in Fig.5(b), block 00 and block 10 connect with block 01 in a 2:1 fashion. Table II shows different biasing voltages that need to be asserted at select lines S0,S1,S2 to enable a single branch conduction and thus transfer the chosen input to output. Threshold voltages and biases follow the order: $(0<V_{TH1}<V_{R1}<V_{TH2}<V_{R2}<V_{TH3}<V_{R3}<V_{TH4}<V_{R4})$. Note, The proposed design is a two stage design compared to traditional NMOS design with 3 stages as shown in Fig.5(a). Also our design needs only 12 transistors while NMOS traditional design takes 14 transistors.

Our design is scalable. For example, for a 16:1 MUX, this approach reduces the number of stages from 4 to 2, total transistors from 30 to 24 using 4 different threshold voltage levels. Benefits increase with increased mux input size and threshold levels.Till now we have discussed about the MUX operations once the V_{TH}s are set. Next we discuss how we set different threshold voltages to 4:1 and 8:1 MUXes using separate body biasing lines.

Table I: Comparison of select lines biases between NMOS PT-based and proposed 4:1 MUX

Address	PT-based				Proposed		
	S_1	S_0	S_1'	S_0'	S_2	S_1	S_0
A	0	0	V_R	V_R	V_{R2}	0	V_{R1}
B	0	V_R	V_R	0	V_{R1}	0	V_{R2}
C	V_R	0	0	V_R	V_{R2}	V_{R1}	0
D	V_R	V_R	0	0	V_{R1}	V_{R2}	0

Table II: Comparison of select lines biases between NMOS PT-based and proposed 8:1 MUX

Address	PT-based						Proposed		
	S_2	S_1	S_0	S_2'	S_1'	S_0'	S_2	S_1	S_0
A	0	0	0	V_R	V_R	V_R	V_{R4}	0	V_{R1}
B	0	0	V_R	V_R	V_R	0	V_{R3}	0	V_{R2}
C	0	V_R	0	V_R	0	V_R	V_{R2}	0	V_{R3}
D	0	V_R	V_R	V_R	0	0	V_{R1}	0	V_{R4}
E	V_R	0	0	0	V_R	V_R	V_{R4}	V_{R1}	0
F	V_R	0	V_R	0	V_R	0	V_{R3}	V_{R2}	0
G	V_R	V_R	0	0	0	V_R	V_{R2}	V_{R3}	0
H	V_R	V_R	V_R	0	0	0	V_{R1}	V_{R4}	0

C. Programming of Transistors

FeFETs can be programmed to different threshold voltages by setting different polarization through the application of write pulses at the gate [4]. In our design, transistors with different V_{TH} are grouped in a block and they share the same gate signal(select lines). This leads to the adoption of a two-step write method and use of the body biasing to selectively

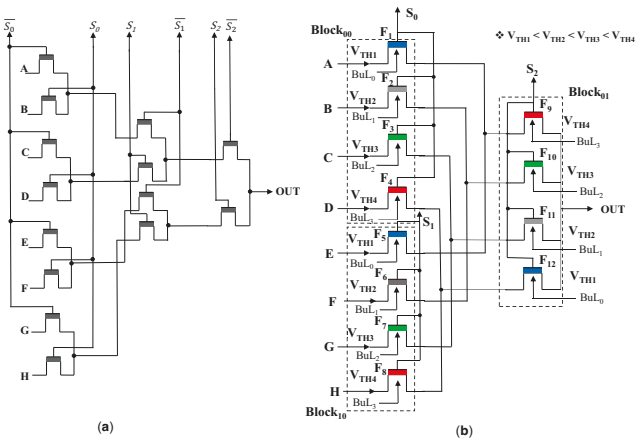

Figure 5: (a) Conventional 8:1 MUX(b)Proposed 8:1 MUX

program targeted transistors and inhibit disturb to unselected transistors [7], [17]. Initially, we set all FeFETs to the low-V_{TH} state by inducing positive polarization through the application of a positive gate write voltage (V_W), while grounding all body terminals (BuL_s) and MUX inputs. Next, we selectively reset the transistors to high-V_{TH} state by applying a negative write voltage to the gate, grounding the body of the target cells, and simultaneously setting all other body terminals (BuL_s) to 50% of the negative write voltage to prevent write upsets. For 4:1 and 8:1 MUX design, first, we set all transistors to LVT(V_{TH1}). In the second step, we apply negative write voltage(-V_W) to all select lines and zero body biasing to BuL_s of targeted cells for setting the targeted cells to (V_{TH2}). Body biasing (-V_W/2) voltage is applied to BuL_s of non-targeted cells for inhibiting non-targeted cell's polarization upset.

For 8:1 MUX, we reset designated cells to HVT1(V_{TH2}), HVT2(V_{TH3}), HVT3(V_{TH4}), by applying -V_{W1}, -V_{W2},-V_{W3} to select lines in step 2,3 and 4. Body biasing is set to -V_{W3}/2 in steps 2,3 and 4 such that it will inhibit the unselected cells state change. We initially set all transistors to LVT (V_{TH1}), given recent findings [17] suggesting that employing a raised voltage body biasing scheme to prevent write upsets may not be effective when setting cells to LVT.

IV. Results and Discussions

We use Virtuoso ADE-XL simulator environment with open-source NCSU 45nm Basekit and a multi-domain FeFET model [6] [12] for our simulation and analysis. For simulations we consider 20 domains in FeFET. We verify the functionality of the proposed 8:1/4:1 MUX designs, detailed below.

A. Proposed 4:1 MUX

Fig.6 demonstrates the functional simulation of the proposed 4:1 MUX shown in Fig.4. First, we program FeFETs to their respective threshold levels. Second, we verify the MUX functionality by selecting different inputs. For our simulations, we choose V_R values on select lines such that output gets more than 98% of the input voltage, and magnitude and read period of V_R's do not upset FeFET polarization (V_{TH}).

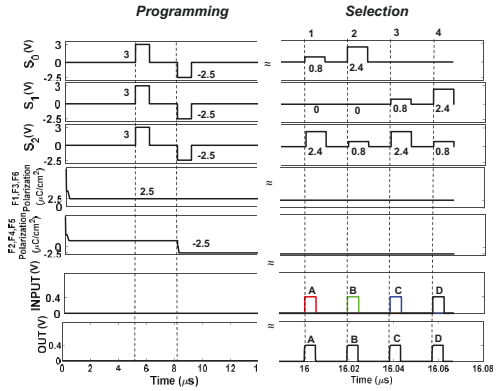

Figure 6: Transient response of proposed 4:1 MUX

1) Programming of FeFET: We program FeFETs F_1, F_3, F_6 to V_{TH1} and F_2, F_4, F_5 to V_{TH2} (refer Fig. 4). We adopt a two step write approach by writing all FeFETs to V_{TH1} state first, and then selectively converting chosen FeFETs to V_{TH2} as mentioned in section IIIC. We assert write voltage 3V on selection lines (S_0,S_1,S_2) from 5 μs to 6 μs, and all FeFETs (F_1-F_6) get set to polarization state 2.5 $\mu C/cm^2$ (corresponding to V_{TH1}). We ground all inputs (A-D) and body biasing lines (BuL_s) during this time. In the second step, we apply write pulse of -2.5 V to select lines (S_0,S_1,S_2) from 8 μs to 9 μs and polarization of F_2, F_4, F_5 get reset to -2.5 $\mu C/cm^2$ (corresponding to V_{TH2}). We prevent the polarization upset of F_1, F_3, F_6 by applying more than half the write voltage to their body biasing lines (BuL_0 = -1.375 V) and thus retain their previous V_{TH1} threshold. V_{TH1}/V_{TH2} are approximated around 0.4V/2.0V.

2) MUX Operation : Selection segment of Fig. 6 demonstrates MUX selection operations. In each selection cycle, we keep only one input at logic 1 (400 mV) and all other inputs at logic 0 (GND). We select specific inputs by applying a unique combination of read voltages on selection lines as mentioned in Table I. To select A, we assert 0.8V, 0V and 2.4V on lines S_0, S_1 and S_2 respectively. This turns transistors F_1, F_5 and F_6 (refer Fig. 4) ON and input A gets transferred though the unique path established by F_1 and F_5 to output. To select B/C/D, we assert (2.4V, 0V, 0.8V)/(0V, 0.8V, 2.4V)/(0V, 2.4V, 0.8V) on (S_0, S_1, S_2).This turns a unique combination of transistors "ON" establishing a unique conducting path and transferring B/C/D to output in selection cycles 2/3/4.

B. Simulation of 8:1 MUX:

Fig.7 demonstrates the functional simulation of the proposed 8:1 MUX from Fig.5(b). The programming and selection operations are explained below.

1) Programming of FeFET: The programming segment of Fig.7 shows the write process to set threshold voltages. We set FeFETs to V_{TH1},V_{TH2},V_{TH3} and V_{TH4} by writing FeFET's polarization states to 2.5$\mu C/cm^2$, 0$\mu C/cm^2$, -2.5$\mu C/cm^2$ and -5$\mu C/cm^2$ respectively. Here, we adopt a multi-step write approach by programming all FeFETs to V_{TH1} state initially and then selectively changing chosen FeFETs to other

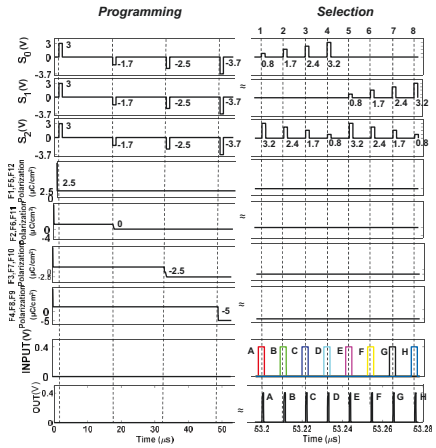

Figure 7: Transient response of proposed 8:1 MUX

threshold voltage states as mentioned in section IIIC. First, all FeFETs are provided with 3V signal ($1\mu s$) through S_0, S_1, and S_2 to set $2.5\mu C/cm^2$ polarization.At this time, we keep all inputs (A-H) and all body biasing signals (BuL_s) grounded. Polarization $0\mu C/cm^2$ is set with a write pulse of -1.7V ($1\mu s$) applied to F_2,F_6, and F_{11} through S_0, S_1, and S_2 (Fig.5(b)). Similarly, -2.5V is applied to set polarization $-2.5\mu C/cm^2$ to F_3,F_7, and F_{10}. Finally, -3.7V is applied to all gate terminals to achieve polarization $-5\mu C/cm^2$ for F_4,F_8, and F_9. To prevent polarization upset of non-targeted FeFETs, the body signals (BuL_s) of all non-targeted FeFETs are kept at -2.22V(60% of -3.7V) after the first step. V_{TH1}/V_{TH2}/V_{TH3}/V_{TH4} are approximated around 0.4V/1.2V/2V/2.75V

2) Selection of Individual Input: Fig.7 shows the selection part in $53.19\mu s$ to $53.29\mu s$ window. In each cycle, we keep only one input at logic 1 and all other inputs at logic 0. For the unique selection of inputs(A-H), 3 different read voltages need to be applied to select lines(refer Table II). Each read pulse duration is limited to 1.8ns, so it turns on FeFETs but does not upset polarization states. To pass input A to output(selection cycle 1), (S_0,S_1,S_2) combination is (0.8V,0V,3.2V). This turns ON FeFETs $F_{1,9,10,11,12}$ and establishes a conducting path through F_1 and F_9. To select input B/C/D/E/F/G/H(selection cycles 2-8), (S_0,S_1,S_2) are asserted with (1.7V, 0V, 2.4V)/(2.4V, 0V, 1.7V)/(3.2V, 0V, 0.8V)/(0V, 0.8V, 3.2V)/(0V, 1.7V, 2.4V)/(0V, 2.4V, 1.7V)/(0V, 3.2V, 0.8V) respectively. Fig 7 shows how each of these select line biasing combination conducts different input values at different cycles.

C. Discussion and overheads

Our analysis shows that the proposed Multi-V_{TH} FeFET design yields a compact MUX. However, dealing with multiple V_{TH} introduces complexity in biasing schemes. The proposed scheme requires different levels of biasing voltages and control circuitry to apply these biases upon the selection of a specific input. The usage of transistors with high V_{TH} values increases the delay through individual transistors, some of this delay is offset by the reduction in the number of intermediate stages in the MUX tree.

Also, usage of higher threshold voltages leads to increased read voltage requirements. This might cause V_{TH} upsets of other transistors in the same block. Moreover, setting FeFETs to different V_{TH} requires a range of write bias voltages. While using regular NMOS transistors with fixed threshold voltage eliminates the complexity in writing V_{TH} and V_{TH} upsets, it lacks the flexibility of FeFETs' V_{TH} tuning and the associated flexibility in operating voltage ranges. This flexibility in operating voltages provides tunable energy consumption for various applications.

V. Conclusion

This work has proposed a novel FeFET based multiplexer design utilizing its multi- level threshold voltages. The design outperforms conventional NMOS MUX design in 2 different ways; one in total number of transistors, second in reduced number of stages. We also presented 4:1/8:1 MUX design and verified their functionality. Our analyses shows, using 4 threshold voltages, the proposed design saves 2 transistors (14.29%) on 8:1 MUX and decreases number of stages in the MUX tree from 3 to 2.

VI. Acknowledgement

This work is supported in part by NSF 2246149 and in part by NSF 2346953.

References

[1] K. Jabeur *et al.*, "High performance 4:1 multiplexer with ambipolar double-gate fets," in *2011 18th ICECS*.
[2] E. Giacomin *et al.*, "Low-power multiplexer designs using three-independent-gate field effect transistors," in *2017 NANOARCH*.
[3] C. Scholl *et al.*, "On the generation of multiplexer circuits for pass transistor logic," in *DATE, Europe*, 2000.
[4] H. Amrouch *et al.*, "Ferroelectric fet technology and applications: From devices to systems," in *2021 ICCAD*.
[5] S. George *et al.*, "Nonvolatile memory design based on ferroelectric fets," in *Design Automation Conference (DAC)*, 2016.
[6] K. Ni *et al.*, "A circuit compatible accurate compact model for ferroelectric-fets," in *2018 IEEE Symposium on VLSI Technology*, 2018.
[7] N. Xiu *et al.*, "Capacitive content-addressable memory: A highly reliable and scalable approach to energy efficient parallel pattern matching applications," in *GLSVLSI 21*.
[8] H. Mulaosmanovich *et al.*, "Evidence of single domain switching in hafnium oxide based fefets: Enabler for multi-level fefet memory cells," in *2015 IEDM*.
[9] S. Dutta *et al.*, "Monolithic 3d integration of high endurance multi-bit ferroelectric fet for accelerating compute-in-memory," in *IEDM*, 2020.
[10] T. Ali *et al.*, "A multilevel fefet memory device based on laminated hso and hzo ferroelectric layers for high-density storage," in *2019 IEDM*.
[11] K. Ni *et al.*, "Critical role of interlayer in hfzr0.5o2 ferroelectric fet nonvolatile memory performance," *ITED*, 2018.
[12] S. Deng *et al.*, "A comprehensive model for ferroelectric fet capturing the key behaviors: Scalability, variation, stochasticity, and accumulation," in *ISVLSI*, 2020.
[13] X. Chen *et al.*, "Power and area efficient fpga building blocks based on ferroelectric fets," *IEEE Transactions on Circuits and Systems*, 2019.
[14] Y. Xu *et al.*, "Ferroelectric fet-based context-switching fpga enabling dynamic reconfiguration for adaptive deep learning machines," *Sci. Adv.*
[15] E. T. BREYER *et al.*, "Compact fefet circuit building blocks for fast and efficient nonvolatile logic-in-memory," vol. 8, pp. 748–756, 2020.
[16] Y.-Y. Huang *et al.*, "Novel complementary fefet- based lookup table and routing switch design and their applications in energy/area-efficient fpga," in *EDTM 2023*.
[17] Y. Xiao *et al.*, "On the write schemes and efficiency of fefet 1t nor array for embedded nonvolatile memory and beyond," in *2022 IEDM*.