IBIS Model Simulation Accuracy Improvement by Including Power-Supply-Induced Jitter Effect

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***Abstract*—The power-aware input/output buffer information specification (IBIS) model does not correctly account for the delay change caused by supply-voltage noise. This article presents a new modification algorithm that improves the accuracy of the IBIS model by including the power-supply-induced jitter (PSIJ) sensitivity effect; more specifically, the dc-jitter-sensitivity effect. The procedure of extracting the key parameters and modifying the switching coefficients is presented and applied in a real design. The performance of the modified IBIS model is validated using two designs, and the simulation accuracy is improved significantly compared with that of the traditional IBIS model. The improved IBIS model is applicable to situations when there is dc or ac noise on the power rail. The predriver propagation delay can also be characterized in the simulation by including the predriver PSIJ effect. The algorithm is efficient while straightforward and easily implemented by introducing just one parameter to the IBIS model.**

***Index Terms*—Input/output buffer information specification (IBIS), jitter sensitivity, modification algorithm, power-supply-induced jitter (PSIJ), propagation delay, switching coefficient.**

I. Introduction

THE input/output buffer information specification (IBIS) model is a behavioral model that uses lookup tables (*I–V* and *V–T* relationships) to describe the electrical behavior of a device directly. Compared with the SPICE model, in which electrical behavior is calculated from the circuit element electrical parameters and transistor models, the IBIS model simulates faster because the voltage/current/time relationships are already given for the external nodes of the entire buffer [1]. Furthermore, there are no transistor-level circuits involved in the IBIS model, so it protects proprietary design information.

The IBIS model has been continuously improved since the IBIS Open Forum was formed and the first IBIS specification was released in 1993 [2]. More than 200 buffer issue resolution documents have been submitted to the IBIS Open Forum to help improve the IBIS performance from version 1 to version 7.2. Furthermore, many research works have promoted the development of the IBIS model. The study in [3] provided an approach for reconstructing an analog SPICE behavioral model based on the information provided by the IBIS model. An approach for IBIS model transient simulation using the latency insertion method is proposed in [4] to offer better convergence than the traditional methods. A solution for better simultaneous switching noise (SSN) representation to properly include SSN information in the circuit with IBIS models was proposed in [5]; and methods for improving SSN simulation accuracy are discussed and validated in [6]. Up to date, research has also focused on finding alternative accurate and efficient ac power-aware snubber models. Souilem et al. [7] propose an analytical input–output (IO) buffer model that includes supply/ground voltage variations at the buffer input and output stages. Machine learning techniques are also widely used in the behavioral modeling. In [8], it demonstrates an IBIS algorithmic modeling interface (IBIS-AMI) model obtained from machine learning for time-domain simulation.

Another aspect that is attracting increasing attention is the tighter timing requirements for high-speed I/O. Simulated driver output transition behavior needs to be accurate enough to meet the requirements in design and production, especially power-supply-induced jitter (PSIJ), which is the time variation in the driver output transition edges from their ideal positions due to power-rail-voltage fluctuations. Different analytical methods for predicting PSIJ have been studied. In [9], it proposed the analytical transfer functions to relate the power and ground voltage fluctuations to the jitter for a single-ended buffer. The power-supply rejection ratio (PSRR) based jitter models in [10] gave generalized expressions for different types of drivers. The power-aware IBIS model, which considers the power/ground effect in a nonideal situation, has also been developed to overcome the "gate modulation effect" that the actual drive strength of the gate may vary depending on the instantaneous value of the supply voltage with the simultaneous switching output noise. The proposal in [11] considered the current required to flow into the power and ground rails allowing for a more accurate analysis of ground and power bounce associated with SSN. In addition, the gate modulation effect can be included by modifying the IBIS model switching coefficients, as stated in [12]. However, the accuracy of the PSIJ simulation remains poorer than that of the SPICE simulation. An IBIS switching-coefficient modification algorithm to improve the IBIS model output PSIJ simulation accuracy by considering the power-rail-voltage time-averaged

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effect has been proposed [13]. However, the key parameters extracted for the modification process are not only purely related to the power-rail voltage but also to the process corner. The simulated output propagation delay change is not caused by supply-voltage change alone.

In this article, an algorithm for improving the accuracy of IBIS model PSIJ simulation is proposed. The IBIS model switching coefficients are amended by introducing a single parameter, i.e., driver dc-jitter sensitivity, to characterize the PSIJ behavior. This parameter is easy to extract and compatible with the IBIS format. The predriver effect can also be included in the switching coefficients. The rest of this article is organized as follows. The details of the proposed algorithm are given in Section II. The algorithm was then applied in a self-built model and a practical model in Section III. The driver output PSIJ sensitivity of the self-built model with different load conditions under dc power noise and ac power noise situations was assessed. The practical model contains a predriver stage, and the complete model was simulated with dc power noise under different load terminal conditions to evaluate the IBIS model output performance. Compared with the conventional IBIS model simulation, the amended IBIS model shows dramatic improvements in the driver output jitter-sensitivity modeling. The difference between the IBIS-simulated PSIJ sensitivity and the SPICE simulation result is reduced to within 15%. Finally, Section IV concludes this article.

II. Jitter-Sensitivity-Based IBIS-Modification Methodology

In this section, the limitations of the power-aware IBIS model from the perspective of PSIJ simulation will be introduced in detail. The improved IBIS model with an algorithm considering the time-averaged power-rail-voltage effect and the PSIJ effect will be given.

A. Limitation of the Current Power-Aware IBIS Model

The power-aware IBIS model is an improvement over the traditional non-power-aware IBIS model by including the gate modulation effect and the ratio modification on the K_{pu} and K_{pd} switching coefficient [11], [12]. After modification, the K_{pu} becomes $K_{sspu}(V_{pu})K_{pu}$, where the K_{sspu} is the modification ratio depends on V_{pu}, and the K_{pd} becomes $K_{sspd}(V_{pd})K_{pd}$, where the K_{sspd} is the modification ratio depends on V_{pd}. However, these coefficients are only functions of the pull-up and pull-down voltage. Thus, the model cannot track output timing delay changes caused by nonideal power voltage [14]. For example, for an inverter chain as an output driver, as shown in Fig. 1, the typical, minimum, and maximum supply power voltages are 1.8 V, 1.7 V, and 1.9 V, respectively. The output transition behaviors of a SPICE circuit simulation, non-power-aware IBIS simulation, and power-aware IBIS simulation for situation where the power-supply voltage varies from the three values above are shown in Fig. 2. From the SPICE circuit simulation results, for the driver output rising and falling edge, the delay difference caused by the supply-voltage difference is clearly shown. However, the propagation delay change is not correctly characterized in either non-power-aware or power-aware IBIS simulations.

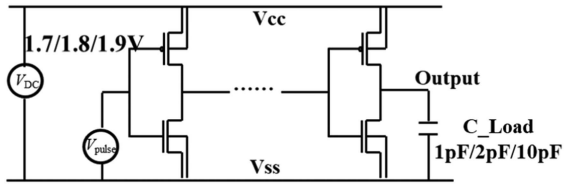


Fig. 1. Eight-stage inverter chain simulation setup with dc power noise.

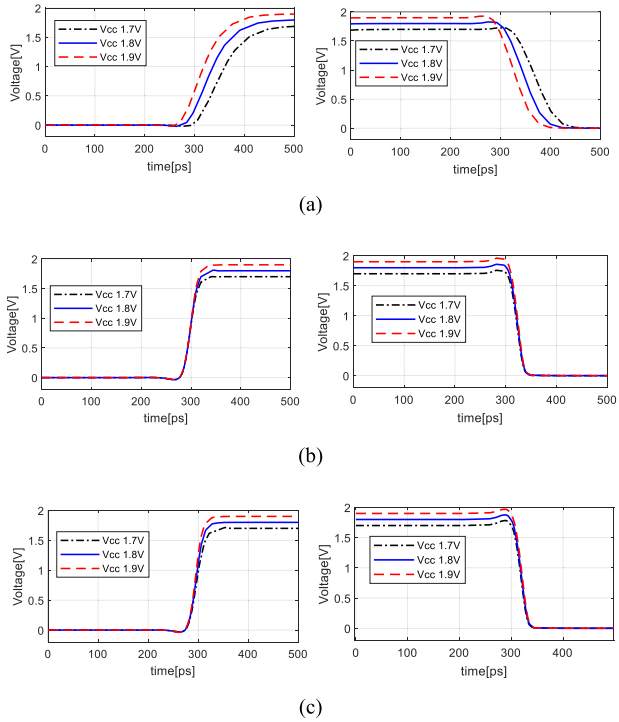


Fig. 2. Inverter chain output rising and falling edge waveform with 2 pF load. (a) From the SPICE simulation. (b) From the non-power-aware IBIS simulation. (c) From the power-aware IBIS simulation.

B. IBIS Model Including the Power-Rail-Voltage Time-Averaged Effect

There is an IBIS model proposed in [13] that includes the power-rail-voltage time-averaged effect to address the issue that the traditional IBIS model cannot simulate the PSIJ correctly.

The IBIS output model structure is shown in Fig. 3. For the model implementation in the IBIS simulation, the buffer transition behavior is mainly described by the pull-up and pull-down switching coefficients, K_{pu} and K_{pd}, as shown in Fig. 3. The algorithm improves the PSIJ simulation accuracy by modifying the switching coefficients as a function of time and the averaged power-rail voltage, as given in (1) and (2)

$$K_{pu}(t) = K_{pu0}(t) + B_{pu}(t)\left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]$$

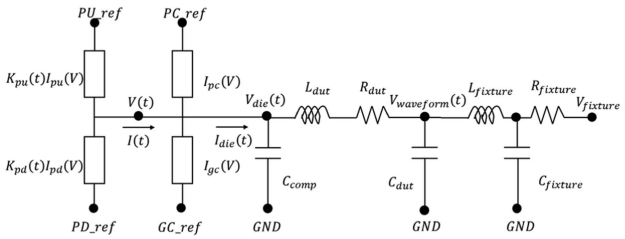


Fig. 3. IBIS output model structure.

$$+ A_{pu}(t)\left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]^2 \quad (1)$$

$$K_{pd}(t) = K_{pd0}(t) + B_{pd}(t)\left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right] + A_{pd}(t)\left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]^2 \quad (2)$$

where

K_{pu0} and K_{pd0} K_{pu} and K_{pd} coefficients for typical power-supply voltage V_{cc0} case;

$B(t)$ and $A(t)$ linear and quadratic fitting coefficients, respectively, that account for the delay change due to the power-rail noise voltage;

$\frac{\int_0^t V_{cc}(\tau)d\tau}{t}$ averaged power-supply voltage since the last input switching event.

The six unknown coefficients $K_{pu0}(t)$, $K_{pd0}(t)$, $B_{pu}(t)$, $B_{pd}(t)$, $A_{pu}(t)$, and $A_{pd}(t)$ can be extracted following the process below.

1) The K_{pu} and K_{pd} coefficients for typical-case $K_{pu0}$and K_{pd0} can be solved using the two equations and two unknowns' algorithms under two different driver output voltage conditions with the *I–V* data for a typical case as (3) and (4)

$$K_{pu}(t)I_{pu}(V_1) + K_{pd}(t)I_{pd}(V_1) + I_{pc}(V_1) + I_{gc}(V_1) = I_{\text{out}}(V_1) \quad (3)$$

$$K_{pu}(t)I_{pu}(V_2) + K_{pd}(t)I_{pd}(V_2) + I_{pc}(V_2) + I_{gc}(V_2) = I_{\text{out}}(V_2) \quad (4)$$

where

$I_{pu}(V)$ and $I_{pd}(V)$ pull-up and pull-down *I–V* tables from the IBIS model;

$I_{pc}(V)$ and $I_{gc}(V)$ power-clamp and ground-clamp *I–V* tables from the IBIS model;

$I_{\text{out}}(V)$ driver output *I–V* relationship.

2) For the $B_{pu}(t)$, $B_{pd}(t)$, $A_{pu}(t)$, and $A_{pd}(t)$ extractions, the two equations and two unknowns' algorithms in (5) and (6) can be used

$$K_{pu/pd\_\max}(t) = K_{pu/pd0}(t) + B_{pu/pd}(t) \times [V_{cc\_\max} - V_{cc0}] + A_{pu/pd}(t)[V_{cc\_\max} - V_{cc0}]^2 \quad (5)$$

$$K_{pu/pd\_\min}(t) = K_{pu/pd0}(t) + B_{pu/pd}(t)\,[V_{cc\_\min} - V_{cc0}] + A_{pu/pd}(t)[V_{cc\_\min} - V_{cc0}]^2 \quad (6)$$

where the $K_{pu/pd\_\max}$ and $K_{pu/pd\_\min}$ should be the K_{pu} and K_{pd} coefficients under maximum and minimum power-supply voltage in the $V_{cc\_\max}$ and $V_{cc\_\min}$ case.

However, according to Sun and Hwang [13], for the above algorithm, in (5) and (6), the $K_{pu/pd\_\max}$ and $K_{pu/pd\_\min}$ are obtained from (3) and (4) when the pull-up and pull-down *I–V* data are actually from the max and min corner. In this way, $B(t)$ and *A(t)* are not only related to the power-rail voltage itself but also to the process corner, which cannot give a model that can count for the propagation delay change caused only by the supply-voltage change. Using the PSIJ sensitivity is needed to obtain K_{pu} and K_{pd} for the cases with nonnominal supply voltage because PSIJ is only caused by the power-rail supply-voltage fluctuation.

C. Improved IBIS Model With K_{pu}/K_{pd} Modification Algorithm Based on the DC PSIJ Sensitivity

To ensure that the functions are purely related to the power-supply-voltage fluctuation and to avoid any effects from the process corners, the dc-jitter sensitivity is introduced to this process to capture the supply-voltage effect on the propagation delay for maximum- and minimum-supply-voltage cases. Moreover, this method can obtain the $B(t)$ and $A(t)$ coefficients by introducing a single parameter and dc-jitter sensitivity, while for the previous algorithm, the extraction of $B(t)$ and $A(t)$ coefficients required two additional sets of the driver output *I–V* relationships with the maximum and minimum supply voltage. Thus, the previously existing problem is resolved, and the algorithm implementation process is simplified.

The impact of the jitter can be represented by the product of the jitter sensitivity and the supply-voltage noise. In [10], it provided a jitter-sensitivity model based on the dc-jitter sensitivity, the PSRR response, and the frequency dependency due to the time-averaged effect, as given in (7). The time-averaged effect is already considered by taking the averages of the V_{cc} in (1) and (2). Furthermore, it proves in [10] that the PSRR response is less important for the inverter/inverter chain and more important for the differential driver. For the former cases, the PSRR term can be neglected. The dc-jitter sensitivity is the last term to be taken into account in the jitter-sensitivity model. The dc-jitter-sensitivity calculation based on the PSRR is given in (7), and it represents the output transition edge time difference per unit dc voltage change

$$\text{JitterSensitivity}(\omega) = \frac{T_{pd\_\max} - T_{pd\_\min}}{V_{cc\_\max} - V_{cc\_\min}}\text{PSRR}'(\omega)e^{j\pi f T_{p0}} \times \sin c(\pi f T_{p0}) \quad (7)$$

where

$\frac{T_{pd_{\max}} - T_{pd_{\min}}}{V_{cc_{\max}} - V_{cc_{\min}}}$ dc-jitter sensitivity;

$\text{PSRR}'(\omega)$ power-supply rejection ratio response;

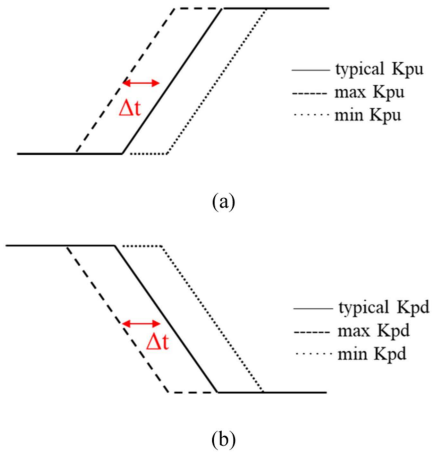


Fig. 4. (a) K_{pu} for typical, maximum, and minimum supply voltage after modification. (b) K_{pd} for typical, maximum, and minimum supply voltage after modification.

$e^{j\pi fT_{p0}}\text{sinc}(\pi fT_{p0})$ frequency dependency due to the time-averaged effect.

For the dc-jitter-sensitivity-based K_{pu} and K_{pd} modification for max- and min-supply-voltage cases, the formula is quite straightforward, as shown in (8) and (9). The output transition edge time difference between the case, where there is noise on the power rail, and the typical case should be added or subtracted

$$K_{pu\_\max/\min}(t) = K_{pu0}(t + \text{DC\_Jitter\_Sensitivity}_{\max/\min} \times \Delta V_{cc}) \quad (8)$$

$$K_{pd\_\max/\min}(t) = K_{pd0}(t + \text{DC\_Jitter\_Sensitivity}_{\max/\min} \times \Delta V_{cc}). \quad (9)$$

As the modified K_{pu} and K_{pd} will substitute the original K_{pu} and K_{pd} in the IBIS model, in the modification processes (8) and (9), the PSIJ effect from the original IBIS model should be excluded. With the PSIJ-sensitivity term, another improvement is that not only the driver itself after modification can be simulated but also the PSIJ effect from the predrivers can be considered. The typical and modified maximum and minimal K_{pu} curves are shown in Fig. 4. The updated driver PSIJ sensitivity for the max or min case is the real driver output PSIJ sensitivity with the PSIJ sensitivity from the original IBIS model subtracted and including the predriver PSIJ sensitivity (if it exists), as shown in (10). The time difference between the K_{pu} and K_{pd} in the typical-voltage and maximum- or minimum-voltage cases is the modified dc PSIJ sensitivity multiplied by the dc supply-voltage difference, as shown in (11)

$$\begin{aligned}&\text{DC\_Jitter\_Sensitivity}_{\max/\min}\\ &= \text{DC\_Jitter\_Sensitivity}_{\max/\min\_\text{output}}\\ &\quad - \text{DC\_Jitter\_Sensitivity}_{\max/\min\_\text{originalIBIS}}\\ &\quad + \text{DC\_Jitter\_Sensitivity}_{\max/\min\_\text{pre}}\end{aligned} \quad (10)$$

where

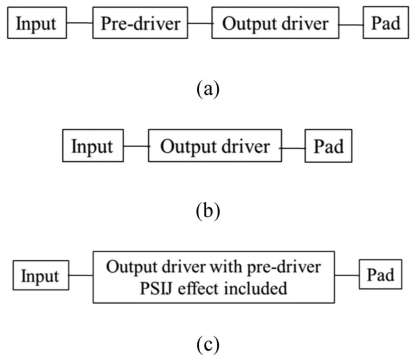


Fig. 5. Schematic of (a) SPICE transistor-level simulation, (b) IBIS behavior model simulation without the predriver, and (c) proposed model simulation, including the predriver.

$\text{DC\_Jitter\_Sensitivity}_{\max/\min\_\text{output}}$ actual simulated or measured dc-jitter-sensitivity value for the driver;

$\text{DC\_Jitter\_Sensitivity}_{\max/\min\_\text{originalIBIS}}$ dc-jitter-sensitivity value from the original IBIS simulation;

$\text{DC\_Jitter\_Sensitivity}_{\max/\min\_\text{pre}}$ predriver dc-jitter sensitivity

$$\Delta t = \text{DC\_Jitter\_Sensitivity}_{\max/\min} \times (V_{cc\_\max/\min} - V_{cc\_\text{typ}}). \quad (11)$$

For the differential driver case, additional terms for the PSRR response should also be introduced to (8) and (9) along with the dc-jitter-sensitivity term for the K_{pu} and K_{pd} modification, and the detailed expression can be found in [10]. The differential output PSRR responses and slopes of the output waveform should be provided, which are required in calculating the PSIJ sensitivity. Other than the discussion above, the jitter-sensitivity-based modification process should be the same as the single-ended case.

The schematic of the improved model regarding the predriver effect compared with the IBIS model is illustrated in Fig. 5. In the SPICE transistor-level simulation, both the predriver and the output buffer can be defined in circuit or element format. However, the conventional IBIS model can only simulate the final driver itself. If the predrivers need to be included in the simulation, either building the circuit for the predrivers and using *B* elements for the IBIS model in SPICE or building another IBIS model for the predrivers is necessary. For the improved model, the PSIJ-sensitivity effect can be included in the K_{pu}/K_{pd} modification process without specific details of the predriver circuit, then the predrivers and final driver can be simulated together.

By applying the jitter-sensitivity-based modification, the K_{pu} and K_{pd} coefficients for maximum- and minimum-supply-voltage cases can be obtained, and the $B(t)$ and $A(t)$ coefficients can be solved accordingly. After the modification, the improved model can be simulated.

III. Simulation Validation

In this section, the proposed K_{pu} and K_{pd} modification algorithm is validated using two models. One is a self-built

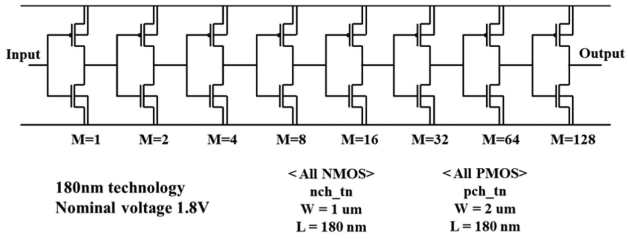


Fig. 6. Design parameters for the eight-stage inverter chain.

eight-stage inverter chain model with different load conditions. The other is a practical DDRx DQ transmitter buffer model with different load terminal voltages.

A. Eight-Stage Inverter Chain

The eight-stage inverter chain SPICE circuit netlist was first built and then simulated and converted to an IBIS model version 3.2 (non-power-aware) and version 5.1 (power-aware) as an output driver. The proposed algorithm was applied to the non-power-aware IBIS model to give the improved IBIS model. PSIJ-sensitivity simulation of the output rising and falling edges was performed for the above four models.

The design parameters for the eight-stage inverter chain are shown in Fig. 6. Input, output, power, and ground pins were defined both in the SPICE circuit model and the IBIS model. The pull-up branch and the pull-down branch in the IBIS model were connected to the power pin and the ground pin, respectively. There was no power clamp branch or ground clamp branch in the model. The IBIS model buffer capacitance, *C*_comp, was extracted using the method provided in [15] and is 0.468 pF for this specific case. The typical, minimum, and maximum supply power voltages were 1.8 V, 1.7 V, and 1.9 V, respectively. The model in the typical (Typ) corner was used to do the validation.

The K_{pu} and K_{pd} switching coefficients for the output rising edge and the falling edge at the typical power-supply voltage of 1.8 V were extracted based on (3) and (4), and are shown in Fig. 7. The dc-jitter sensitivities for the three different load conditions were simulated using SPICE. Implementing (8) and (9), the K_{pu} and K_{pd} switching coefficients at the minimum and maximum power-supply-voltage conditions were obtained and are shown in Fig. 7. The pull-up and pull-down correction coefficients $B(t)$ and $A(t)$ for output rising and falling transitions were extracted using (5) and (6) and are shown in Fig. 7. Substituting the corresponding parameters in (1) and (2), the K_{pu} and K_{pd} coefficients were updated, and the improved IBIS model was obtained.

The simulation setup for the first validation is shown in Fig. 1. The output pin of the inverter chain would be connected to the 1 pF, 2 pF, and 10 pF capacitors, respectively, to show the generalization of the proposed algorithm. The models were first tested when the nominal voltage (1.8 V) was affected by the dc power noise ($\pm$ 0.1 V amplitude), which means the power-rail voltages were 1.8 V, 1.7 V, and 1.9 V. The driver output rising edge and falling edge PSIJ-sensitivity comparison

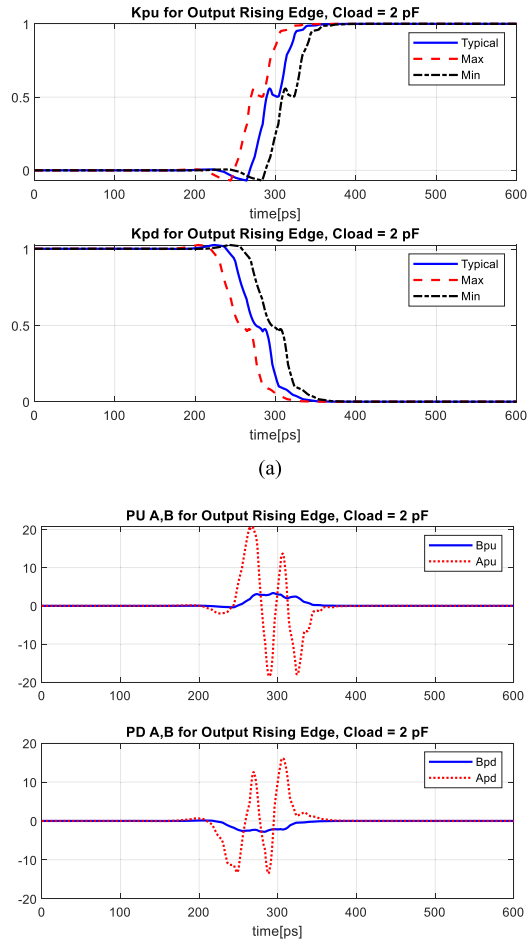


Fig. 7. (a) Output rising edge K_{pu} and K_{pd} extracted for the 2 pF load condition. (b) Output rising edge pull-up and pull-down *B* and *A* extracted for the 2 pF load condition.

TABLE I
EIGHT-STAGE INVERTER CHAIN OUTPUT RISING EDGE PSIJ-SENSITIVITY COMPARISON

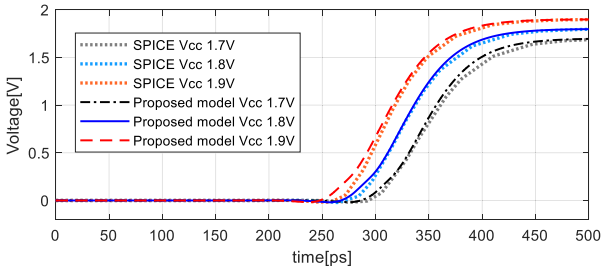
	PSIJ Sensitivity (ps/V)					
	Load 1 pF		Load 2 pF		Load 10 pF	
SPICE	184.45		207		350	
Non-power-aware IBIS	6.5		9.5		39.5	
Power-aware IBIS	35.5		54		217	
Proposed Algorithm	187		210.5		355	
	Difference to SPICE					
	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%
Non-power-aware IBIS	177.95	96.48	197.5	95.41	310.9	88.71
Power-aware IBIS	148.95	80.75	153	73.91	133	38
Proposed Algorithm	2.55	1.38	3.5	1.69	5	1.43

in dc supply-voltage noise is given in Tables I and II. The SPICE circuit simulation results were used as a reference.

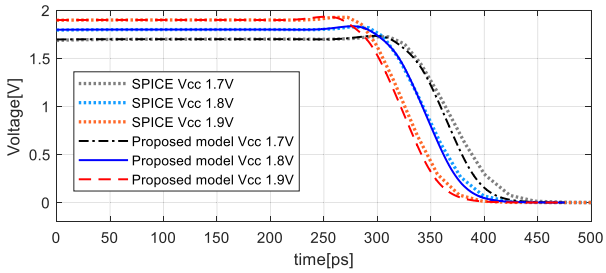
For the driver output rising edge, the non-power-aware IBIS model and the power-aware IBIS model show a PSIJ-sensitivity discrepancy with a SPICE circuit simulation result of up to

TABLE II
EIGHT-STAGE INVERTER CHAIN OUTPUT FALLING EDGE PSIJ-SENSITIVITY COMPARISON

	PSIJ Sensitivity (ps/V)					
	Load 1 pF		Load 2 pF		Load 10 pF	
SPICE	-193.91		-194.16		-188.71	
Non-power-aware IBIS	24.41		36.07		123.21	
Power-aware IBIS	25		35		135	
Proposed Model	-188.95		-186.75		-175.85	
	Difference to SPICE					
	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%
Non-power-aware IBIS	218.32	112.59	230.23	118.58	311.92	165.29
Power-aware IBIS	218.91	112.89	229.16	118.03	323.71	171.53
Proposed Model	4.96	2.56	7.41	3.82	12.86	6.81



(a)



(b)

Fig. 8. Comparison of SPICE simulation and proposed model simulation for output (a) rising edge and (b) falling edge.

96.48%. However, the improved IBIS model using the proposed algorithm reduces the discrepancy to within 2% for the three tested load conditions.

For the driver output falling edge, the non-power-aware IBIS model and the power-aware IBIS model behave even more poorly. The simulated PSIJ sensitivities show the opposite trend to the SPICE results, as seen in Table II and Fig. 2. The IBIS model applying the proposed algorithm corrects the trend and reduces the differences to less than 7%. The detailed output transition behavior for this case is plotted in Fig. 8. Thus, the improved IBIS model using the proposed algorithm works well when there is dc noise in the power rail.

The second simulation was conducted when the nominal voltage (1.8 V) was affected by ac sinusoidal power noise (50 mV amplitude) at different frequencies from 5 MHz to 5 GHz. The modified IBIS models are the same as those in the validation of supply-voltage dc noise conditions. The simulation

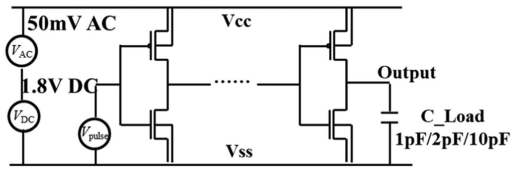


Fig. 9. Eight-stage inverter chain simulation setup with ac power noise.

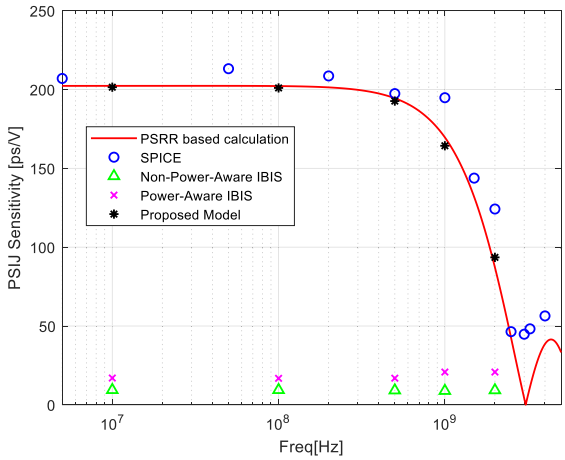


Fig. 10. PSIJ-sensitivity comparison for the inverter chain with ac noise when the load is 2 pF.

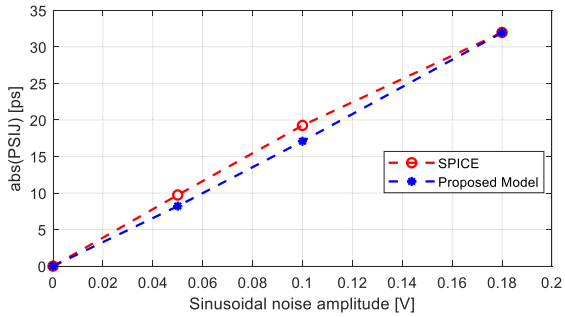


Fig. 11. Inverter chain output rising edge PSIJ comparison with different ac noise amplitudes at 1 GHz when the load is 2 pF.

setup is detailed in Fig. 9. A result comparison for the condition with the 2-pF load is plotted in Fig. 10. The PSIJ sensitivities simulated from the non-power-aware IBIS model and the power-aware IBIS model are flat in the tested frequency band and show no frequency-dependent characteristics. The SPICE circuit simulation and the improved IBIS model simulation show good correlation when the power noise frequency changes. The frequency-dependent PSIJ sensitivity was also calculated using the method based on the PSRR given in (7), and the good match further validates the accuracy of the proposed algorithm.

The ac noise amplitude variation range of sinusoidal power-supply noise for which the proposed technology can work properly was also investigated and presented in Fig. 11. The frequency of the noise is 1 GHz. The inverter chain output rising edge PSIJ was observed when the ac signal amplitude varied

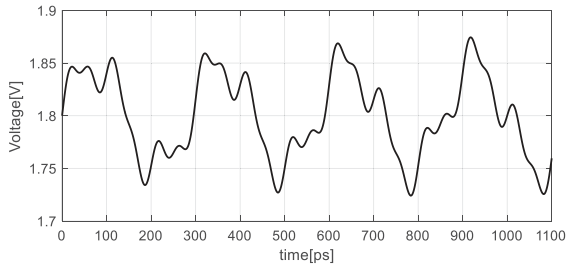


Fig. 12. Power-supply voltage with noise signal with three frequency components.

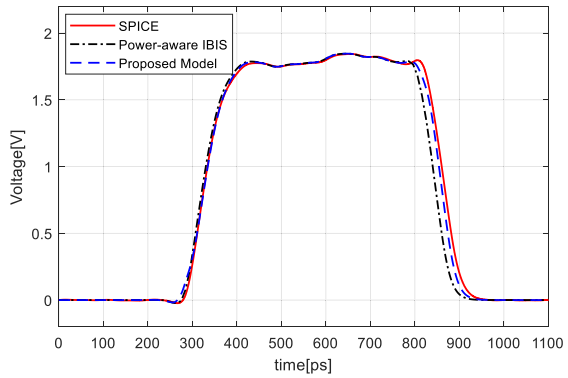


Fig. 13. Inverter chain output waveform comparison with noise signal with three frequency components when the load is 2 pF.

from 0% to 10% of the dc supply voltage. The discrepancy between the SPICE simulation and the proposed model simulation is within 15%.

Further validation was conducted to test the reliability of the proposed model when the noise was in another format. In general, the power-supply noise in the linear system can be regarded as a superposition of the sinusoidal signals of different frequencies. Consider a noise signal that is composed of three sinusoidal signals whose amplitude is 50 mV, 20 mV, and 10 mV, separately, and frequency is 3.5 GHz, 10 GHz, and 20 GHz, separately, was in the 1.8 V power rail of the inverter chain circuit. The supply voltage is shown in Fig. 12. Under this condition, the driver output behavior was compared in Fig. 13 for the SPICE simulation and the proposed model simulation.

The proposed algorithm enables the IBIS model to accurately capture the ac noise on the power rail and react correctly as investigated above.

B. DDRx DQ Tx Buffer With Predriver

The schematic of the practical DDRx DQ buffer circuit is given in Fig. 14 and the problem of the IBIS simulation for this model is stated in [16]. Two control signals control the pull-up and pull-down branches. Two predriver stages are in two different power domains, VDD and VDDQ, and they are not included in the IBIS model. The DDRx DQ IBIS model is shown in the figure as the final driver and is in the same VDDQ power domain as the second predriver stage. The typical, minimum, and maximum supply power voltages are 1.1 V, 1.045 V, and 1.155

TABLE III
DDRx DQ Tx Buffer With Predriver Output Rising Edge PSIJ-Sensitivity Comparison

	PSIJ Sensitivity (ps/V)					
	Load 50 Ohm to VSS		Load 50 Ohm to VDDQ		Load 50 Ohm to V_{typ} 1.1V	
SPICE	156.65		134.17		95.45	
Non-Power-aware IBIS	15.45		38.18		6.36	
Power-aware IBIS	60		45.45		14.55	
Proposed Model	159.09		147.27		107.27	
	Difference to SPICE					
	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%
Non-Power-aware IBIS	141.2	90.14	95.99	71.54	89.09	93.34
Power-aware IBIS	96.65	61.70	88.72	66.13	80.9	84.76
Proposed Model	2.44	1.56	13.1	8.9	11.82	12.38

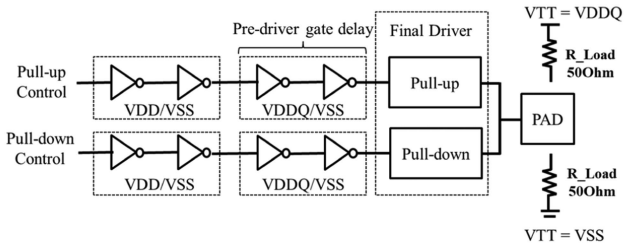


Fig. 14. DDRx DQ buffer schematic.

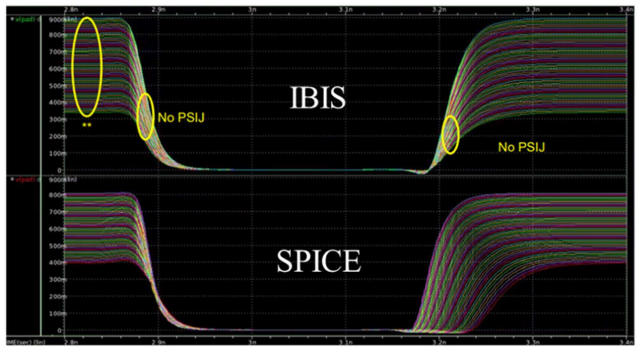


Fig. 15. Simulated DDRx DQ output waveform comparison for a 50-Ω load connected to the VSS where the VDDQ was swept from 0.85 to 1.35 V.

V, respectively. The model in the typical (Typ) corner was used for the validation. The output pad was connected to a 50-Ω load with three different terminal voltages for validation purposes. The terminal voltage was set for the first case as VSS (0 V). For the second case, the terminal voltage was the same as the power-supply-voltage VDDQ, irrespective of power-rail noise. For the third case, the terminal voltage was the typical voltage ($V_{\rm typ}$) of 1.1 V. In this test, the power-rail noise was ± 0.055 V dc noise, which means that the VDDQs were 1.1 V, 1.045 V, and 1.155 V.

For the first case, when the 50-Ω load was connected to the VSS and the VDDQ was swept from 0.85 to 1.35 V, the SPICE circuit simulation and IBIS simulation outputs are given in Fig. 15. In the IBIS simulation, the predriver and final driver

PSIJ effects are not included. The PSIJ was not characterized correctly.

The simulation results for all the test cases for the DDRx DQ Tx buffer output rising edge are given in Table III. The output PSIJ sensitivities of the traditional non-power-aware and power-aware IBIS models are more than 60% different from the SPICE circuit simulation results. The difference is reduced to less than 13% after applying the proposed algorithm. The IBIS model improved using the proposed algorithm works well for this practical model when there is dc noise in the power rail.

IV. Conclusion

An IBIS model with a modified switching coefficients algorithm is proposed to improve its PSIJ simulation accuracy. The improvement is achieved by including the driver dc PSIJ effect in the IBIS model switching coefficients. The straightforward and effective introduction of the dc-jitter-sensitivity parameter is key to ensuring that the improved model output PSIJ behavior is not affected by the process corner.

The accuracy of the proposed algorithm was validated using an inverter chain model and a practical DDRx DQ model. After the modification, the IBIS simulation output transition behaviors match well with the SPICE transistor-level circuit simulation. The results show that for both dc and ac noise in the power rail, the improved model behaves accurately. The predriver PSIJ effect can also be simulated together with the final driver IBIS model without knowing the circuit details.

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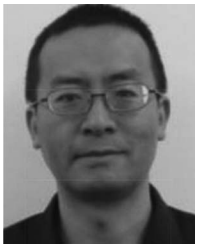

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