

Implementation of Silicon Carbide Four-Switch Three-Phase Inverters

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Abstract—The paper presents a silicon carbide (SiC) four-switch three-phase (FSTP) inverter as a low-cost, compact, and highly efficient alternative to traditional six-switch three-phase (SSTP) inverters. The integration of SiC semiconductor technology with a four-switch three-phase topology can effectively reduce the cost and size of SiC inverters due to the low part counts in the topology while leveraging the advantages of SiC devices. A SiC FSTP inverter prototype has been developed and tested in this study. A unique control methodology for the inverter is proposed and employed. It is not only straightforward to implement but also highly effective in addressing the imbalance issue inherent in the FSTP topology. Simulation models based on MATLAB Simscape, are also utilized to validate the inverter's performance and predict its efficiency. The SiC FSTP inverter, as well as a Si FSTP and an SSTP inverter with comparable designs, have been tested with the same inductive load. Both simulation and experimental results consistently indicate that the SiC FSTP inverter outperforms its counterparts, proving to be the most efficient and cost-effective option under the testing conditions studied in this paper.

Keywords—SiC, four-switch three-phase, inverter, SVPWM, imbalance compensation, efficiency, simulation

I. INTRODUCTION

Silicon carbide (SiC) semiconductor technology has been available for over two decades since the commercialization of the first SiC Schottky diode in 2001. Widely recognized as an alternative to traditional silicon (Si) semiconductor technology, SiC semiconductor technology offers several advantages, including high efficiency, high frequency, high power density, and the capability for high-temperature operation, etc. With rapid growth over the past decade, the global SiC power device market has expanded significantly and reached \$1.3 billion in size in 2022 [1]. The projections from multiple market reports [2-5] anticipate a further surge, estimating the market value to be \$7 - 10 billion by 2030. This would represent more than 10% of the total power electronics market at that time. The adoption of SiC in electric vehicles (EVs) is the key driver of this significant increase. Tesla, for instance, has incorporated SiC inverters in the Model 3 since 2018, setting a trend subsequently followed by several other automakers including Porsche, Audi, Hyundai, and others [6]. According to Wolfspeed, a SiC industry pioneer, the automotive SiC market attained a value of approximately \$1.055 billion in 2020. Notably, 90% of this market value was allocated to inverters, with the remaining 10% distributed between onboard chargers and DC-DC converters [7]. The projections in [3] suggest that the automotive SiC market is expected to reach \$3.3 billion by 2025 and \$7.5 billion

by 2030. Beyond EV applications, SiC devices have found commercial applications in various sectors, including wind and solar power factor correction, lighting, railway traction, motor drives, and uninterrupted power supply (UPS), etc. Despite the fast growth of the SiC market in recent years, the high cost of these devices remains a significant obstacle to achieving further market penetration, alongside technical challenges as discussed in [8-10]. As seen in Fig.1 and 2, the retail price of 1200 V SiC MOSFETs remains considerably higher than that of Si IGBTs. On average, the cost for discrete SiC devices is approximately 4.7 times higher, and for modules, it is around 6.9 times higher than their Si counterparts. This substantial price difference can be primarily attributed to the high cost of SiC substrates, requiring a high-temperature fabrication process exceeding 2000 °C [11]. As demonstrated in [12-13], the cost of switching devices dominates the overall cost of an inverter. Although the potential savings in cooling, filters, and efficiency improvements can outweigh the high cost sometimes, the impact of high device costs remains substantial. Consequently, addressing the high cost is imperative from every perspective.

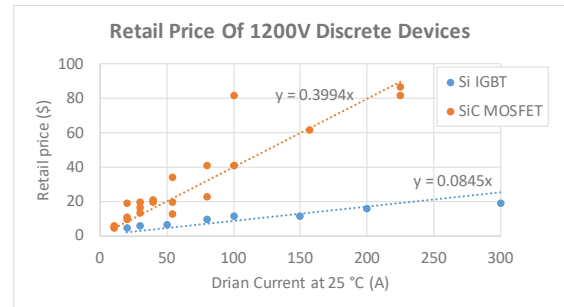


Fig. 1. The retail price of 1200V discrete devices

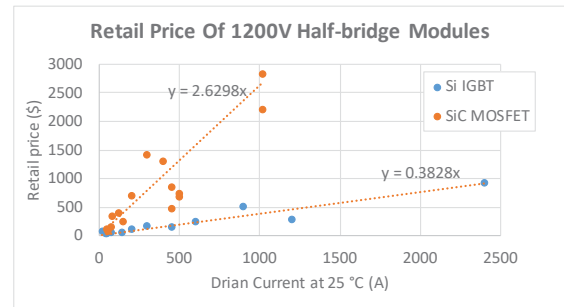


Fig. 2. The retail price of 1200V half-bridge Modules

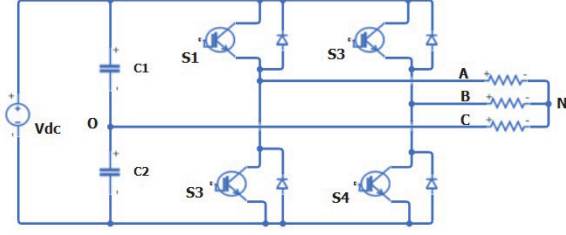


Fig. 3. The topology of FSTP inverters

As a potential solution, this paper proposes a four-switch three-phase topology for SiC inverters to reduce the overall inverter cost. In contrast to conventional SSTP inverters consisting of three phase-legs, FSTP inverters, as illustrated in Fig. 3, have only two phase-legs, inherently resulting in a reduction of both cost and size by one-third. Note that these inverters have a relatively low output-to-input voltage ratio. But this is not always a disadvantage. Some applications may benefit from this. For example, it can facilitate the adoption of a high DC architecture in electric vehicles when used as a traction inverter [14], which helps to reduce the charging time.

The primary challenges associated with these inverters pertain to their control strategy and performance. Subsequent sections will delve into a novel control and compensation method for SiC FSTP inverters and examine their performance thoroughly through simulations and experiments, drawing comparisons with the silicon counterparts.

II. CONTROL AND COMPENSATION

Unlike traditional SSTP inverters, which utilize six controllable devices, FSTP inverters rely on the switching of four semiconductor devices (S1-S4) to generate a three-phase balanced voltage. Therefore, the control strategy of FSTP inverters is relatively complex. This paper presents a unique Space Vector Pulse Width Modulation (SVPWM) control method, which greatly reduces the complexity of the traditional SVPWM methods presented in [15-16]. The simplified method not only eliminates the constraint of modulation sections in SVPWM but also represents the control algorithm using unified explicit equations that are valid for the entire fundamental period. Moreover, the method also effectively integrates compensation for the imbalance issue in FSTP inverters arising from the voltage ripple at the center tap of the DC link (Point O in Fig. 3). This method differs from other approaches, such as those outlined in [17], in that it does not require any additional components in the primary power path. Further details are provided in the following sections.

A. The simplified SVPWM Control

The goal of SVPWM control is to generate a three-phase balanced voltage as represented by (1) in the time domain or by (2) in the vector domain, where S_1 and S_3 are the state variables of the high-side switches and their values are "1" for "ON state" and "0" for "OFF state," respectively.

$$\begin{aligned} V_{AN} &= (4S_1 - 2S_3 - 1) \frac{V_{dc}}{6} \\ V_{BN} &= (4S_3 - 2S_1 - 1) \frac{V_{dc}}{6} \\ V_{CN} &= (1 - S_1 - S_3) \frac{V_{dc}}{3} \end{aligned} \quad (1)$$

$$\mathbf{V}_{ref} = V_\alpha + jV_\beta, \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}} \left(S_1 - \frac{1}{2}S_3 - \frac{1}{4} \right) \\ \sqrt{\frac{1}{2}} \left(S_3 - \frac{1}{2} \right) \end{bmatrix} V_{dc} \quad (2)$$

According to the four combinations of the two state variables, four distinct space vectors ($\mathbf{V}_0 - \mathbf{V}_3$) are produced as shown in Fig. 4. A zero vector can be obtained by summing $\mathbf{V}_0$ and $\mathbf{V}_3$, or $\mathbf{V}_1$ and $\mathbf{V}_2$. The four space vectors divide the vector domain into four sections (① - ④). Within each section, the two adjacent space vectors along with a zero vector are modulated to make their time-weighted average equal to a reference vector, denoted as $\mathbf{V}_{ref}$ in Fig. 4, which represents the desired output voltage. By arranging the switching sequence according to Fig. 5, unified equations for the switch duty ratios can be derived as expressed in (3), which are applicable across all four sections. For more details, please refer to [18].

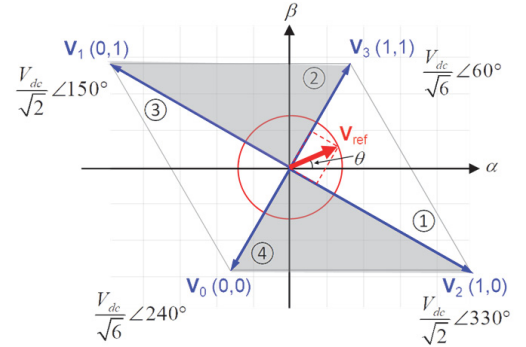


Fig. 4. Space vector diagram for SVPWM FSTP inverters

Section ① and ④					
	$\mathbf{V}_0$	$\mathbf{V}_2$	$\mathbf{V}_3$	$\mathbf{V}_3$	$\mathbf{V}_2$
S_1		1	1	1	1
S_3		0	1	1	0

Section ② and ③					
	$\mathbf{V}_0$	$\mathbf{V}_1$	$\mathbf{V}_3$	$\mathbf{V}_3$	$\mathbf{V}_1$
S_1		1	1	1	1
S_3		1	1	1	0

Fig. 5. SVPWM switching sequence

$$D_{s_1} = \frac{1}{2} [1 + m \sin(\theta + 60^\circ)],$$

$$D_{s_3} = \frac{1}{2} (1 + m \sin \theta),$$

m – amplitude modulation ratio.

B. Imbalance compensation

One major problem with FSTP inverters is the occurrence of unbalanced three-phase output caused by the uneven distribution of the input voltage across the two input capacitors, C_1 and C_2 in Fig. 3. The charging and discharging of these capacitors inevitably cause voltage fluctuations at the center tap of the DC link. This, in turn, leads to unbalanced phase voltages at the output. Through space vector analysis, it is discovered that the voltage ripple at the center tap introduces a shift to the vector trajectory of the output voltage under imbalanced situations. As seen in Fig. 4, in balanced scenarios, the vector trajectory of the output voltage, $\mathbf{V}_{\text{ref}}$, forms a circular path (shown in red) with its center at the origin of the coordinate system. In contrast, under unbalanced situations, as illustrated in Fig. 6, the vector trajectory (shown in blue) deviates from the origin by $\Delta\mathbf{V}$ while remaining circular, where $\Delta\mathbf{V} = \sqrt{2/3}\Delta V \angle 60^\circ$ with the assumption that the voltage of C_1 is $V_{dc}/2 + \Delta V$. Thus, adding $-\Delta\mathbf{V}$ to the desired $\mathbf{V}_{\text{ref}}$ during modulation can realign the vector trajectory back to the origin. This adjustment replicates the balanced situation, ensuring a balanced output voltage. To implement this method, the switch duty ratios are calculated using the real-time value of ΔV . Two correction factors, A_m and B_θ , are introduced to adjust the original values derived from (3). These factors can be calculated by (4). During the compensation, m and θ in (3) should be replaced by $A_m m$ and B_θ , respectively.

$$A_m = \sqrt{1 + \frac{16\Delta V^2}{3m^2 V_{dc}^2} - \frac{8\Delta V}{\sqrt{3}m V_{dc}} \sin(\theta + 30^\circ)}$$

$$B_\theta = \tan^{-1} \left(\frac{\sin \theta - 2\Delta V/m V_{dc}}{\cos \theta - 2\Delta V/\sqrt{3}m V_{dc}} \right)$$

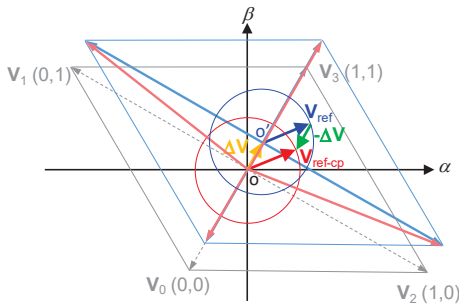


Fig. 6. Space vector diagram when the voltage ripple at the center tap is ΔV .

III. INVERTER SPECIFICATIONS

To further validate the proposed method, both simulations and experiments have been conducted for a SiC FSTP inverter and a Si FSTP inverter with similar designs while driving an

TABLE I. INVERTER SPECIFICATIONS

COMPONENTS	PARAMETERS	
	SiC inverter	Si inverter
Switches	1200V 36A MOSFET	600V 30A IGBT
Diodes	1200V 33A Schottky	600V 30A FRD
Gate Drivers	$V_{gs} = -5V/20V$ $T_{dead} = 520\text{ns}$	$V_{gs} = 0V/15V$ $T_{dead} = 700\text{ns}$
Snubber Circuits	$R = 10 \Omega$ $C = 220 \text{pF}$	$R = 10 \Omega$ $C = 220 \text{pF}$
Input capacitors	250V/470 μF 2 in series	450V/470 μF 2 in parallel
Load	3-phase inductive load $R = 10.4 \Omega, L = 10\text{mH}$	

identical load. The specifications of the main components in these inverters are listed in Table I. The control circuit is developed using a TMS320F28335 microprocessor capable of executing the proposed SVPWM control with or without compensation. The simulation results and experimental results are presented and discussed in the next two sections, respectively.

IV. SIMULATIONS

Simulation models have been developed for the FSTP SiC inverter using the power component models from the electrical library of MATLAB Simscape as shown in Fig 7. This model can capture the influence of crucial design elements on inverter performance, encompassing aspects such as control strategy, device characteristics, switching frequency, driver design, snubber circuits, etc.

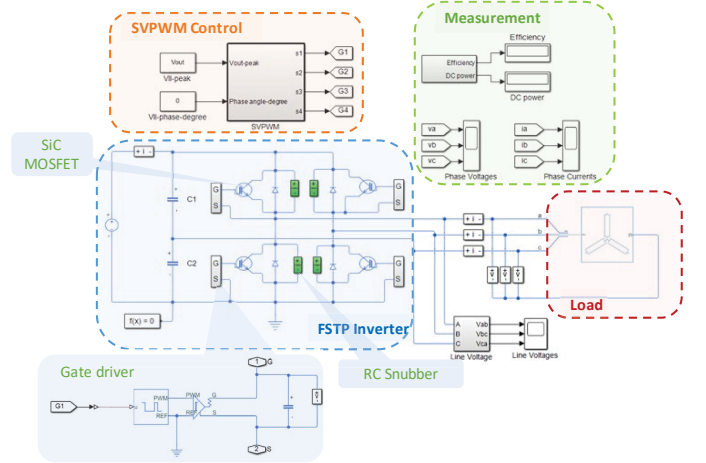


Fig. 7. Simulation models for the FSTP inverter

Fig. 8 demonstrates the simulation results of the trajectory of the output voltage. Due to the unbalanced output voltage, the trajectory of the output voltage in Fig. 8 (a) is not circular. After implementing the proposed compensation, the trajectory became a circle as seen in Fig. 8 (b), which represents a balanced three-phase output voltage. The waveforms of the inverter output phase voltages and currents are also shown in Fig. 9. Corresponding to Fig. 8, the imbalance of the output currents in Fig. 9 (c) is mitigated as a result of the compensation.

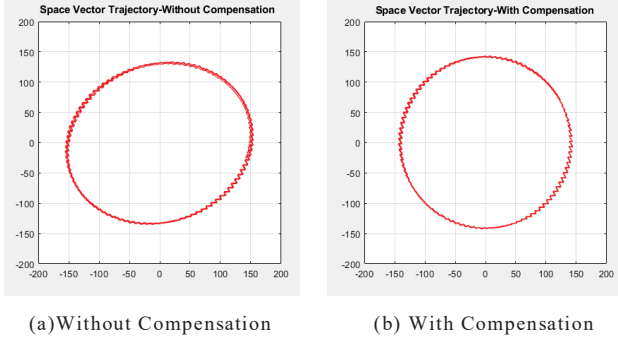
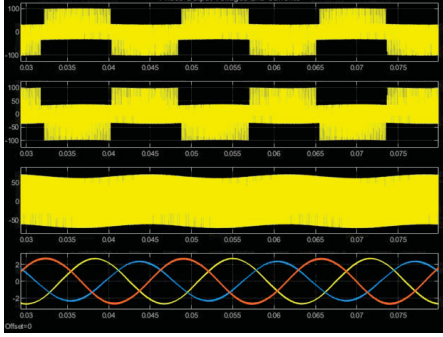
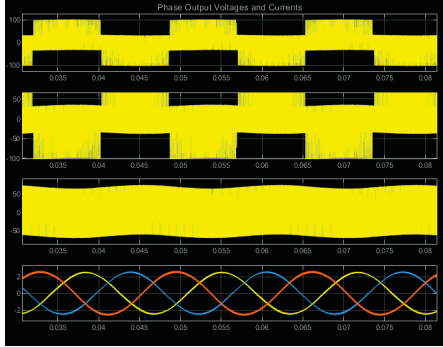


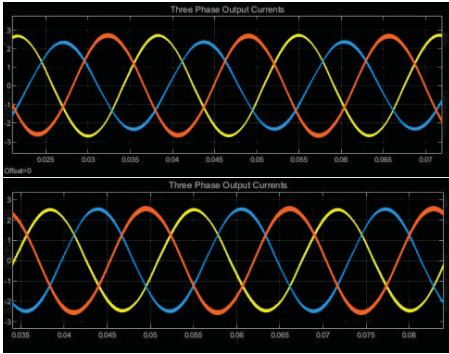
Fig. 8. Trajectory of the inverter output voltage



(a) The inverter output voltages and currents without compensation



(b) The inverter output voltages and currents with compensation



(c) The output currents with compensation (bottom) and without compensation (top).

Fig. 9. The simulation results of the SiC FSTP inverter when $V_{dc}=200\text{V}$, $f_c=10\text{kHz}$, and $m=0.5$

Beyond generating waveforms for voltages and currents, the simulations can also provide quantitative estimations of power consumption and efficiency. For example, the efficiency of the SiC FSTP inverter is estimated to be 98.3% with an input voltage of 200 V and a modulation ratio of 0.5. The parameters used in the simulations are obtained from device testing or manufacture datasheets.

V. EXPERIMENTS

The inverters have been tested with the inductive load specified in Table I. The testing setup is shown in Fig. 10. Waveforms similar to the simulation results in Fig. 9 are also obtained and demonstrated in Fig. 11, illustrating the effectiveness of the proposed control and compensation method. The efficiency of the SiC FSTP inverter is evaluated across

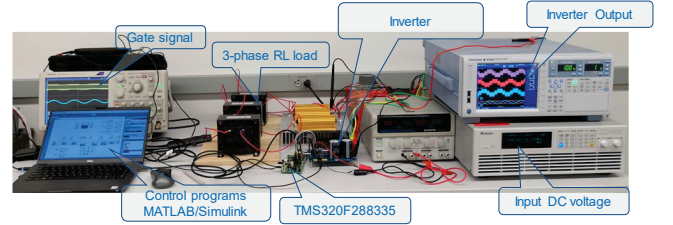
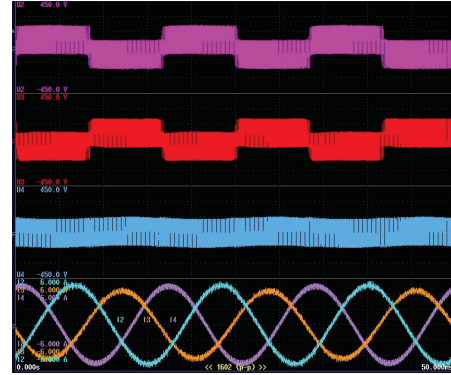
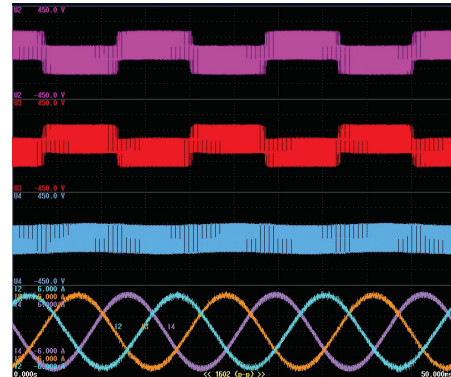


Fig. 10. Testing setup

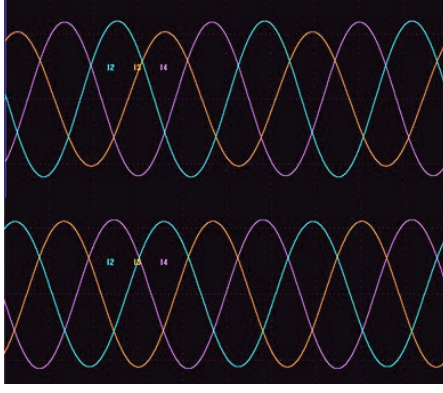


(a) The inverter output voltages and currents without compensation



(b) The inverter output voltage and current with compensation

Fig. 11. The experimental results of the SiC FSTP inverter when $V_{dc}=400\text{V}$, $f_c=10\text{kHz}$, and $m=0.5$



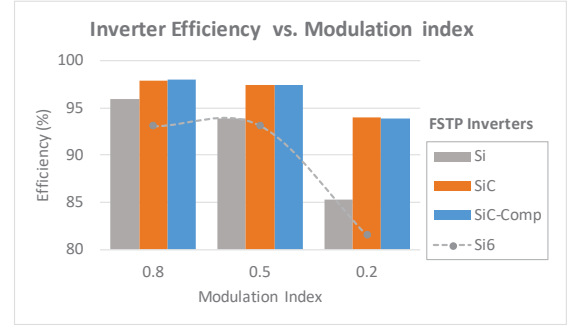
(c) The fundamentals of the output currents with compensation (bottom) and without compensation (top).

Fig. 11. The experimental results of the SiC FSTP inverter when $V_{dc} = 400\text{V}$, $f_s = 10\text{kHz}$, and $m = 0.5$

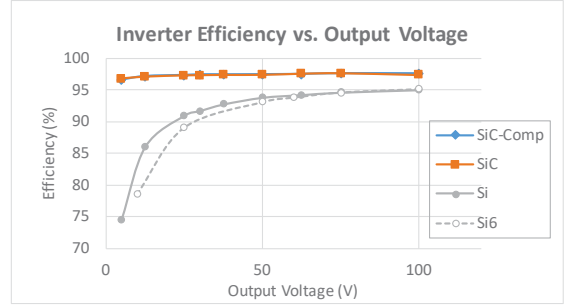
various input voltages, modulation ratios, and switching frequencies. Results are obtained for both the control algorithm with and without compensation, and these are presented in Fig. 12 alongside the efficiency data for the Si FSTP and SSTP inverters. As seen in the figures, the efficiency of the inverters decreases with the reduction in the modulation ratio (Fig. 12 (a)) and the output voltage (Fig. 12 (b)), as well as the increase in the switching frequency (Fig. 12 (c)). The efficiency variation in the Si inverters is significant, particularly at light loads and high frequencies. Its value declines dramatically from 95.1% under normal loads to 74.6% at low loads. In contrast, the efficiency of the SiC FSTP remains relatively stable, hovering around 97.5% throughout most of the testing range, with the highest value at 98.0% and the lowest at 93.9%. Thus, the SiC FSTP is more efficient than its Si counterparts under the same load conditions. The typical efficiency improvement is about 3.8%, corresponding to a loss saving of 60.2%. Furthermore, as evident in Fig. 12, the efficiency of the compensated SiC FSTP inverter closely aligns with that of the uncompensated one. This indicates that the proposed control method does not adversely impact inverter efficiency while effectively addressing the imbalance issue. In addition to the efficiency advantages, the SiC FSTP inverter is not only 30% more cost-effective but also smaller in size compared to the SiC SSTP, and it incurs only a ~12% higher cost than the Si SSTP.

VI. CONCLUSION

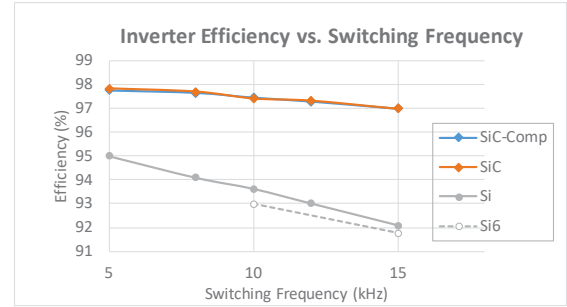
This paper studies silicon carbide four-switch three-phase inverters that integrate the four-switch topology with SiC semiconductor technology. The SiC FSTP inverter leverages the advantages of both technologies, offering cost-effectiveness and compactness attributed to the low part counts in the topology, as well as high efficiency due to the superior properties of SiC devices. The paper delves into the control, simulation, and implementation of the SiC FSTP inverter, presenting a novel SVPWM control method to address common imbalance issues associated with the four-switch topology. A prototype of the SiC FSTP inverter has been simulated and tested with the proposed control methods. The results from both simulation and



(a) The efficiency changing with the modulation ratio when $V_{ll,pk} = 50\text{V}$ and $f_s = 10\text{kHz}$;



(b) The efficiency changing with the output voltage when $f_s = 10\text{kHz}$ and $m = 0.5$



(c) The efficiency changing with the switching frequency when $V_{ll,pk} = 50\text{V}$ and $m = 0.5$.

Fig. 12. The efficiency of the SiC FSTP inverter in comparison to the Si FSTP and SSTP inverters

experiments validate the efficacy of the new control methodology and highlight the advantages of the SiC FSTP inverter over its silicon counterparts. In summary, SiC FSTP converters can be low-cost alternatives to conventional SSTP inverters in some applications, especially when the high input voltage is not an issue.

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