A mm-Wave Concurrent Dual-Band Dual-Beam Phased Array Receiver Front-End in 22-nm CMOS FDSOI

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***Abstract*— This article presents a mm-Wave concurrent dual-band (28 and 39 GHz) dual-beam phased array multiple-input multiple-output (MIMO) receiver (RX) front-end with mid-band rejection in the 22-nm fully depleted silicon-on-insulator (FDSOI) CMOS process. This phased array RX front-end has four inputs and two output streams with fully connected (FC) configuration where it takes advantage of sharing low-noise amplifier (LNA) and quadrature network (QN) and using a unique phase shifter (PS) structure which allows power and area saving. The measured 3-dB gain bandwidth is from 23 to 30 GHz for the lower bandwidth with a peak gain of 21 dB at 29 GHz, and from 36 to 40 GHz for the upper bandwidth with a peak gain of 18 dB at 38.5 GHz, and a noise figure (NF) of a minimum of 6 and 7 dB at 28 and 37 GHz, respectively. The 21-dB mid-band rejection at 33.5 GHz is provided by the LNA to attenuate the out-of-band unwanted interference helping relaxing the linearity requirement. The entire single-channel RX front-end achieves third order intercept point (IIP3) varying from −18 to −11 dBm, and input 1-dB compression point varying from −25 to −18 dBm. The front-end has 5-bit phase control and 7-dB gain control achieving the rms phase and gain errors less than 6° and 1.2 dB, respectively, enabling orthogonality. This array demonstrates the concurrent functionality and carrier aggregation (CA) for over-the-air (OTA) beam-steering and error vector magnitude (EVM) measurements. The chip has a length of 2738 μm, a width of 1808 μm, and an area of 4.95 mm^2 including all dc, radio frequency (RF) pads, and decoupling capacitors.**

***Index Terms*— Beamforming, carrier aggregation (CA), concurrent, dual-band, 5G, front-end, fully connected (FC), fully depleted silicon-on-insulator (FDSOI) CMOS, mm-Wave, multiple-input multiple-output (MIMO), null tuning, phased array, wideband.**

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I. Introduction

THE fifth generation of wireless communication systems is expected to offer faster and more reliable connectivity, support more devices and network capacity [1], and enable new use cases that are currently impossible with the existing technologies, such as autonomous vehicles [2], [3], [4]. One of the key technological advancements in 5G wireless systems is the use of multiantenna approaches [5], which improve the performance of wireless communication by compensating for free path loss, particularly at mm-Wave frequencies. Another advantage of exploiting the multiantenna approach is spatial multiplexing, which allows multiple data streams to be received/transmitted simultaneously at the same or different frequencies [6]. In addition, interference reduction is a critical element in multiantenna systems, where unwanted in-band or out-of-band signals at different angles from the desired signal are filtered out by spatial filtering. Multiple-input multiple-output (MIMO) and beamforming (RF/analog, digital, or hybrid) are both important techniques used in multiantenna systems to achieve aforementioned features [7]. In addition, mm-Wave frequencies offer advantages such as increased channel bandwidth and data rate. For 5G applications, several mm-Wave frequency bands have been defined, including n257 (26.50–29.50 GHz), n258 (24.25–27.5 GHz), n259 (39.5–43.5 GHz), n260 (37–40 GHz), and n261 (27.5–28.35 GHz) [8].

To enable multiband MIMO communication in multiantenna systems, it is essential to develop an mm-Wave concurrent multistream beamforming front-end receiver (RX) that can support multiple frequency bands (23–30 and 36–40 GHz). In this work, a dual-band (28 and 39 GHz) RF-beamforming (RFB) RX front-end supporting two simultaneous output streams with fully connected (FC) configuration is introduced. The work that is presented in this article features major contributions compared with the state-of-the-art works in the literature in both system-level architecture and circuit-level implementation. In terms of system-level architecture, to the authors' knowledge, this article features the first fully integrated mm-Wave concurrent dual-band dual-beam phased array RX front-end that is implemented based on RFB architecture which supports concurrent dual-band dual-beam

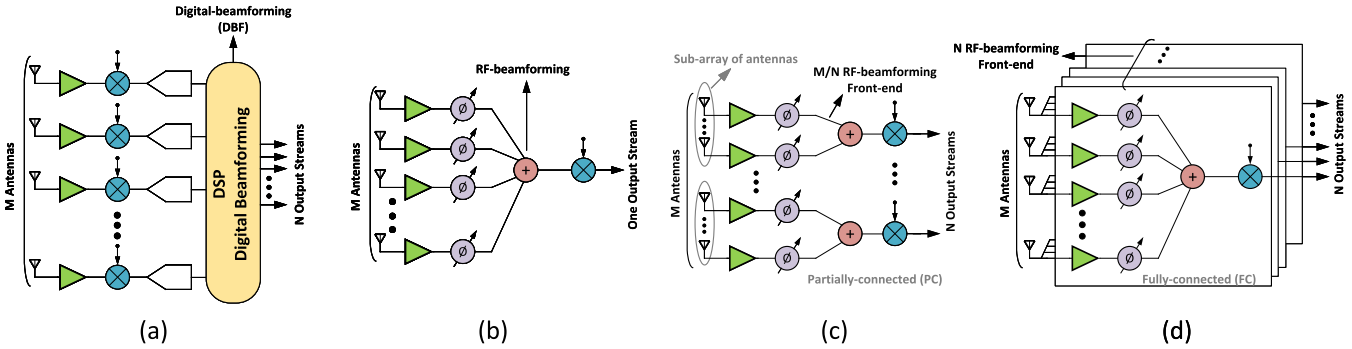

Fig. 1. Different types of beamforming. (a) DBF supporting N output streams. (b) RFB supporting only one output stream. (c) RFB supporting N output streams with PC configuration. (d) RFB supporting N output streams with FC configuration.

functionality. The unique phase shifter (PS) design which enables simultaneous RFB for two independent output streams results in a compact, power-efficient, and scalable architecture and robustness to spatial interfere signals. In addition, the use of RF null tuning using a variable gain low-noise amplifier (VLNA) results in more efficient spectral interfere cancellation. The front-end architecture uses a dual-band frequency response with mid-band rejection which achieves optimized bandwidth for lower and higher bands and canceling spectral interfere right after low-noise amplifier (LNA). In terms of circuit level, two authors' previous works for LNA [9] and PS [10] with significant modifications are used in this work as following.

1) The last stage of the LNA (third stage) in this work is optimized to be conjugate match to quadrature network (QN) of PS. To verify the results, elaborative EM simulations and system-level simulations are performed.
2) To achieve a compact system, a unique active PS is used where a gain-compensated two-stage RC-poly-phase filter (PPF) as the QN is shared between two independent vector modulators (VMs).
3) Two unique distributed active combiners along with their output matching networks are used to coherently combine phase-shifted signals in each output stream.
4) A customized four-element antenna array from 25 to 47 GHz which covers both mm-Wave bands simultaneously is designed to enable over-the-air (OTA) measurements with modulated signals.

Several single (multi)-beam/single (multi)-band RXs/transmitters (TXs) have been reported in literature [7], [8], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24]. In [20] and [23], a 16-element fully integrated 28-GHz digital beamforming (DBF) RX and a 28-GHz frequency-division multiplexing-based MIMO RX with spatial filtering are presented, respectfully. Both support four simultaneous beams but only support 28 GHz and do not work as dual-band beamformer. In [13], a 28-GHz phased array transceiver is realized as a 2×2 MIMO system. In the RX side, two independent RXs each with eight inputs and one output are implemented on the same die, and hence, two simultaneous streams are achieved. Since for each beam one phased array system is used, it is not area- and power-efficient.

In [8], a 25–30-GHz FC hybrid beamforming RX is introduced for MIMO communications. The RX supports two simultaneous received output signal streams. As a hybrid beamformer, part of combining is done in the analog domain and part of it through digital signal processing (DSP) in the digital domain. The architecture uses a Cartesian phase-shifting technique performed in the downconversion section. This approach has the advantage of avoiding any QN which eases the need for the amplifier to compensate the gain loss. In addition, this approach is inherently wideband. The work in [15] which is an expansion of [8] can support both 28-/37-GHz frequency bands and has two simultaneous output streams. This work presents the most comprehensive mm-Wave dual-band dual-beam concurrent beamforming topology. Although the two bands have relatively high gain difference and the middle band frequency rejection is very limited, it should be noted that the chip is realized in the 65-nm process.

In [22], a dual-band dual-beam phased array for 5G applications is presented. It can support dual-band and dual-beam operating using eight 28-GHz phased array transceiver chips and eight 39-GHz phased array transceiver chips on the board level. In this realization, each beam can only support one frequency of operation so the two output streams are not considered simultaneous because they cannot operate in the carrier-aggregation (CA) mode. Therefore, to have a phased array beamforming RX that can support two frequency bands for 5G applications (28 and 39 GHz), with dual beams where each is capable of working in either band simultaneously, a fully integrated mm-Wave concurrent dual-band dual-beam phased array RX front-end using RF beam forming architecture with FC antenna arrays and middle-band frequency rejection is presented in this article.

II. Review of MIMO/Beamforming Architectures

In the subset of MIMO systems, two main types of beamforming are used: DBF and RFB. In DBF [see Fig. 1(a)], spatial selectivity is achieved in the digital domain, which provides flexibility in beam/null adaptation. However, DBFs have several major challenges, including high power consumption and high cost due to the need for a RX/TX channel for each antenna. Another disadvantage is that interference cancellation is performed in the digital domain, which requires highly linear down/up-conversion mixers in the transceiver, making it challenging to realize especially at mm-Wave frequencies [7].

In RFB [see Fig. 1(b)], spatial selectivity is achieved in the RF domain. RFB has the advantages of simplicity and support for a large number of antennas, but it also has the challenge of low flexibility. Another challenge is that the conventional RF beamformers only support one stream. To be able to make them suitable to support multibeams, based on the connection of antennas (partially-connected (PC), or FC configurations), two architectures can be implemented [see Fig. 1(c) and (d)], but here the FC [see Fig. 1(d)] is desired due to its advantages over PC in terms of reducing spatial interferences, and higher antenna gain and efficiency (the beam in FC array is narrower) [19]. The advantage of Fig. 1(d) over DBF is that with a large number of antennas, the number of downconverters is limited to the number of streams, whereas in DBF, the number of downconverters and analog-to-digital (ADC) blocks increases with the number of antennas.

III. Concurrent Dual-Band Dual-Beam Phased Array Receiver Architecture

In the context of 5G communications, designing a phased array beamformer that can support multibands and multiple beams at mm-Wave frequencies poses significant challenges, as evidenced by the literature review. Most RFB phased array systems reported in the literature can only support one band and one stream, which is insufficient for 5G MIMO requirements. While having multiple independent phased array systems in one chip or PCB is a viable solution for supporting multibands, it is not power- or area-efficient, particularly for mobile handsets. Recent research has attempted to address this issue by presenting solutions that can support multibeams, albeit at the cost of a relatively high number of highly linear mixers, and typically only support one band, mostly at 28 GHz [8]. Supporting multiple bands is also a challenge, as 28 and 37 GHz are relatively separated frequencies requiring a wideband system, which is challenging for designing LNAs, PSs, and other components.

To overcome these challenges, a fully integrated mm-Wave concurrent dual-band dual-beam phased array beamforming solution is proposed. This design incorporates two independent output streams, allowing for three distinct scenarios: 1) both the output streams operating at 28 GHz; 2) both the output streams operating at 39 GHz; and 3) CA mode where one output stream operates at 28 GHz and the other operates at 39 GHz simultaneously, thereby increasing the data rate. This design overcomes the limitations of previous solutions and demonstrates the feasibility of supporting multiband and multi-beam in a power- and area-efficient manner. The proposed system functionality is illustrated in Fig. 2.

A. System-Level Architecture

Fig. 3 illustrates the block diagram of the proposed mm-Wave concurrent dual-band dual-beam phased array RX. This architecture is a 4 × 2 phased array MIMO RX that uses four input channels and two output streams. To achieve narrower beams and higher gain, FC topology over the PC one is chosen. The proposed architecture shares both mm-Wave LNA and QN, which has several advantages over: 1) a parallel architecture using twice the number of every block (LNA, PS, VM, combiner) for each stream or 2) an architecture with only shared LNA [15].

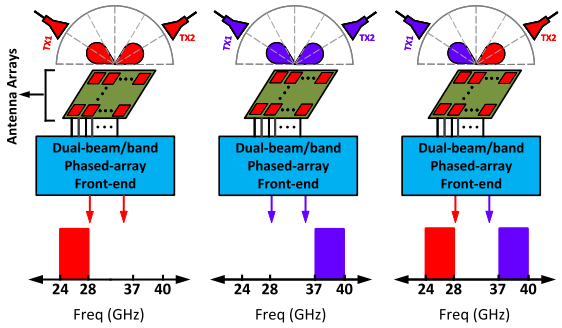

Fig. 2. Proposed concurrent dual-band dual-beam phased array RX different functionality scenarios.

One benefit of the proposed architecture is that the area of the LNA is relatively high, and by sharing the LNA, the area decreases notably while saving power consumption. Another advantage over the second architecture, where only the LNA is shared, is the ability to cascade the blocks in the receive path. This way, the high loading effect of VMs in the PS unit is not seen by the LNA. Instead, the LNA only sees the loading effect of one QN. However, this feature poses a significant challenge for the QN, since the loading effect of multisets of VMs directly affects its phase and gain accuracy. To address this challenge, a QN is used that is not sensitive to the capacitive loading effect of VM, as presented in [10] and [25].

While wideband [26] and reconfigurable [27] LNAs are reported in the literature, the proposed architecture also features the use of a mm-Wave dual-band LNA that covers 23.7–30.3 and 38–42.7 GHz in the first and second bands, respectively. In addition, notch filtering is performed in the middle band (31–36 GHz) to surpass out-of-band interference signals, which results in increasing linearity. Designing a dual-band frequency response with middle-band rejection is challenging, which is why the LNA uses a technique presented in [9], while the rest of the blocks are designed in a wideband manner, which is more straightforward compared with a concurrent design.

To achieve null tuning in the antenna beam pattern, the proposed LNA has a variable gain control feature with constant phase response for each gain setting. After the received signal is amplified in the LNA, quadrature signals are created in QN and fed to two sets of VMs, with each set working for one output beam. These four phase-shifted signals of four sets of VMs are combined in an active combiner and then sent to the RF output.

B. System-Level Simulations

To ensure the functionality of the proposed architecture in Fig. 3, various system-level simulations were conducted, as shown in Fig. 4, to validate the design capabilities, including single beam-steering, concurrent dual-beam operation, studying the effect of gain mismatch, and demonstrating RF-domain null-steering in a case study. These simulations are all conducted in MATLAB using mathematical equations for the proposed architecture. In this approach, each channel is modeled as a signal with a magnitude and a phase. The

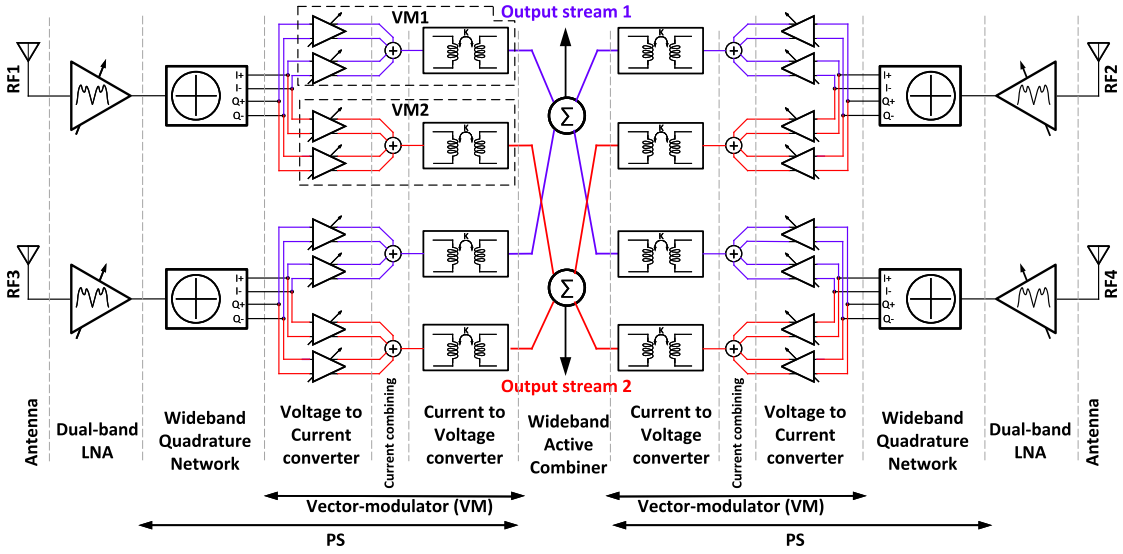

Fig. 3. Block diagram of the proposed mm-Wave concurrent dual-band dual-beam phased array RX front-end.

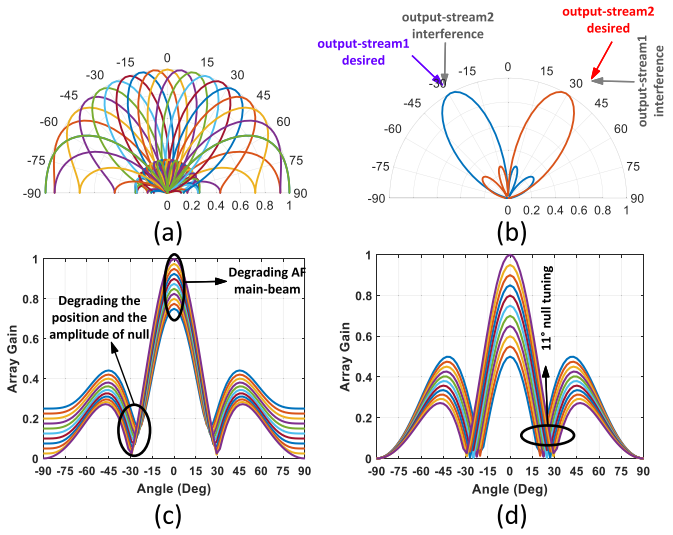

Fig. 4. System-level simulations at 28 GHz. (a) Single beam-steering with 11.25° steps a 28 GHz. (b) Concurrent dual-beam functionality. (c) Effect of gain mismatch on the AF. (d) Proposed RF null-steering with main beam at 0°.

magnitude is equal to the gain of the LNA and combiner together and the phase is the desired phase shift in PS. Then all the four channels are combined together, and the simulation results are shown in Fig. 4.

Fig. 4(a) demonstrates the single beam-steering functionality of the array for a single output stream at 28 GHz. The array uses a 5-bit PS, allowing beam-steering in the range of −90°–90°, with normalized amplitude. Fig. 4(b) shows the concurrent dual-beam functionality at 28 GHz, where two transmitted signals, one at −30° and the other at 30°, are received by the proposed phased array. The main beam and null of the first output stream are set to −30° and 30°, respectively. Similarly, the main beam and null of the second output stream are set to 30° and −30°, respectively. This configuration allows the array to nullify the interfering signal at the correct positions for each output stream, enabling two output streams to function concurrently. However, in cases where the interfering signal is not located at the null position, additional null steering or an increase in the number of antenna arrays may be required for optimal performance. Fig. 4(c) shows the effect of gain mismatch of one element among the four elements of the phased array, with the gain of that element multiplied by a factor of $0 \leq \text{cf} \leq 1$. As shown, the gain mismatch degrades the null and array factor. To address this issue, a VLNA is used to ensure minimal gain mismatch.

Null tuning is done using a nonuniform set of VLNA gain settings as demonstrated in Fig. 4(d). First, the main beam is selected by setting the PSs, and then null tuning is performed by setting the first and fourth front-end elements to maximum gain while multiplying the gain factor of the second and third front-ends by $0 \leq \text{cf} \leq 1$. Fig. 4(d) shows that up to 11° null-steering is achieved when the mean beam is at 0°. Although this approach may cause at most a 6-dB decrease in the gain of the array, it is useful when the interference signal saturates the system. VLNAs are used in each front-end to change the gain of each element. To prove the null tuning functionality, the normalized output signal equation for a four-channel phased array RX with $\lambda/2$ antenna spacing after simplification is given by

$$\begin{aligned} \text{Output} &= 1 + \text{cf} \times e^{-j\phi} + \text{cf} \times e^{-2j\phi} + e^{-3j\phi} \\ \phi &= \pi \sin(\theta) \end{aligned} \tag{1}$$

where θ is the beam incident wave angle with respect to horizontal line. Now for two cases of $\text{cf} = 1$ (uniform distribution) and $\text{cf} = 0$ (nonuniform distribution), the equations are equal to

$$\begin{aligned} \text{Output}(\text{cf} = 1) &= \frac{1 - e^{-j4\pi \sin(\theta)}}{1 - e^{-j\pi \sin(\theta)}} \\ \text{Output}(\text{cf} = 0) &= 1 + e^{-3j\pi \sin(\theta)}. \end{aligned} \tag{2}$$

Now, if both the equations are equal to zero, for the first equation, the null will be at 30°, and for the second, it will at 19° which shows that null position changes with different VLNA gains.

C. Link Budget Analysis

To take advantage of the features of 5G standard, mm-Wave frequencies are chosen to use wide channel bandwidths. The maximum channel bandwidth (BW_c) for 5G NR band n257 is 400 MHz [12]. Since 5G NR standard allows maximum equivalent isotropic radiated power (EIRP) of 75 dBm/100 MHz [28] and a single-element TX output power around 8 dBm is realizable for modulation schemes such as 64-QAM and 256-QAM [12], a TX array with 256 elements is assumed in this link budget analysis. In addition, the number of RX array antenna elements is chosen to be four. The downlink communication is implemented via 64-QAM signaling with the BW_c equal to 100, 200, and 400 MHz, and the gain of both the RX and TX single-element antennas are assumed to be 3 dB [12]. The distance between TX and RX arrays varies between 100 and 700 m in a line-of-sight fashion. According to the Friis equation

$$P_{RX} = P_{TX} + G_{TX,ANT} + 10\log\left(N_{TX,ANT}^2\right) - L_{FS} + G_{RX,ANT} + 10\log\left(N_{RX,ANT}^2\right) \quad (3)$$

where P_{RX}, P_{TX}, $G_{TX,ANT}$, L_{FS}, $G_{RX,ANT}$, $N_{TX,ANT}$, and $N_{RX,ANT}$ are the received power in a single element of the RX, transmitted power of a single-element of the TX, gain of the TX antenna per element, free-space path loss, gain of the RX antenna per element, and number of RX and TX antenna elements, respectively. On the other side, to have appropriate bit error rate (BER), P_{RX} needs to be more than the power level specified below

$$P_{RX,min} = -174\ \frac{\text{dBm}}{\text{Hz}} + 10\log(BW_c) + SNR_{out} + NF_{RX} + \text{Link Margin} \quad (4)$$

where BW_c is the channel bandwidth, NF_{RX} is the noise figure of RX per channel, SNR_{out} is the required output SNR at the output of RX, and Link Margin = 3 dB for antenna alignment loses [29]. To find out the required noise figure (NF) value for the proposed RX, the required error vector magnitude (EVM) is set, and then the required SNR_{out} can be obtained using the following equation [30]:

$$(SNR)_{out} = 20\log\left(\frac{1}{EVM}\right). \quad (5)$$

Fig. 5(a) shows the maximum allowable NF for the RX per channel versus different EVM percentages for different channel bandwidths where the distance is set to 300 m at 28 and 40 GHz. It can be seen that for worse case scenario where the channel bandwidth is 400 MHz and for EVM equal to 2%, the required NF should be smaller than 5 and 8 dB for 28- and 40-GHz frequencies, respectively. In addition, Fig. 5(b) shows the required NF for the RX versus distance from 100 to 700 m for different EVM percentages of 3, 4, and 5 for constant channel bandwidth of 400 MHz. It can be seen that the required NF for the 700-m communication range should be smaller than 4 and 2 dB at 28 and 40 GHz, respectively.

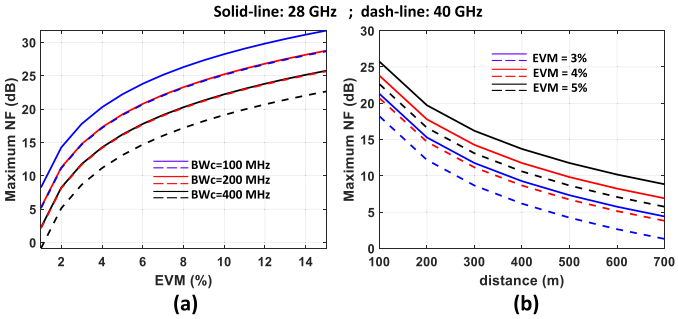

Fig. 5. (a) Required NF for the RX per channel versus different EVM percentages for different channel bandwidths at 300-m distance for communication. (b) Required NF for the RX versus distance for different EVM percentages at the 400-MHz channel bandwidth.

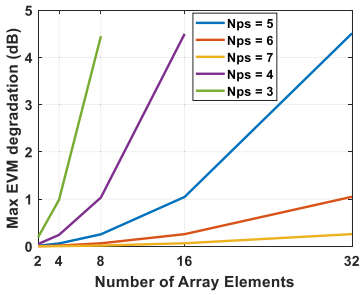

Fig. 6. Effect of phase step error on EVM.

D. Effect of Number of Bits of PS on EVM

As beam-steering is performed by changing the phase of each array element via the PS, the beam misalignment issue is directly related to the accuracy of the PS steps. The best case scenario is using continuous tuning phase shifting but digitally controlled phase shifting has its own advantages such as better control of the beam position. The maximum amount of EVM degradation due to beam misalignment as a function of the number of antenna elements in the array (N) and the number of bits in a digital PS (N_{PS}) is given by the following equation and is shown in Fig. 6 [31]:

$$\text{Max} - \text{EVM} - \text{degradation} = N \times \left[\frac{\sin\left(\frac{2*\pi}{4\times 2^{N_{ps}}}\right)}{\sin\left(N \times \frac{2*\pi}{4\times 2^{N_{ps}}}\right)}\right]. \quad (6)$$

Hence, this equation is not dependent on the frequency since it is related to the beam angle. Based on the fact that the maximum EVM degradation should be smaller than 3 dB [32], for $N = 4$ and $N_{PS} = 5$ in this work, the EVM degradation is well below 1 dB. It can be seen according to Fig. 6 that as the number of the array elements increases, the effect of the EVM will be worst and that is because of the fact that the beam in this situation is narrower and a more precise PS is required to compensate for EVM degradation.

IV. Circuit Design

As shown in Fig. 3, the proposed architecture has four inputs and two outputs. Each phased array front-end consists of a variable-gain dual-band LNA, wideband QN, two parallel sets

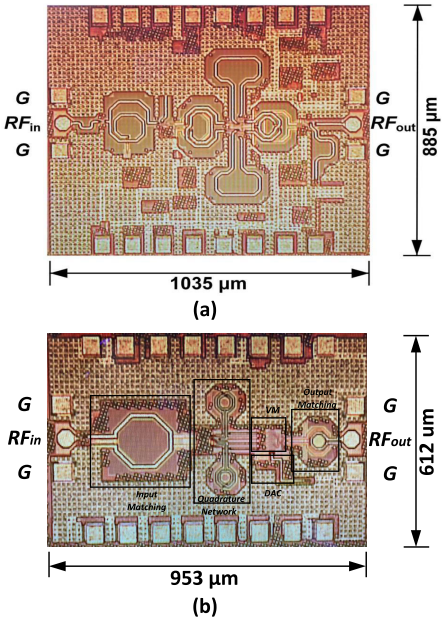

Fig. 7. Micrographs of (a) stand-alone LNA [9] and (b) stand-alone PS [10], both fabricated in the 22-nm CMOS FDSOI process.

TABLE I
STANDALONE LNA AND PS SPECIFICATIONS

Standalone Blocks Specifications			
LNA [9]		*PS* [10]	
Freq (GHz)	23.7 – 30.3 38 – 42.7	Freq (GHz)	24 - 36
Peak Gain (dB)	22 16	Gain (dB)	-8.2 ~ -5
NF (dB)	2.55 – 3.8 4.75 – 6.1	Resolution (bits)	11.25 (5)
Stopband rejection (dB)	19.2 13.2	RMS Phase Error (°)	< 4
Power (mw)	18	RMS Gain Error (dB)	< 0.6
Gain ctrl & range (dB)	8-step Digi. 7	Power (mw)	7.2
Area (mm^2)	0.915	Area (mm^2)	0.6

of Gilbert-cell VMs, and an active combiner. The proposed architecture is fabricated in the 22-nm CMOS fully depleted silicon-on-insulator (FDSOI) process. The circuits typologies and design considerations are described in this section.

A. Stand-Alone Blocks

To make sure that the LNA and PS used in this architecture meet the requirements for the array, their stand-alone test circuits are fabricated using the 22-nm CMOS FDSOI and are shown in Fig. 7. Those stand-alone blocks are tested and measured successfully and are explained in detail in [9] and [10], respectively. Table I shows the summary of the specifications of LNA and PS stand-alone blocks.

The dual-band LNA [9] is a three-stage cascode design with an active notch in the second stage for in-band rejection and an eight-step gain control in the third stage, with the layout shown in Fig. 7(a). The single-ended input–output design is for convenience of measurement. The first stage is a single-ended cascode structure to minimize the NF. The input matching network uses inductive source degeneration and coupled inductors for wideband matching. The interstage matching between the first & second stages and the second & third stages includes baluns for conversions between single-ended and differential. The second gain stage is differential to allow for cross-coupled pair realization boosting the quality factor of the in-band series notch generated by a series passive LC resonator. The cross-coupled pair is placed between input and cascode transistor. The gain of third stage is varied in a digital fashion with a 3-bit DAC to achieve eight different gain steps.

The wideband low rms phase/gain error active PS layout of [10] is shown in Fig. 7(b). The stand-alone PS is implemented differentially with single-ended (differential) to differential (single-ended) input (output) matching network for measurement purposes. As shown in Table I, the upper band frequency of PS is limited to 36 GHz, and it is because of a parasitic inductance that appears in series with shunt load capacitor due to routing at the secondary side of the double-tuned transformer and is not considered in the EM simulation, but in this work, more elaborative EM simulations are done to make sure all the parasitic inductors and capacitors are considered and PS works up to 40 GHz. In addition, PS is implemented in a differential manner as part of the RX array. The PS consists of a QN that creates differential orthogonal signals, followed by a Gilbert-cell VM that creates desired phase shifting based on quadrature signals. The QN is a two-stage RC PPF, the relatively high insertion loss of which is compensated using a shunt inductor at its output. The VM is implemented as a cascode stage to better isolate the current-summing section from load which results in better phase accuracy. The proposed PS used in this work has 11.25° (5 bits) accuracy, and the phase steps are controlled digitally through on-chip scan chain.

B. Quadrature Network to Two Parallel VMs Interface

Fig. 8 illustrates the connection of the QN to two parallel VMs to facilitate the concurrent generation of two output streams. Two shunt inductors (L_{sh}) are used at the output of the QN for gain compensation as discussed in [10]. Moreover, the architecture incorporates double the amount of loading capacitance in comparison to [10], contributing to an overall reduction in the footprint of the two shunt inductors and consequently, the overall area for each channel. Despite connecting the IQ network to two VMs, the overall interface area has been reduced by 50% compared with the configuration detailed in [10].

To preserve the accuracy of phase and amplitude for the quadrature signals, it is imperative to maintain a high degree of symmetry in the routing lines. As depicted in Fig. 8(a), the routing paths can be effectively modeled using a series inductance (L_{sI} and L_{sQ}). Given the capacitive nature of the input impedance of the VMs, the interface can be represented as a low-pass filter with a cutoff frequency well above the frequency band of interest. (With a input capacitance about 70 fF and $L_{sI(Q)} = 50$ pH, the cutoff frequency is around

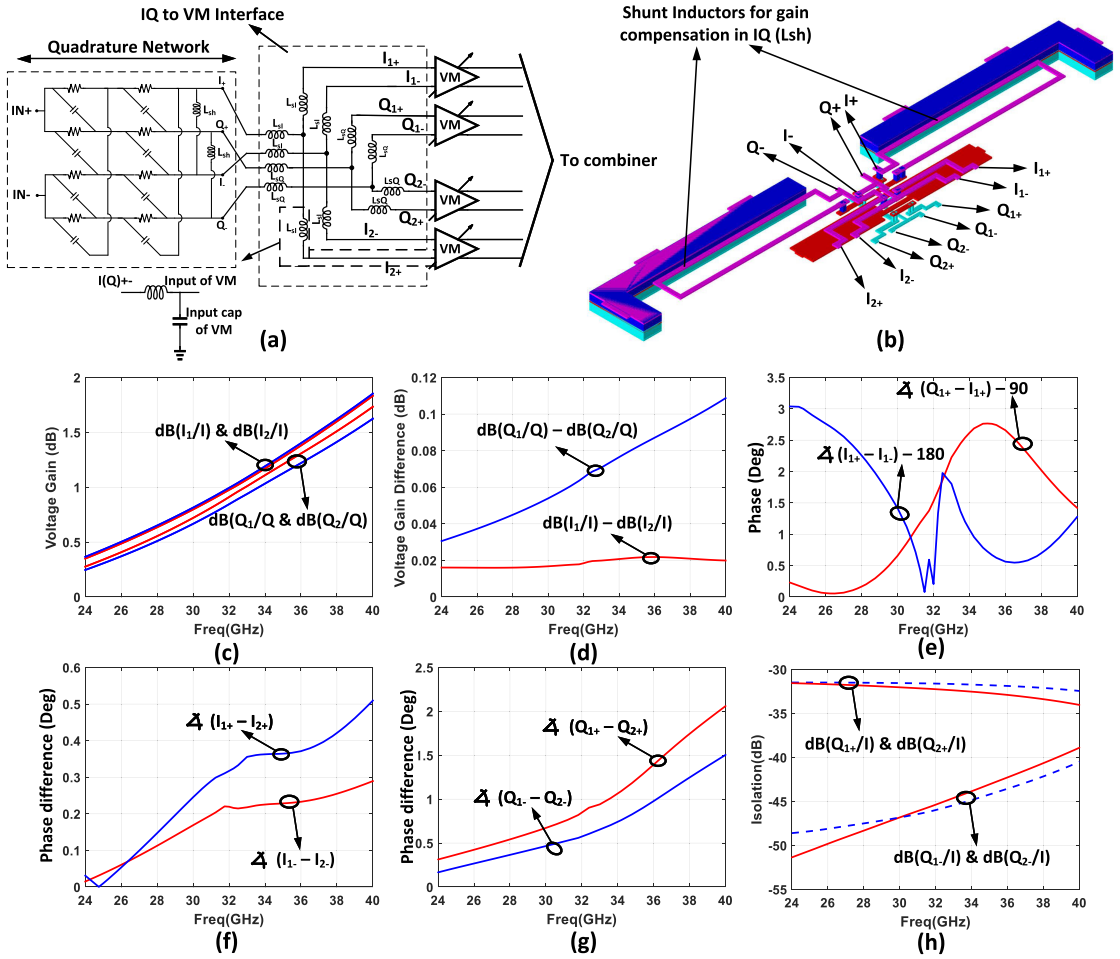

Fig. 8. Layout and simulation results for interface from IQ network to VM. (a) Simplified schematic of the IQ, VM, and the interface. (b) 3-D view layout of the proposed interface and the shunt inductor for gain compensation at IQ network. (c) Voltage gain of differential I and Q paths of two VMs. (d) Voltage gain difference of $I_1(Q_1)$ and $I_2(Q_2)$ paths. (e) Phase difference of quadrature and differential signals with respect to 90° and 180°, respectively. (f) Phase imbalance of two I paths. (g) Phase imbalance of two Q paths. (h) Isolation between I and Q paths when I is excited at the input of interface.

85 GHz.) Furthermore, meticulous effort has been made to minimize the length of the routing lines to mitigate their impact on the accuracy of the IQ network as shown in Fig. 8(b). Hence, series inductance, $L_{sI(Q)}$, along with the input capacitance of the VM results in increasing the capacitance value at the output node of QN. As a result, the value of L_{sh} needs to be reduced to compensate for this effect. Fig. 8(c) presents the differential voltage gain characteristics of the interface, with the gain ranging from 0.5 to 1.5 dB. Meanwhile, Fig. 8(d) provides insight into the gain imbalance between the I and Q paths, which remains under 0.12 dB across the entire frequency band of interest. The phase behavior of the interface is depicted in Fig. 8(e), showing phase imbalances within 3° for both the quadrature and differential signals with respect to 90° and 180°, respectively. Fig. 8(f) and (g) further elaborates on the phase imbalances between the I and Q paths. Notably, Fig. 8(g) illustrates a peak phase imbalance of 2° at 40 GHz, attributed to the increased usage of vias in the layout for routing from the IQ network to the Q path of the two VMs. Finally, Fig. 8(h) highlights the isolation between the I and Q sections under excitation of an ac signal in I while testing Q. The observed isolation exceeds 30 dB, signifying robust isolation. The addition, the weaker isolation on the positive side of the Q section is attributed to its proximity to the I path, as shown in Fig. 8(b). Exciting ac signal in the Q path and looking at the isolation in the I path provide similar results as in Fig. 8(h).

C. Interface of VM to Combiner

A double-tuned transformer is used between the interface of the output of the G_m cell of the VM (voltage-to-current converter which is shown in Fig. 3) to the input of the combiner as shown in Fig. 9(a). This wideband load provides sufficient voltage gain for the frequency band of interest. The 3-D view of the layout of the proposed transformer is shown in Fig. 9(b). According to [26], the value of inductance and capacitors can be calculated using the following equations:

$$k_{\text{flat}}^2 \approx \frac{1}{1+Q^2} \approx \frac{L_1}{L_1 + R_1^2 C_1} \tag{7}$$

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \frac{1}{\sqrt[4]{1-k^2}}. \tag{8}$$

By increasing k to be greater than k_{flat}, the bandwidth of the double-tuned transformer increases at the cost of having

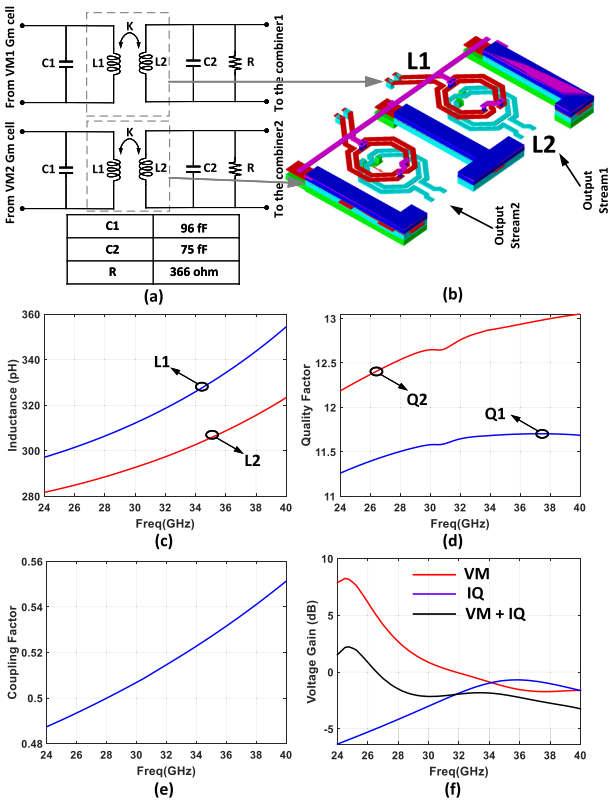

Fig. 9. Layout and simulation results of interface between the VMs and combiner. (a) Double-tuned transformer used between the output of the VM and the input of the combiner along with the values of capacitors and the resistor. (b) 3-D view layout of the wideband load (interface between VM G_m cell and the combiner). (c) Inductance values of two inductors L_1 and L_2. (d) Quality factor of inductors L_1 and L_2. (e) Coupling factor of the transformer. (f) Voltage gain of VM, IQ network, and VM + IQ.

higher in-band variation [26]. In addition, ω_0 is the center frequency where the voltage gain has it own maximum for $k < k_{\text{flat}}$, but for $k > k_{\text{flat}}$ the voltage gain will have two peaks at two frequencies, one lower than ω_0 and the other higher than ω_0. Since in this work, the frequency range is assumed to be 24–40 GHz, ω_0 is chosen to be 31 GHz and also k is chosen to be more than $k_{\text{flat}} = 0.18$, and therefore, two voltage gain peaking is achieved one before ω_0 and one after. According to ω_0 and k choices, the initial values of L_1 and L_2 are found. Then, by doing some optimization, the final values of L_1, L_2, C_1, and C_2 are achieved. Fig. 9(c)–(e) shows the characteristics of the proposed transformer. The values of inductors L_1 and L_2 are around 320 and 300 pH with quality factor Q_1 and Q_2 around 11.5 and 12.5, respectively. In addition, the coupling factor between two inductors is around 0.52. Fig. 9(f) shows the voltage gain of VM, IQ, and VM + IQ. As shown, the voltage gain of VM and IQ is optimized to have overall flat frequency response for input of IQ network to the output of the VM. Therefore, the gain difference in IQ network (~ -5 dB) is compensated by the voltage gain response of VM. VM + IQ voltage gain has a peak voltage gain of 1.5 dB from 24 to 28 GHz and the peak voltage gain of -2.5 dB from -36 to 40 GHz and also it has less than 3.5-dB gain variation from 24 to 40 GHz.

D. Wideband Distributed Active Combiner

1) Combining Core: One of the most challenging circuits in a phased array RX system is the combiner where the phased shifted signals should be combined together and sent to the output. During this process, the combining technique has to be accurate and any mismatch in combining results in lowering the SNR of output signals. In addition, since the combiner adds the phase-shifted signals of different channels together, and each of these signals comes from a different point of chip and relatively far from each other, the signal routings in the combiner should be considered as distributed elements. The combiner can be realized as a passive or active component. One commonly used integrated passive combiner for mm-Wave phased array RXs is the Wilkinson combiner [33]. They do not consume any power and are linear, but they have large footprint and are lossy. They also have lower isolation compared with their active counterparts. Therefore, a wideband distributed active combiner is introduced in this article which is shown in Fig. 10(a). In this circuit, the output phase-shifted voltage of the VM is converted into ac current through transistor M1 [34]. Then, this current is carried through transmission lines TLs to the cascode transistor M2. The first step of current combining is performed at the output of the cascode transistors. The reason for using TLs between M1 and M2 is the fact that the distance between these two transistors is comparable to $\lambda/10$ and it should be considered as a distributed element. The 3-D view layout of the proposed TLs is shown in Fig. 10(b). The input impedance that is seen from the source of the cascode transistor M2 to the top is approximately equal to $(1/g_m)$. Therefore, if the characteristic impedance of TLs is equal to $2 \times (1/g_m)$, and the loss of the transmission line is negligible, TLs perfectly transfer the power to the cascode transistor M2 and will not affect the voltage gain of the combiner. Fig. 10(b) also shows the cross section view of the proposed TLs' transmission line. To increase the isolation, the signal lines (S), which are realized with metal layer QA, are located in a cavity where top, bottom, and sides are shielded with ground through metal layers QB, JA, and QA, respectively. Then, after the currents were combined in cascode transistor M2, to achieve even more isolation another current combining is performed through transistor M3. Finally, the output current is converted into voltage through a wideband double-tuned transformer and is transferred to the output by a 50-Ω transmission line (TL_L) which is explained in detail in Section IV-D2. M_{CS} gate voltage VCS is set to achieve 5.625-mA current for each channel of the combiner. M2 gate voltage (VBCS) is optimized to achieve maximum linearity in the combiner, while the gate voltage of M3 is connected to VDD to provide enough headroom for M2.

The postlayout simulation results of the proposed combiner core are shown in Fig. 10(c)–(j). Fig. 10(c) shows the voltage gain of the combiner when different signals are applied to one, two, three, and four channels; also, the gain difference between two combiners is because of the difference in the length of TLs. It can be seen that the 3-dB bandwidth is met from 24 to 40 GHz. In addition, the gain difference is shown in

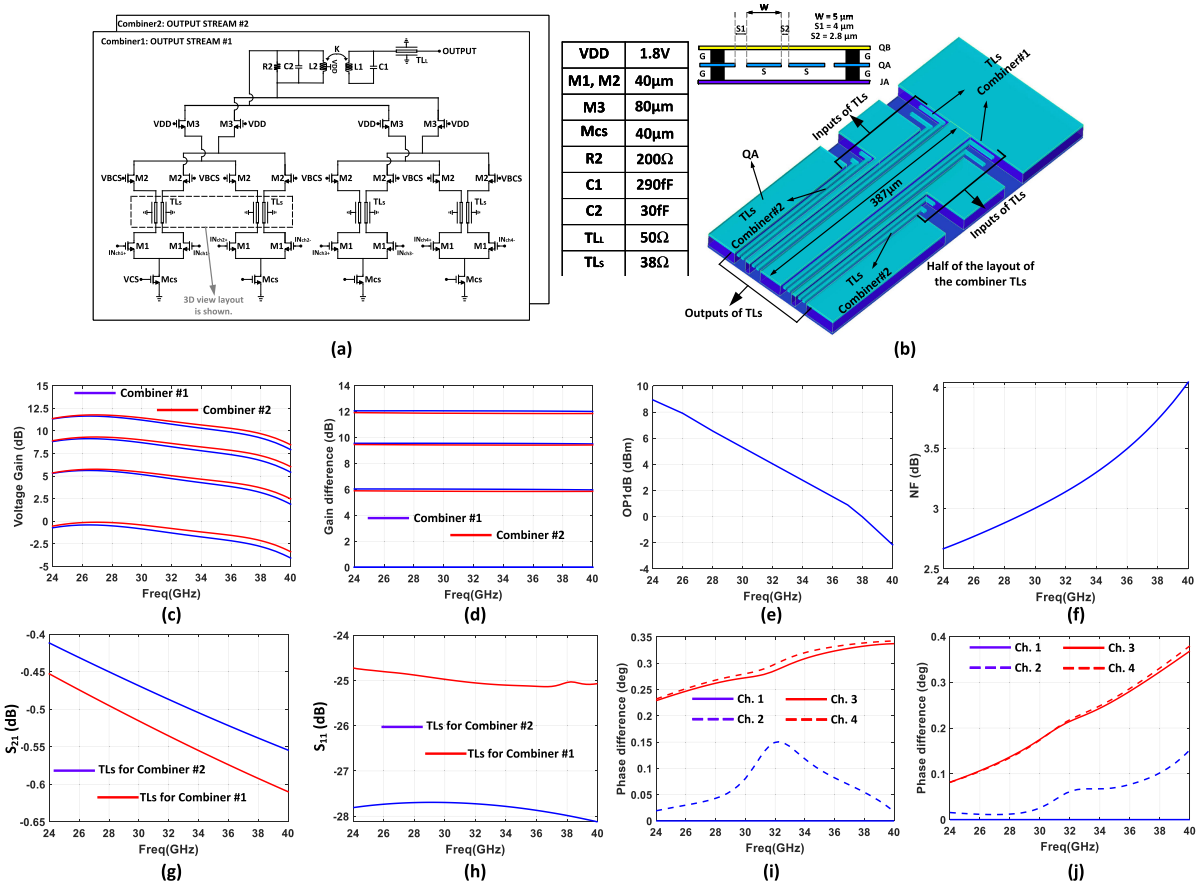

Fig. 10. Schematic, layout, and simulation results of the proposed distributed active combiner. (a) Schematic of the proposed combiner and its corresponding table. (b) 3-D view layout and cross section view of the proposed TLs for combiner1 and combiner2. (The layout is shown for half of the combiner routings. Also, in this view QB is removed and is shown in cross section view.) (c) Voltage gain of the combiner when signal is applied to one, two, three, or four channels. (d) Voltage gain difference for different voltage gains. (e) OP1dB. (f) NF of the combiner versus frequency. (g) Insertion loss of the proposed TLs for combiner1 and combiner2. (h) Input return loss of TLs for combiner1 and combiner2 when $Z_0 = 38\ \Omega$ for a terminated 38-Ω load. (i) Phase difference at the output of combiner1 when each time only one channel is ON and others are OFF based on channel1 of combiner1. (j) Phase difference at the output of combiner2 when each time only one channel is ON and others are OFF based on channel1 of combiner2.

Fig. 10(d), where the ideal values are 0, 6, 9, and 12 dB. As can be seen, the simulation results are very close to ideal values. The active combiner core needs to have a relatively high output P1dB (OP1dB) as shown in Fig. 10(e). Fig. 10(f) shows the NF of the combiner. Since the combiner is the last block in the system, its NF will not affect the overall NF of single channel of the array, although by itself it shows relatively good NF which is below 4 dB for 24–40 GHz. Fig. 10(g) and (h) shows the characteristics of the proposed TLs' transmission line and since g_m of the cascode transistor M2 is 52 ms, the differential characteristic impedance of TLs should be 38 Ω. Therefore, S_1, S_2, and W are chosen to provide this impedance value. Fig. 10(g) shows S_{21} of the transmission line which is >-0.65 dB for the entire band. Fig. 10(h) shows S_{11} of the TLs which is terminated by a 38-Ω differential load ($Z_0 = 38\ \Omega$). It can be seen that S_{11} is below -27 dB for 24–40 GHz. Fig. 10(i) and (j) shows the phase difference at the output of two combiners when at each combiner only one channel is ON at the time and others are OFF, then the phase differences in four channels for each combiner are reported based on the phase response of channel1 of the corresponding combiner at the output. It can be seen that the maximum phase difference for all the states is $<0.4°$.

2) Output Matching Network With 50-Ω TL (TL_L): The output matching circuit of the combiner in Fig. 11(a) consists of two parts: first, the lumped-element section which is a double-tunded transformer, two capacitors (C_1, C_2), and a resistor (R_2) [see Fig. 10(a)] matches the output impedance of the combiner to 50 Ω. It also converts the final summed current into the voltage and acts as differential to single-ended converter. To route this single-ended signal to output path for each stream, a 50-Ω single-ended transmission line is used. Fig. 11(a) shows the 3-D view layout of the output matching circuit along with 50-Ω transmission line where the signal line is realized using top metal (LB) and is shielded through side grounds using top metal LB and the metal layer QB for the bottom ground plan. The width of the signal line ($W = 4\ \mu$m) and the spacing between the signal line and side grounds ($S = 20\ \mu$m) are optimized so that overall line achieves 50-Ω characteristic impedance. Fig. 11(b) and (c) shows the inductor values and quality factors for the primary and secondary inductors of the double-tuned transformer are extracted using the equations in [26] and are 400 pH, 100 pH, 8, and 10, respectively. Fig. 11(d) shows the coupling factor of the transformer which is around 0.5. Fig. 11(e) and (f) shows the S_{11} and S_{21} of the single-ended 50-Ω transmission

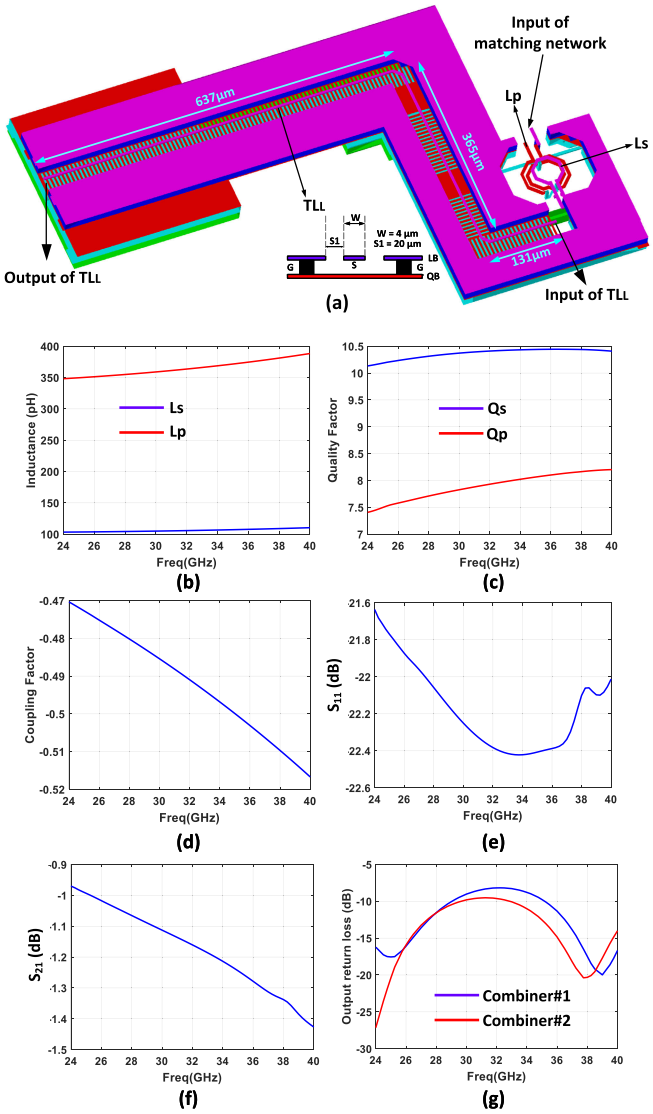

Fig. 11. Output matching of the combiner. (a) 3-D view layout of the matching network along with 50-Ω transmission line. (b) Inductance values of primary and secondary inductors in the transformer. (c) Quality factors of two Lp and Ls inductors. (d) Coupling factor. (e) S_11 and (f) S_21 of TL_L. (g) Output return loss of the combiner.

line which S_{11} is better than -21 dB and S_{21} is less than -1.5 dB over the 24–40-GHz range. Finally, Fig. 11(g) shows the output return loss of the combiner which is better than -10 dB for both the 24–28- and 37–40-GHz frequency bands. The proposed phased array RX uses two combiners for two output streams that both of them consume 45-mA currents together which shows that each channel consumes 5.625 mA and the supply voltage of the combiner is 1.8 V.

E. Antenna Array Design

To be able to measure beam-steering and OTA EVM, two sets of customized microstrip patch antenna arrays are designed for each lower and higher sides of the mm-Waveband. Two customized antenna arrays comprise four microstrip patch antenna elements which are shown in Fig. 12(a) and (b). RT/duroid 5880LZ laminate is used as the

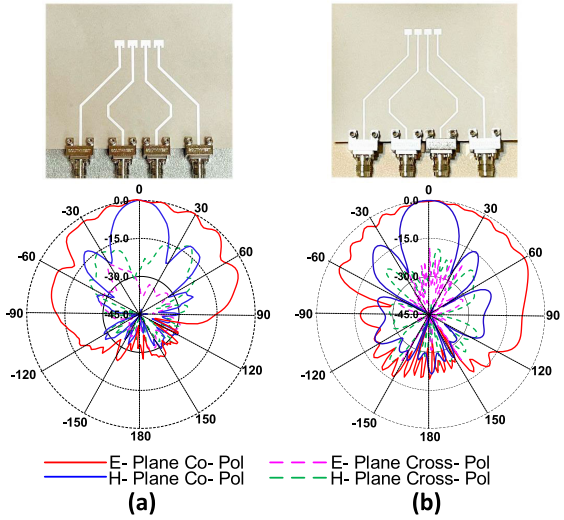

Fig. 12. Two customized microstrip patch antenna arrays working at (a) 26.5 and (b) 40 GHz, with their corresponding E- and H-plane measured beam pattern results [35].

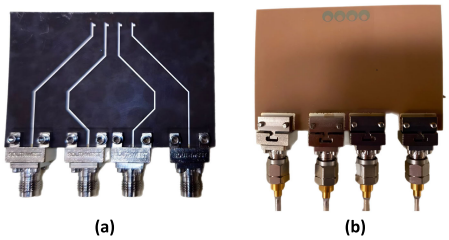

Fig. 13. Four-element dual-band antenna array fabricated layout. (a) Front–side view. (b) Back-side view.

substrate to provide adequate matching for the two mm-Wave frequency bands. Two 26.5- and 39.5-GHz antenna arrays achieve bandwidths of 1.8 and 2.3 GHz and gains of 12.9 and 12.4 dB, respectively. In addition, to avoid grating lobes for $+/-50°$ at mm-Wave, the antenna element spacing is set to 0.55 wavelength. The realization of these arrays is explained in more detail in [35].

In addition, a broadband antenna array from 25 to 47 GHz which covers both the mm-Wave bands simultaneously is shown in Fig. 13. The wideband antenna array takes advantage of printed slot antenna elements where a circular patch located inside a circular slot etched off the ground plane is excited by a feedline on the other side of the board terminated by a shunt stub to enable matching for a broad bandwidth as well as constant gain and linear polarization and pure radiation pattern within two mm-Wave bands [36].

The fabricated two sets of single mm-Wave bands (26.5 and 39.5 GHz along with the fabricated four-element broadband antenna array operating from 25 to 47 GHz) are used for OTA EVM measurement to show dual-band dual-beam operation.

V. Fabrication and Measurement

The concurrent phased array RX front-end is fabricated using the 22-nm FDSOI CMOS process from Global Foundries. The photograph of the die under microscope is shown in Fig. 14. The die has a length of 2738 μm, a width

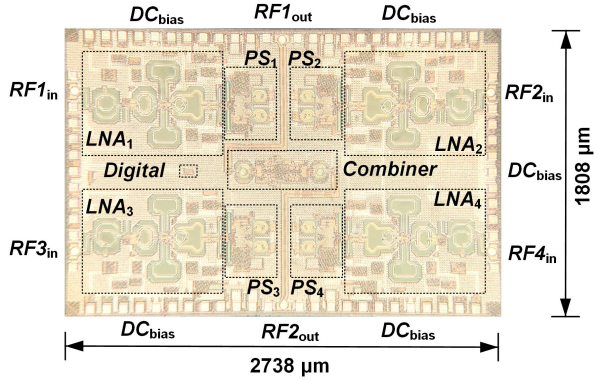

Fig. 14. Die photograph of the concurrent dual-band dual-beam phased array RX.

(a) (b)

Fig. 15. (a) Top view of four probes in the probe station. (b) Test setup of OTA measurement.

of 1808 μm, and an area of 4.95 mm^2 including all dc, RF pads, and decoupling capacitors. This phased array RX front-end is measured on wafer and by probing the dc biasing, RF input, and output using four customized InfinityQuad multicontact RF probes from FormFactor, shown in Fig. 15(a). The cables and the RF probes are deembedded by through, open, short, and matched (TOSM) calibration substrate for the single-channel characterization by network analyzer. The Rohde & Schwarz ZVA67 network analyzer was used to perform S-parameter, 1-dB compression point, and third order intercept point (IIP3) measurements. The Rohde & Schwarz FSV40 spectrum analyzer and Pasternack PE85N1008 noise source performed the NF measurement. The front-end consumes 54.8 mW with a supply voltage of 0.8 V for the first stage and 1 V for the second and third stages of the LNA, 1.2 and 1.8 V for the PS and combiner estimated per-channel per-stream at the maximum gain setting.

For OTA measurement, the ETS-Lindgren 3116C double-ridged waveguide horn antenna and customized patch array antennas [35] (one for the lower band and, one for the upper band, and one as a dual-band) are used, and the deembedding of the path loss is done manually by measuring two horn antennas at the same locations. The horn antenna is mounted on the Oben CT-2491 Carbon Fiber Tripod. The ZVA67, the oscilloscope, and the Keysight M8190A arbitrary waveform generator (AWG) performed

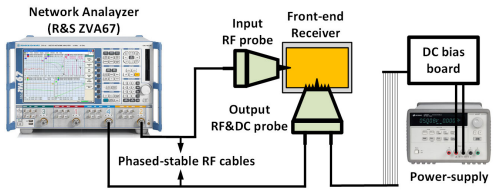

Fig. 16. Setup of single-channel characterization.

the EVM measurement including the commercially available upconverter board (EVAL-ADMV1013) and downconverter boards (EVAL-HMC977LP4E/EVAL-HMC6789BLC5A for the lower/upper band) addressing the limitation of analog bandwidth of the AWG. Due to the limitation of the lab environment, all the OTA measurements are carried in a regular laboratory, shown in Fig. 15(b).

A. Single-Channel Characterization

In Fig. 16, the single-channel characterization test setup is shown and performed with four multicontact RF probes for RF inputs, RF outputs, and dc biasings measured by ZVA67. Fig. 17(a)–(c) shows the measured and simulated results for different gains (S_{5X}/S_{6X}, $X = 1, 2, 3, 4$), input return losses ($S_{11}/S_{22}/S_{33}/S_{44}$), output return losses (S_{55}/S_{66}) versus frequency, respectively. The measured 3-dB gain bandwidth is from 23 to 30 GHz for the low bands with a peak gain of 21 dB at 29 GHz, and form 36 to 40 GHz for the high bands with a peak gain of 18 dB at 38.5 GHz. The measured input return losses are better than -10 dB from 23.8 to 40 GHz. The measured output return losses are better than -10 dB from 20 to 32 and 36 to 40 GHz. The notch is 0 dB at 33.5 GHz; compared with the low band the rejection is around 21 dB. Fig. 17(d) shows the measured stability factor K for each channel. The measured K is larger than 1 across the entire band. Although the measured stability factor K has some degradation compared with simulations, it still satisfies the necessary and sufficient conditions for unconditional stability $K > 1$ and $B1 > 0$.

The measured and simulated NFs are shown in Fig. 17(e). The Y-factor method was used for NF measurement. The minimum measured NF is 6 dB at 28 GHz. The NF is measured up to 40 GHz due to the limitation of the spectrum analyzer, and the NF is 9 dB at 40 GHz. In Fig. 17(f), the measured results of input IP3 and input 1-dB compression point are shown. The IIP3 is measured with 10-MHz two-tone spacing at each frequency. IIP3 varies from -18 to -13 dBm, and the input 1-dB compression point varies from -25 to -18 dBm for the lower band. IIP3 varies from -12 to -11 dBm, and the input 1-dB compression point varies from -22 to -21 dBm for the higher band. The measured and simulated phase errors and gain errors are shown in Fig. 17(g) and (h). The rms phase and gain errors are less than 6° and 1.2 dB for the entire frequency band, respectively. RMS phase and gain error are low enough to ensure the effects of these errors on the main lobe shape are negligible as well as the effect of maximum phase error since it only exists for one phase state which is only for one channel while four antenna elements are used. In addition, both rms phase/gain errors

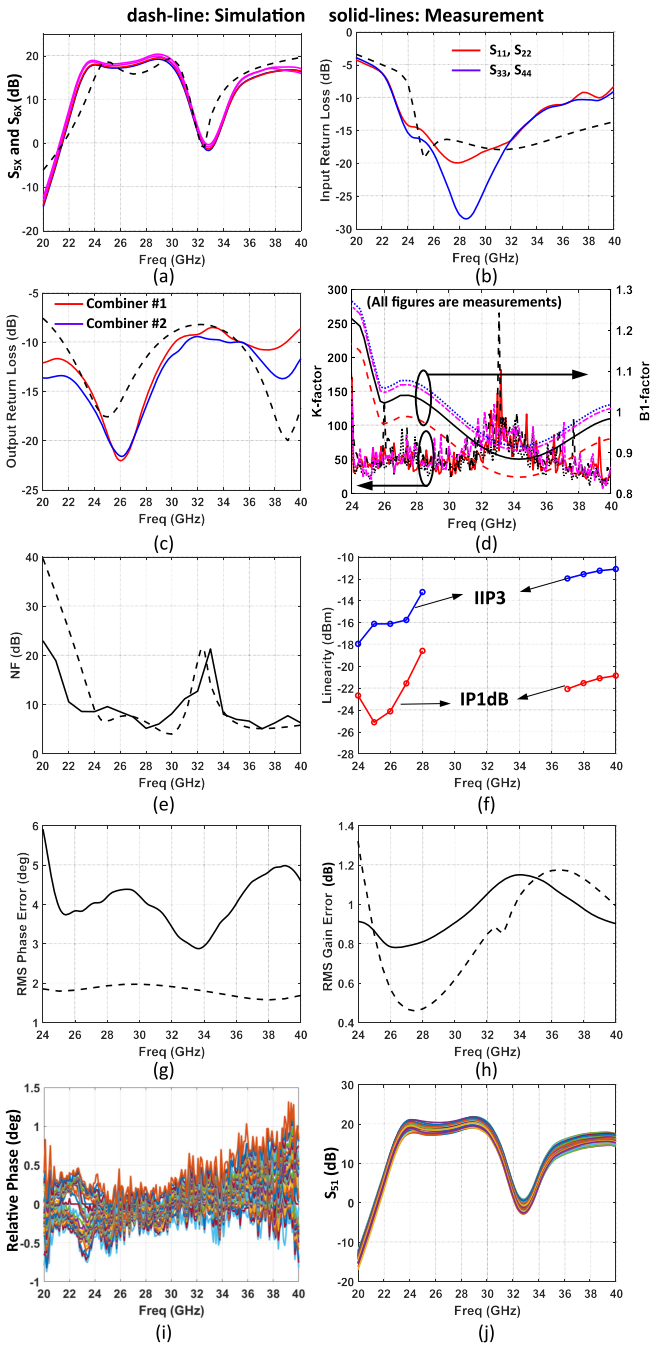

Fig. 17. Simulation and measurement results for single-channel characterization. (a) S_{5X} and S_{6X} where $X = 1, 2, 3, 4$. (b) Input return loss of four channels. (c) Output return loss of two output streams. (d) K-factor and $B1$-factor for four channels. (e) NF for channel1. (f) IIP3 and IP1dB for channel1. (g) RMS phase error for channel1. (h) RMS gain error of channel1. (i) Relative phase error of channel1 of output stream 2. (j) S_{51} (channel1 to output1) for 32 phase steps.

show good consistency with the simulation results. Fig. 17(i) shows the relative phase of channel1 of stream2 with constant phase steps when all 32 phase steps of channel1 of stream1 are swept. It shows that the relative phase changes at most by 1.5°. This result also shows that the beam of second stream is not affected when the beam of first stream is changed because the number of input channels is four the half power beamwidth (HPBW) for a four-element antenna array which is relatively high, and therefore, 20° beam-steering is done. If the spacing between antenna elements is exactly one half of the signal wavelength, then the phase difference between two adjacent channels is equal to $\pi \sin\theta$ (where θ is the beam angle), and for 20° beam-steering steps, the effect of steering beam 1 (changing the first PS of each channel on beam 2 (the second PS of each channel) is negligible. Fig. 17(j) shows the voltage gain of stream1 for channel1 with different 32 phase steps of the same stream. As can be seen, the gain variation is within 17–21 dB.

B. Beam-Steering Measurement

The OTA beam-steering measurements are performed with two customized patch antenna arrays as the RX antenna by probing with four multicontact RF probes for RF inputs, RF outputs, and dc biasings for two frequencies at 26 and 39 GHz, respectively, while a horn antenna is mounted on the tripod in the far-field (the distance between the horn antenna and the patch antenna array is 1 m) and rotated at different angles on the TX side transmitting a continuous wave (CW) (continuous waveform) signal from ZVA67 in Fig. 18(i). To perform the OTA measurements with wafer probing, the customized patch antenna array was connected to RF probes using short semi-rigid coaxial cables with very low loss (IL ~ -0.2 dB at 40 GHz). The RX is programmed using an Arduino board for different settings of the phase for each channel under test to steer the beam for tracking the rotated TX antenna. The 0° ON-axis, +20°/30°/40°, and −20°/30°/40° OFF-axis beam-steerings are tested. The E-plane patterns are measured at 26 and 39 GHz without any phase or amplitude calibration, and the results match well with simulations. The measured and simulated beam patterns at 26 GHz are shown in Fig. 18(a)–(e), and the beam patterns at 39 GHz are similar to those at 26 GHz. The sidelobe levels are ≤ -10 dB over all the scan angles (without tapering).

The concurrent functionality has been tested with one customized dual-band patch antenna array for 28 and 40 GHz simultaneously, while two horn antennas were mounted on two tripods in the far-field (1 m away) at two different directions as the TX antennas, shown in Fig. 18(j). The peak of the first beam is aligned with the null of the second beam, while the null of the first beam is aligned with the peak of the second beam simultaneously. The measured and simulated dual-beam patterns are shown in Fig. 18(f)–(h). In Fig. 18(f), the array on the RX side is programmed in a way that the first beam is steered at 0°, and the second beam is steered at 30°. On the TX side, one horn antenna is placed at 0° transmitting at a 28-GHz CW signal, and another horn antenna is placed at 30° transmitting a 40-GHz CW signal. In Fig. 18(g) and (h), the results are shown for 20° at 28 GHz and −40° at 40 GHz, 30° at 28 GHz and −30° at 40 GHz, respectively. The measured results match well with simulations, and the measured results show the concurrent functionality of the array.

C. Null Tuning

In the system-level analysis sections, it was mentioned that one of the advantages of dBF over the radio frequency (RF) beam-forming (RFBF) is that in dBF, in addition to the

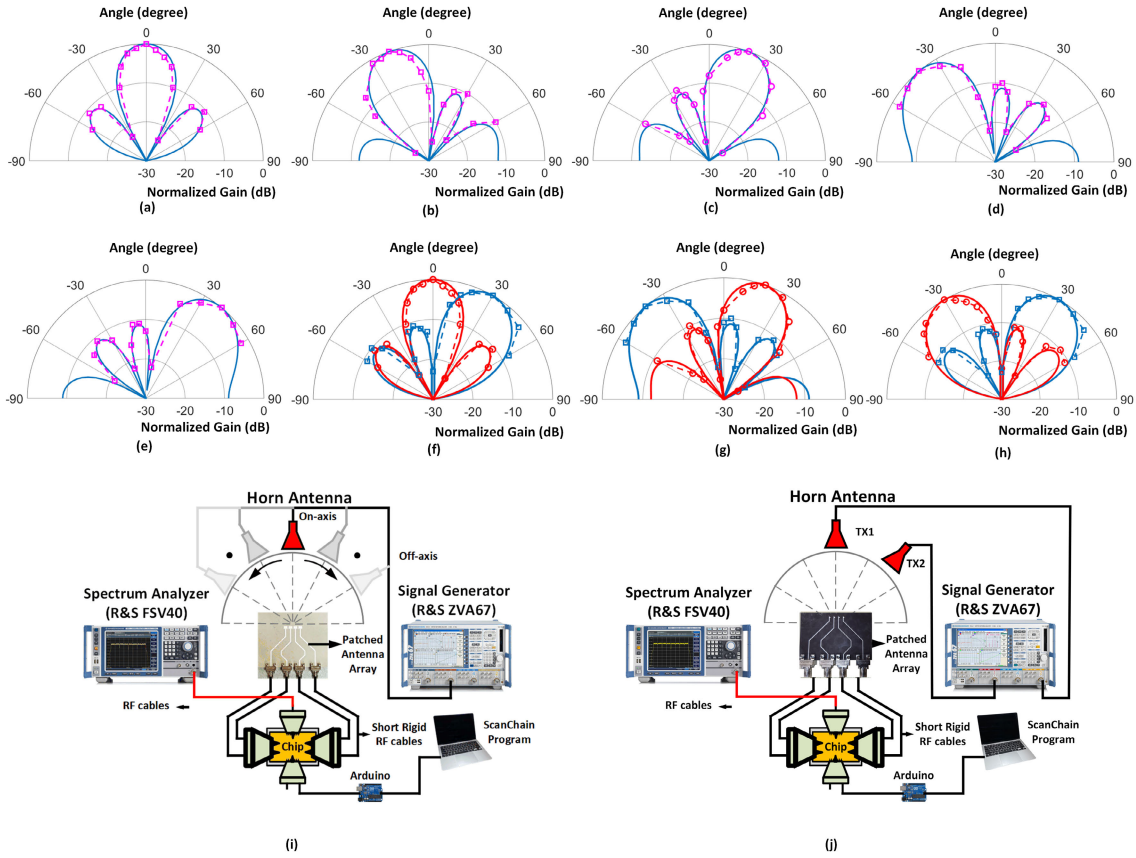

Fig. 18. Measured (dashed line) and simulated (solid line) single-beam patterns. (a) 0°. (b) −20°. (c) 20°. (d) −40°. (e) 40°. Measured (dashed line) and simulated (solid line) dual-beam patterns. (f) 0°/30°. (g) −40°/20°. (h) −30°/30°. (i) Measurement setup for OTA beam pattern using horn antenna and four-element narrowband patch antenna. (j) Measurement setup for OTA concurrent two-beam using two horn antennas and four-element dual-band patch antenna.

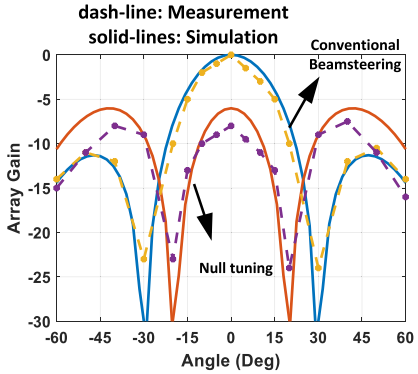

Fig. 19. Measured null tuning when the beam is set at 0° at 28 GHz.

location of maximum, the location of nulls is also adjustable. But in RFBF if the distribution of amplitude is not uniform, the location of null can also be adjusted at the cost of loosing gain for the maximum angle. In Fig. 19, the gain of channel numbers 2 and 3 of the output stream one is set to 0 and channel numbers 1 and 4 are set to their maximum values at 28 GHz. Then, beam-steering is compared with the conventional situation. It can be seen that for the proposed approach at the cost of 6-dB loss, the null position is changed from 30° to 20°. The null tuning uses a lookup table for a specific null angle.

D. Measurements With Modulated Signals

EVM measurements were performed in both cable-only and OTA tests. For the cable-only EVM tests, on the TX side, various modulations such as QPSK, 16QAM, 32QAM, and 64QAM signals are generated by the AWG at an IF frequency of 3.3 GHz and upconverted by the aforementioned upconverter board to mm-Wave frequency through cables, shown in Fig. 20(e). Due to the limitations of the oscilloscope specifications available in the laboratory, the measured EVMs are tested with 100-, 200-, 400-, and 500-MBd rate, respectively. The received signal was downconverted by the downconverter board and sent to the oscilloscope. Then the EVM results of received signal were calculated using Path-wave software [37]. For 28 and 40 GHz, the EVM is tested for QPSK, 16QAM, 32QAM, and 64QAM, respectively. The constellations of 64QAM are shown for both 28 and 40 GHz and outputs 1 and 2 in Fig. 20(a) and (b). Outputs 1 and 2 show similar results, and the EVM is better than −25.25 dB at 28 GHz, and −26.78 dB at 40 GHz. The 40 GHz has slightly better performance than 28 GHz, and this is due to different performance of two downconverted boards.

For OTA EVM measurements, for dual-beam single-band operation, two customized patch antenna arrays one resonating at 28 GHz and the other one resonating at 40 GHz are used, while for the concurrent dual-band dual-beam measurements

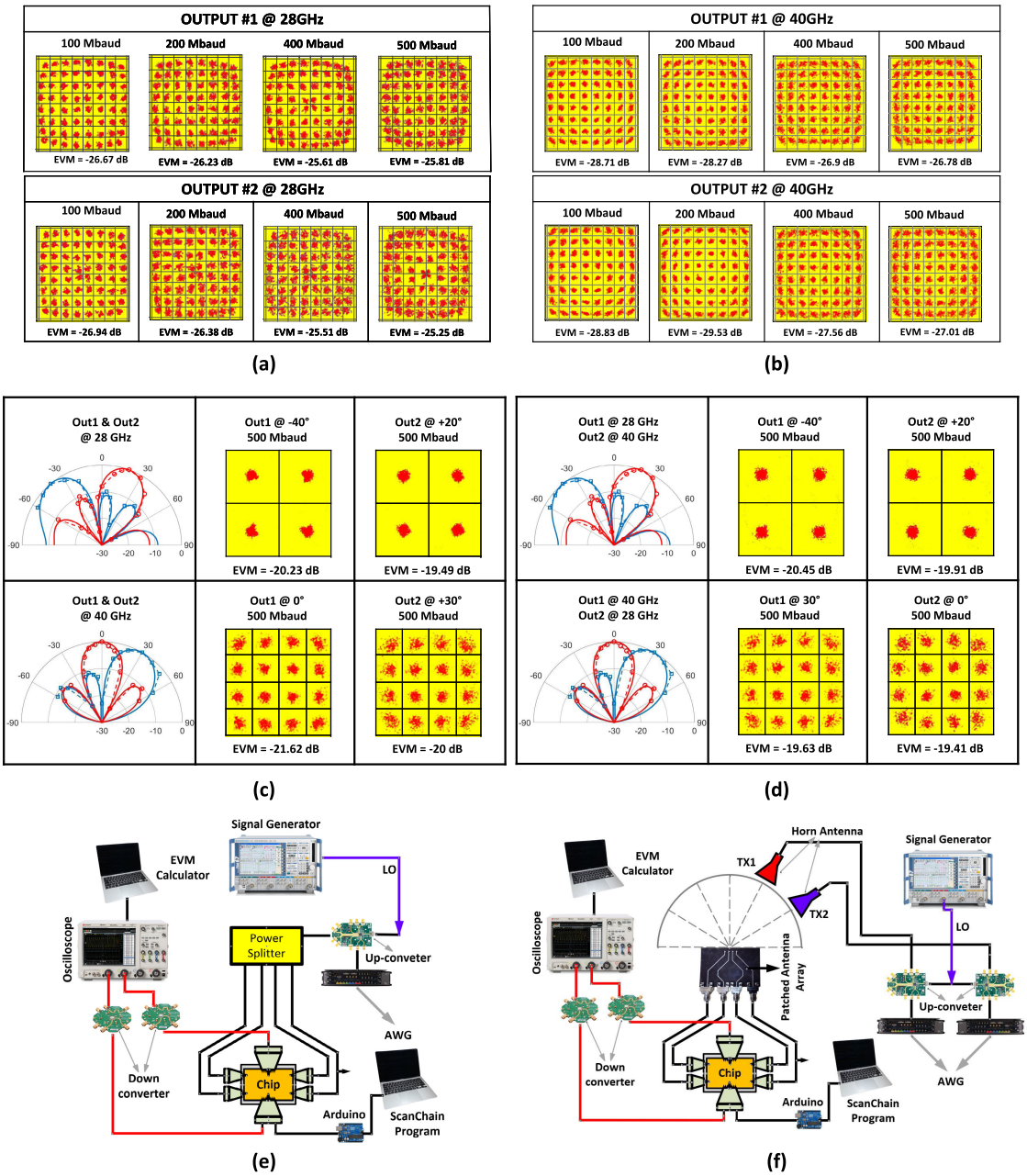

Fig. 20. EVM measurement results and setup. (a) and (b) Measured EVM for wired communication for two output streams at 28 and 40 GHz for 64-QAM and 100, 200, 400, and 500-MBd rates. (c) OTA EVM measurement for dual-beam at the same frequency (28, and 40 GHz) output stream for two modulations, QPSK and 16-QAM. (d) OTA EVM measurement for dual-band dual-beam scenario with QPSK and 16-QAM modulation for 500-MBd symbol rate. (e) EVM measurement setup for wired communication. (f) EVM measurement setup for OTA communication.

(one beam for each band) a dual-band antenna array covering 24–28 and 37–40 GHz is used. Two horn antennas are on the TX side transmitting QPSK and 16QAM with 500-MBd rate signals generated by the AWG at an IF frequency of 3.3 GHz and upconverted by the upconverter board to the desired mm-Wave frequency. The received signal was downconverted by two different downconverter boards each for one output stream and sent to two independent channels of the oscilloscope for EVM calculation using Pathwave, as shown in Fig. 20(f). The results are shown in Fig. 20(c) for 28 and 40 GHz, respectively, and in Fig. 20(d) for concurrent dual-band dual-beam scenario. For the received signal at 28 GHz, the QPSK and 16QAM EVM values are better than −19.49 and −19.41 dB, respectively, while for the received signal at 40 GHz, the QPSK and 16QAM EVM values are better than −19.91 and −19.63 dB, respectively.

In Table II, the proposed mm-Wave concurrent dual-band dual-beam phased array RX front-end is compared with some of the state-of-the-art mm-Wave phased array RXs. As can be seen, single-channel/single-beam specs are comparable. In terms of number of elements, this work and [7], [8], [13], and [23] are suitable for handset applications and [20], [22], and [24] due to the high number of elements, and hence relatively high area and power consumption are proper choice

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART mm-WAVE PHASED ARRAYS RXS FOR 5G

References / Specs	This Work		[20] JSSC'21	[23] JSSC'21	[13] JSSC'18	[8] JSSC'18	[22][d] MTT'23		[7] JSSC'22		[24] MTT'22	[15] JSSC'19
Single-Channel/Single-Beam												
Technology	22nm CMOS FDSOI		40nm CMOS	65nm CMOS	28nm RF-CMOS	65nm CMOS	180nm SiGe BiCMOS		65nm CMOS		180nm BiCMOS	65nm CMOS
Topology	RFBF		DBF	Analog-BF/ FDM	RFBF	HBF	RFBF		HBF		RFBF	HBF
Freq (GHz)	23-30	36-40	28	28	25.8-28	25-30	26-28.5	37-40.5	26.75-29.25	35.62-38.37	15-57	27-29.75 35-38.75
Gain (dB)	20.5	18	21[a]	>16	69[b]	34[b]	26	26	44[b]	37[b]	22	33[b] 26.6[b]
NF_{min} (dB)	6	7	11.8[a]	6	6	7.3	5.5	5.5	7.9	8.8	4.7	5.7 8.5
S11 (dB)	<-9	<-9	-8.5[a]	-	<-8.5	<-8	-	-	-12	-8	<-10	-10 -15
S22 (dB)	<-10	<-10	-	-	<-10	-	-	-	-	-	<-10	-
RMS Phase Error (°)	<6	<5	-	-	-	<6	4.11	4.26	-	-	<5.5	-
RMS Gain Error (dB)	<0.9	<1.1	-	-	-	-	1.27	1.02	-	-	-	-
IP1dB (dBm)	-25	-22	3[a]	-36.9	-68.9	-29	-29	-28	-29	-22	-28	-30 -23
IIP3dB (dBm)	-18[c]	-12[c]	-12.6[a]	-26.9[c]	-59.9	-19[c]	-19[c]	-18[c]	-19[c]	-11[c]	-18[c]	-
Power (mW)	54.8		177	28.1	-	27.5	130	130	98.75		200	52.5
Area (mm^2)	0.62		0.48	0.66	-	0.32	-	-	1.05		0.765	0.46
Phased-Array												
No. of Elements	4		16	4	16	8	32/4X[e]	32/4X[f]	8		64/4X[j]	4
No. of Streams	2		4	4	2	2	1	1	4		1	2
Non-OTA EVM (dB)	-25.81 64QAM 500Mbaud @28GHz	-27 64QAM 500Mbaud @40GHz	-	-	-	-	-	-	-27.9 64QAM 1.5Gb/s @28GHz	-26.3 64QAM 1.5Gb/s @37GHz	-	-
Single-beam/single-band OTA EVM (dB)	-21.62 16QAM 500Mbaud		-18 4QAM 5Ms/s	-27.95 16QAM 100Msps	-33 64QAM LTE 20MHz	-	-31.7[g] 64QAM 100Mbaud	-31.7[g] 64QAM 100Mbaud	-24.8 16QAM 1 Gb/s		-33.68 64QAM 400Mbaud	-
Dual-beam/single-band OTA EVM (dB)	-21.62 16QAM 500Mbaud @40GHz	-20 16QAM 500Mbaud @40GHz	-	-16.55/-16.17 16QAM 100Msps @ 28GHz	-	-	-	-	-24.8 16QAM 1Gb/s @28GHz	-24.3 4QAM 0.5Gb/s @28GHz	-	-
Dual-beam/Dual-band OTA EVM (dB)	-19.41 16QAM 500Mbaud @28GHz	-19.63 16QAM 500Mbaud @40GHz	-	-	-	-	-28.3[g] 64QAM 100Mbaud @28GHz	-29.1[g] 64QAM 100Mbaud @39GHz	-		-	-
Power (mW)	344		2800	450	400	340	520[h]	520[h]	1370		800[h]	310
Area (mm^2)	5		7.73	10.6	7.28	6.16	12.95[i]	-	12.65		12.5[k]	4.5

[a] Simulated result. [b] Full Receiver. [c] Approximated as: ($Gain_{dB}$ – 10) + IP1dB.
[d] This work is in PCB level and the reported RF chips are for two commercial chips; Renesas F5280 and F5390.
[e(f)] Phased-array functionality is achieved at 28 (39) GHz with 8 chips combined in PCB-level, each consisting of an array of 4-elemenets.
[g] TX EVM. [h] Approximated as 4 times of power of one channel for one chip. [i] Including Package for only one chip.
[j] Phased-array functionality is achieved with 4 chips combined in PCB-level, each consisting of an array of 16-elements.
[k] Only one chip is considered.

for base stations or sat-com applications. In terms of number of streams, this work and [7] are concurrent dual-band and dual-beam. Although [8], [20], and [23] operate as multibeam arrays, they only work at a single band (28 GHz). The reported non-OTA EVM in this work and [7] have similar results although [7] has higher data rate. Alhamed et al. [24] showed the best single-beam/single-band OTA EVM measurement, due to the high number of elements (64) and lower data rate (400 MBd). Mondal et al. [7] report the best dual-beam dual-band OTA EVM but the second beam uses 4-QAM modulation while in this work 16-QAM modulation is used for both the beams. Both this work and the work in [22] report OTA EVM for dual-band dual-beam array operation. The main difference is that in this work, this functionality is achieved using an integrated solution while in [22] each beam is generated using a dedicated commercial chip one at 28 GHz and the other one at 39 GHz.

VI. CONCLUSION

A concurrent dual-band dual-beam phased array RX front-end with FC four inputs and two output streams is introduced using the 22-nm FDSOI process. It covers the 23–30- and 36–40-GHz 5G bands achieving low NF, low power consumption, low rms phase error, low rms gain error,

beam-steering, mid-band rejection, and wideband matching. This array demonstrates the concurrent functionality, null tuning, and CA during measurements.

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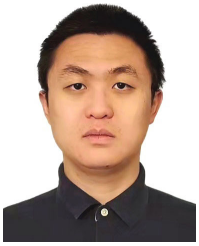

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