

A Novel Physics-Assisted Genetic Algorithm for Decoupling Capacitor Optimization

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Abstract—This article proposes a new physics-assisted genetic algorithm (PAGA) for decoupling capacitor (decap) optimization in power distribution networks (PDNs), which is a highly efficient approach to minimizing the number of decaps within an enormous search space. In the proposed PAGA method, the priority of the decap ports is first determined based on their physical loop inductances. Then, an initial solution is quickly obtained by placing decaps sequentially on the port with the highest priority. Subsequently, a GA with prior physical knowledge is developed to find better decap solutions progressively. A port removal scheme that eliminates the low-priority ports and a modified mutation operation that better guides the mutation direction are developed to accelerate the convergence of the GA. The initial solution and the proposed auxiliary schemes can significantly narrow the search space and incorporate physical knowledge into the GA, thus greatly accelerating the convergence process. Several representative state-of-the-art algorithms and commercial tools are thoroughly compared with the proposed PAGA in different application scenarios. This new PAGA demonstrates better performance in efficiently finding high-quality decap solutions and exhibits strong robustness to handle real-world and large-scale problems, which brings decap optimization algorithms to a new benchmark.

Index Terms—Decoupling capacitor (decap) optimization, genetic algorithm (GA), physical knowledge, port priority, power distribution network (PDN).

I. INTRODUCTION

IN MODERN high-speed integrated circuits (ICs), the operating data rate and working current are continuously increasing, and the power supply voltages are constantly decreasing, rendering the power supply noises in power

distribution networks (PDNs) more troublesome [1]. To reduce the noise in the power supply, the PDN impedance needs to be minimized to meet the target impedance over the frequency range of interest. Usually, large amounts of decoupling capacitors (decaps) on a printed circuit board (PCB) surrounding a high-speed IC are demanded to suppress the PDN impedance and satisfy a target impedance. Minimizing the number of decaps while satisfying the target impedance is pursued in the industry to save cost and layout area [2], [3]. However, efficiently seeking the optimal decap solution for PDN design has been a longstanding challenge due to the huge search space caused by different combinations of decap locations and decap types.

Various approaches have been proposed to determine the optimal selection of decaps. Metaheuristic searching algorithms such as genetic algorithm (GA) [4], [5], [6], [7], [8], [9] and particle swarm optimization (PSO) [10] have been proposed for decap optimization and demonstrate good performance in finding solutions with the minimum number of decaps. Recently, with the popularization of artificial intelligence, machine learning (ML)-based methods, such as reinforcement learning (RL) [11], [12], [13], [14], have been broadly adopted in power integrity (PI) optimization problems. In addition, some algorithms based on human experience and knowledge have also been proposed to quickly determine the decap distribution, such as the Newton–Hessian minimization method [15] and several other approaches [16], [17], [18], [19], [20] with different empirical knowledge and decision-making rules.

However, decap optimization is a combinatorial optimization problem with a large search space. In addition, different decap locations are not independent, and the collaborative contribution of different decaps should be considered, making it impossible to optimize each decap individually [14]. Therefore, it is a great challenge to efficiently find the optimal decap solution and well-balance solution quality (i.e., minimizing the number of decaps in this article) and optimization efficiency in the huge search space. The conventional metaheuristic algorithms [4], [5], [6], [7], [8], [9], [10] can find an optimal decap combination, but the consumed computation time is extremely long, especially when they are applied in large-scale optimization problems with a large number of decap types and locations. The RL-based methods [11], [12], [13], [14] require a significant amount of time for data generation and model training, and the robustness and generalization performance of

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the RL models are difficult to ensure. The human-knowledge-inspired methods [15], [16], [17], [18], [19], [20] can find feasible decap solutions, but the solution quality cannot be guaranteed for large-scale scenarios. In addition, some methods mentioned above [13], [20] can only optimize either the selection of decap types or the decap locations, but not simultaneously. Moreover, most of these methods assume that all decap types can be placed at each candidate location; however, in real designs, there are usually different constraints on decap sizes at different decap locations. Therefore, an algorithm that can be applied in various real-world scenarios with high optimization quality and efficiency is urgently needed.

This article presents a novel and powerful physics-assisted GA (PAGA) that can quickly determine the optimal decap placement solutions for different real-world decap optimization problems. The novel PAGA innovatively combines a GA with prior physical knowledge, thus significantly narrowing the search space and accelerating the convergence speed without missing the optimal decap solution. The prior physical knowledge refers to the priority of different decap ports determined by their physical loop inductances. Based on the port priority, an initial solution is obtained by placing decaps sequentially on the prioritized locations. Further, a hybrid GA integrated with the prior physical knowledge is developed to efficiently find better solutions with fewer decaps based on the initial solution. The proposed PAGA shows a noticeable advantage in finding high-quality solutions with high time efficiency compared to other methods in various application scenarios. The proposed method can also consider the package size constraint of each decap location and support arbitrarily shaped target impedances. The proposed PAGA method has strong robustness and high reliability and solves the longstanding contradiction between solution quality and optimization speed in large-scale decap optimization problems.

The rest of this article is organized as follows. The decap optimization problem is clarified, and some conventional decap optimization algorithms are briefly introduced in Section II. The details of the proposed PAGA are elaborated in Section III. The proposed method is validated and compared with other approaches and commercial tools through several application cases in Section IV. Finally, a conclusion is presented in Section V.

II. PROBLEM DESCRIPTION

In this section, the decap optimization problem in this article is first defined. Then, some conventional decap optimization methods as well as their advantages and limitations are briefly summarized.

A. Problem Definition of Decap Optimization

Decap optimization can be regarded as a combinatorial optimization problem that involves two sets of discrete variables. One set of variables is N available decap locations denoted as $L_1, L_2, \dots, L_N$, and the other is M decap types represented by $D_1, D_2, \dots, D_M$. In the proposed GA method, the two sets of variables are coded together into a 1-D integer array $V_1, V_2, \dots, V_N$. As shown in Fig. 1, the indexes of array elements refer to the decap locations, and the values of the

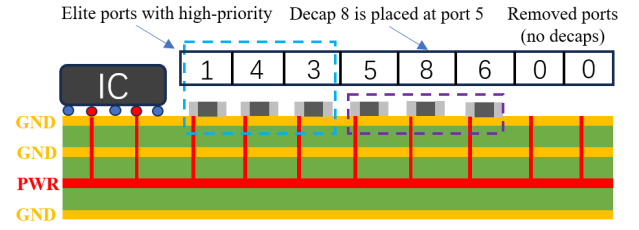


Fig. 1. Example of variable encoding in the GA models. Ports are arranged in a descending order of priority.

elements represent the decap types. The meaning of elite ports and eliminated ports will be introduced later in Section III. Considering that there can be no decaps placed at some locations, the values of the array variables $V_1, V_2, \dots, V_N$ can vary from 0 to M , where 0 means no decap and numbers $1 - M$ represent decap types. The total number of possible cases for this problem is $(M + 1)^N$, which is a huge number and makes it impractical to perform a full search, especially when the number of decap locations and the number of decap types become considerable.

In this article, similar to some previous approaches [7], [8], [9], [14], [15], [16], [20], the primary purpose of decap optimization is to minimize the number of decaps while ensuring that the PDN impedance satisfies a given target impedance to save layout area and cost. Thus, the decap optimization is summarized as a minimization problem with the objective function expressed as

$$\begin{aligned} \arg \min_{V_1, V_2, \dots, V_N} N_{\text{decap}} \\ \text{s.t. } Z_{\text{pdn}}(f) \leq Z_{\text{target}}(f) \end{aligned} \quad (1)$$

where N_{decap} represents the number of used decaps, namely, the nonzero element in the array $V_1, V_2, \dots, V_N$. Full-wave simulations or some fast numerical algorithms [21], [22], [23] can be adopted to obtain the Z -parameter matrix of a PDN, where the ports of the Z -parameter are defined at the IC observation port and the decap locations. Then, the PDN impedance after placing decaps can be calculated using the Z -parameter matrix by a segmentation method [24] as

$$Z'_{aa} = Z_{aa} - Z_{ap}(Z_{pp} + Z_{dd})^{-1}Z_{pa} \quad (2)$$

where p is the port indexes that are connected to the decaps, a is the remaining port indexes without decap connection, and Z_{dd} is the impedance matrix of the decaps being connected. This decap connection operation is the most time-consuming part and must be performed repeatedly during the decap optimization.

B. Conventional Optimization Methods

As mentioned in Section I, numerous approaches have been proposed for decap optimization. In this article, some representative state-of-the-art algorithms are reproduced and compared with the proposed PAGA method. For a fair comparison, some of these methods are slightly modified with their core concepts maintained. These methods are briefly reviewed and summarized as follows.

1) *Sequential Search Method* [6]: This method selects decaps sequentially, and a GA is adopted to determine the

location and type of each newly added decap. This method can significantly improve the optimization speed but sacrifices the solution quality [14]. Here, we replace the GA with a full search to determine the location and type for each newly added decap. Thus, the core concept of this method is retained, and the solution quality of the full search will be better than or at least the same as the GA. This reproduced method is called the “sequential search method” in the remainder of this article.

2) *Sorting Search Algorithm [16]*: In this algorithm, the relative importance of the decap ports is first determined based on their loop inductances, and this concept is also adopted in the proposed PAGA of this article, which will be explained in Section III. Based on the relative importance of the decap locations and the equivalent series inductances (ESL) of different decap types, a complex decision-making procedure is proposed to add decaps sequentially to the candidate locations. This method is called the “sorting search method” in the remainder of this article.

3) *Newton–Hessian Method [15]*: The Newton–Hessian method optimizes the decap locations as continuous variables. In this method, the decaps are also added sequentially. During each iteration, the decap type with the resonance frequency closest to the frequency of the maximum impedance is first selected. Subsequently, the Newton–Hessian minimization method is applied to optimize the decap location to minimize the maximum PDN impedance. This method needs a closed-form expression of PDN impedance for location optimization and only supports constant target impedances, so the application scenario is greatly limited. To compare this method with the proposed PAGA, we assume the decap locations are discrete and traverse all locations instead of using the Newton–Hessian minimization method during each iteration.

4) *GA Methods*: The method proposed in [7] uses a GA to optimize the power supply-induced jitter and the PDN impedance. Here, the optimization target of this GA method is modified to be the same as the proposed PAGA as expressed by (1) for a fair comparison. A modified GA [8] has been recently proposed that performs better in finding the optimal decap solution than the conventional GA [7]. A size variation control scheme is presented to narrow the search space and improve optimization efficiency. Another GA method [9] has been proposed and performs better than the modified GA [8] in efficiently finding high-quality decap solutions.

These GA methods are expected to find the optimal solution as long as enough searching time is given. However, as mentioned earlier, the total search space of the decap optimization problem is enormous, and the PDN impedance evaluation is time-consuming, which means the GA methods [7], [8], [9] may need an unbearably long time to find the optimal solution. None of the GA methods in [7], [8], and [9] have exhibited enough scalability when facing large-scale decap optimization scenarios. Thus, a new approach that can effectively improve the optimization speed without missing the optimal solution for large-scale decap optimization problems is urgently demanded.

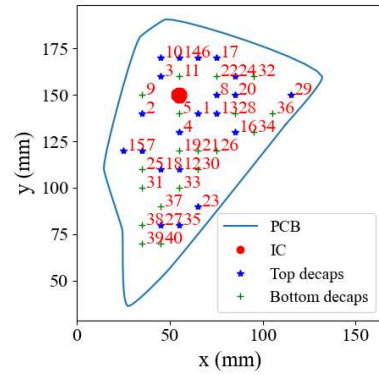


Fig. 2. Example of port priority distribution for a four-layer board with 40 decap ports. The port with the highest priority is annotated as 1. The stackup of this board from the top to bottom layer is GND, PWR, GND, and GND. The thickness of the dielectric layers is 0.2, 0.3, and 0.2 mm.

III. PROPOSED METHOD

In this section, several critical steps of the proposed decap optimization method are elaborated, which include calculating the port priority of the decap locations, determining the initial solution, and finding the optimal decap solution using the proposed PAGA.

A. Port Prioritization Based on Physical Inductance

Different decap locations have varying effects on suppressing the PDN impedance due to their respective loop inductances. According to physical understanding, decap locations that provide current return paths with smaller loop inductances are usually more effective. Therefore, the method proposed in [12] and [16] is adopted to quantitatively evaluate the priority of each decap location.

Fig. 2 gives an example of the port prioritization result of a PDN board with 40 decap ports. It shows that the locations with smaller loop inductances are more likely to have higher priorities. Thus, the prioritization result is consistent with our physical understanding. As the decap optimization problem focuses on a relatively low-frequency range, the inductances of each port can be considered frequency-independent. Therefore, we choose one representative frequency to perform the port prioritization rather than the entire frequency range of interest, significantly improving the prioritization efficiency.

B. Initial Solution Determination

After evaluating the priority of all decap ports, the second strategy proposed is to determine a feasible initial solution by iteratively connecting decaps to the unused port with the highest priority. In each decap connection, the best decap type that can minimize the area of the target impedance violation is selected. Hence, by selecting and adding decaps to the prioritized locations sequentially until the target impedance is satisfied, an initial solution can be efficiently obtained.

In real decap optimization applications, decap ports can be predesigned to allow only a specific package size or decap type. This package size constraint makes it difficult to strictly follow the method of initial solution determination mentioned above. To solve this problem, a concept of subpriority for each decap type is proposed. Namely, for each decap type,

Algorithm 1 Initial Solution Determination

Var: $L_1, L_2, \dots, L_N$: corresponding to prioritized (high to low) decap locations based on inductances;
 $D_1, D_2, \dots, D_M$: represent different decap types;
 $V_1, V_2, \dots, V_N$: decap solution, initialized to 0;
Input: $Z_{\text{target}}(f)$: target impedance, f is frequency;
for $i \in \{1, 2, \dots, M\}$ **do**:
 Find sub-priority of the locations for decap type D_i using one single frequency;
for $i \in \{1, 2, \dots, N\}$ **do**:
 for $j \in \{1, 2, \dots, M\}$ **do**:
 Connect decap type D_j to its best empty location with the highest sub-priority respectively;
 end for
 Find the best decap type D_j minimizing $\sum_f \max[Z_{\text{pdn}}(f) - Z_{\text{target}}(f), 0]$;
 Choose the best location L_k of decap D_j ;
 Connect the best D_j to location L_k ($V_k = D_j$);
 if $\forall f : Z_{\text{pdn}}(f) \leq Z_{\text{target}}(f)$:
 break;
 end if
end for
Obtain the initial solution $V_1, V_2, \dots, V_N$.

the subpriorities of the locations that allow this decap type are calculated using the approach proposed in [12]. When all the decap types are allowed at each location, the subpriority lists for different decap types will be identical to the global priority without considering package size constraints.

Using the calculated subpriority, an initial solution can be quickly determined using Algorithm 1. The core concept of Algorithm 1 is as follows. Each decap type is connected to the port with the highest corresponding subpriority; hence, all the decap types are, respectively, visited, and the decap type that minimizes the area where the PDN impedance violates the target impedance is selected and connected to its best empty port with the highest subpriority; finally, a feasible initial solution can be determined by adding decaps iteratively until the target impedance is satisfied.

According to the method presented in [16], the port priority is not affected by the decap type connected to it, which means that the port prioritization calculation only needs to be performed once. In addition, this method requires MN times of PDN impedance evaluations at most to find the initial solution after extracting the port priority or subpriority. Therefore, the time efficiency of this algorithm is greatly guaranteed. Even though this method may not find the optimal solution, it provides a feasible starting point toward the optimal solution and significantly narrows the search space, which can remarkably accelerate the convergence process of the proposed GA.

C. Proposed PAGA

Once a feasible initial solution is determined using Algorithm 1, it can be continuously improved toward the optimal solution. GA can be used to improve solution quality and has recently become popular in decap optimization problems

[25], [26]. However, the conventional GA algorithms may need an extremely long time to find a satisfactory solution. Thus, some acceleration strategies are crucial to make the GA more practical and valuable.

A size variation control scheme that limits the number of used decaps in each population was proposed to accelerate the convergence process in a modified GA [8]. This scheme has been proven effective in accelerating the convergence process and is adopted in this article's proposed method.

In each iteration, the objective function of each population to be minimized is calculated as

$$f_{\text{obj}} = \begin{cases} -N_d, & \text{if } \forall f : Z_{\text{pdn}}(f) \leq Z_{\text{target}}(f) \\ \max[Z_{\text{pdn}}(f) - Z_{\text{target}}(f), 0] & \text{if } \exists f : Z_{\text{pdn}}(f) > Z_{\text{target}}(f) \end{cases} \quad (3)$$

where N_d refers to the number of unused decap ports. When the target impedance can be satisfied, the optimization objective is to minimize the number of decaps being used. However, it is also possible that the no decap solution can be found to satisfy the target impedance. Under this circumstance, the optimization objective is to minimize the target impedance violation.

To further facilitate the convergence of the GA, a PAGA with a port removal scheme and a modified mutation operation is proposed to narrow the search space and incorporate more physical knowledge into the GA. The number of decaps used in the current best solution is also recorded, and all the unused ports with lower priority are removed from the search space. The corresponding variables of the removed ports in all the populations are set to zero. At the same time, the corresponding rows and columns of the unused ports are also removed from the PDN Z-parameter matrix, which can accelerate the mathematical operation of the decap connection in (2).

Further, a modified mutation operation is proposed to better guide the mutation direction. During the mutation operation, variables corresponding to the removed ports remain zero without participating in the mutation. For the unremoved ports, a certain proportion of them with higher priority are defined as the elite ports and will never be mutated to zero, as illustrated in Fig. 1. A small elite port proportion will encourage the GA to explore the search space more extensively, and a large proportion will help fine-tune the current best solution. For this article, the elite port proportion is set as 0.5. The other unremoved ports will be mutated randomly to pursue a better solution with fewer decaps.

The proposed port removal scheme and modified mutation operation are reasonable since better solutions can be more easily found among the locations with higher priorities due to smaller physical inductances. The detailed process of the proposed PAGA is elaborated in the pseudocode of Algorithm 2.

The proposed port removal scheme and modified mutation operation accelerate the convergence process mainly in three aspects. First, the search space is significantly narrowed. After port removal, the total search space will be reduced from $(M+1)^N$ to $(M+1)^{N-E}$, where E is the number of eliminated ports. Second, it incorporates the physical knowledge of the relative port importance into the GA and better

Algorithm 2 Proposed PAGA

Var: $V_1, V_2, \dots, V_N$: variables corresponding to the decap locations and decap types;
 N_d : no. of nonzero elements in variables $V_1 \sim V_N$;
Input: Z_{pdn} : Z-parameter matrix of PDN;
 $V'_1, V'_2, \dots, V'_N$: initial sol. using Algorithm 1;
 $Z_{\text{target}}(f)$: target impedance, f is frequency;
 N_g : no. of generations;
 N_p : population size;
 V : size variation factor;
Fitness Function f_{obj} : Eqn. (3);
for $i \in \{1, \dots, N_g\}$ **do**:
 if $i = 1$ **do**:
 Assign initial solution $V'_1 \sim V'_N$ to first population;
 Randomly generate $N_p - 1$ populations;
 end if
 // Port removal
 Count the number of used decaps D in best solution;
 for $j \in \{1, \dots, N_p\}$ **do**:
 Set $N - D$ variables with lower sub priority to 0;
 end for
 Update Z_{pdn} with unremoved ports;
 Selection;
 Crossover;
 Modified Mutation (only for unremoved ports);
 for $j \in \{1, \dots, N_p\}$ **do**:
 do: **if** $N_d < D - V$ or $N_d > D$ **for** j^{th} population **do**:
 Perform the size variation control scheme;
 end if
 end for
 Compute f_{obj} according to Eqn. (3);
 Sort populations according to f_{obj} ;
end for
Obtain the final solution $V_1, V_2, \dots, V_N$.

TABLE I
DECAP LIBRARY

Model #	C (uF)	ESL (nH)	ESR (mΩ)	Package
1	0.1	0.30	20.4	0402
2	0.47	0.28	24.4	0402
3	1	0.17	15.1	0402
4	1	0.52	8.6	0603
5	2.2	0.35	8.7	0603
6	4.7	0.40	6.1	0603
7	4.7	0.34	5.9	0805
8	10	0.58	3.8	0805
9	22	0.51	3.5	0805
10	47	0.73	2.8	0805
11	47	0.96	2.8	1206
12	100	0.58	2.8	1206
13	220	1.0	1.9	1206

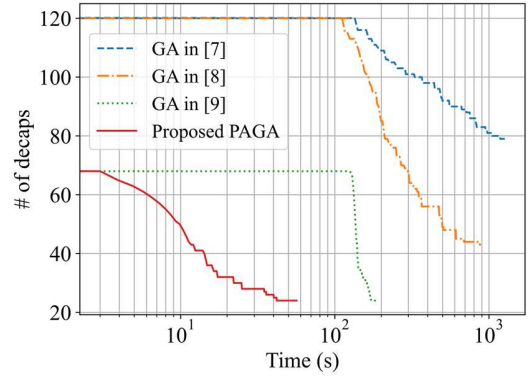


Fig. 3. Comparison of the overall performance between different GA methods and proposed PAGA for Case 1.

guides the mutation direction. Third, as mentioned earlier, the most time-consuming part of decap optimization is the PDN impedance evaluation when connecting decaps. It can be shown from (2) that the computational complexity of the Z-matrix algebraic operation for the decap connection positively correlates with the number of ports. When some ports are removed, the time used for the impedance evaluation will be decreased. As the number of decaps is iteratively and progressively reduced in the decap optimization process, the saved computation time for the decap connection will gradually become considerable compared to the modified GA [8] without matrix size reduction.

IV. METHOD VALIDATION

In this section, the performance and robustness of the proposed PAGA approach are validated. Some representative state-of-the-art algorithms and commercial tools, including Ansys SIwave [27] and Cadence OptimizePI (OPI) [28], are thoroughly compared with the proposed method. These two commercial tools are separately compared with other approaches in different scenarios. In each scenario, the Z-parameter matrix is exported from the corresponding

tool (SIwave [27], OPI [28], or the boundary integration method [21]) and used for decap optimization in other methods. The used decaps library is listed in Table I. All the optimizations are performed on a personal computer with an Intel i9 CPU.

A. Case 1: Randomly Generated Board

A four-layer PDN board with 120 ports generated by the method proposed in [21] is used to validate the proposed optimization method. The stack-up of this board is the same as the example in Fig. 2, and the voltage regulator module (VRM) is modeled as an R - L circuit with R equal to 3 mΩ and L equal to 2.2 nH. The target impedance is a constant value of 0.5 mΩ over the frequency range from 200 kHz to 1 MHz. The overall performance of the proposed PAGA is compared with other methods regarding solution quality and time efficiency. In all the GA algorithms, including the GAs in [7], [8], and [9], and the proposed PAGA, all the hyperparameters are the same as follows: the population size N_p is set to 50, the size variation factor is set to 2, the mutation probability is set to 0.1, the cross probability is set to 0.5, and the elite port ratio (the ratio of the number of elite ports to the total number of nonempty ports) is set to 0.5.

The convergence process of the proposed PAGA and other GA methods is compared in Fig. 3. The flat region at the beginning of the proposed PAGA and the GA in [9] stands for the time used for port prioritization and initial solution determination. The flat region at the beginning of other GA

TABLE II
OPTIMIZATION RESULT COMPARISON—CASE 1

Methods	Time (s)	Decaps Number
GA in [7]	1266	79
GA in [8]	887	43
GA in [9]	187	24
Sequential search method [6]	\	61
Sorting search method [16]	\	No Sol.
Newton-Hessian method [15]	\	101
Proposed PAGA	61	24

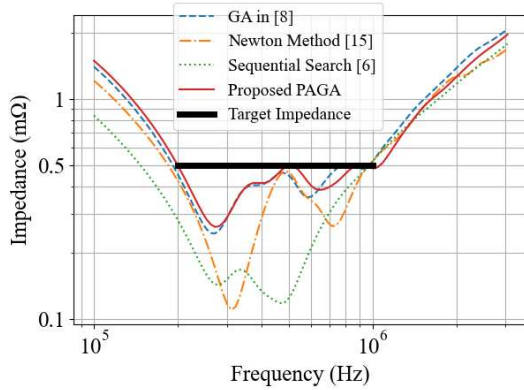


Fig. 4. Optimized impedance curves of the final solutions by different methods for Case 1. The Newton-Hessian method is called the “Newton method” for simplicity.

methods stands for the consumed time to find a feasible solution. All the GAs are iterated 300 times, and the number of decaps in the final solution of the four approaches is 79, 43, 24, and 24, respectively. It can be found that the initial solution saves lots of time and makes a critical contribution to the fast convergence of GA. After a feasible solution is found, the proposed PAGA can quickly converge to a much better solution with 24 decaps, while the GAs in [7] and [8] take a much longer time and still miss the optimal solution. It is shown that the convergence speed and solution quality of the proposed PAGA are remarkable and overwhelming compared with other GA methods.

Besides comparing the proposed method with different GA approaches, we also compare it with several other algorithms. The consumed time and the number of decaps of different methods are listed in Table II. As mentioned earlier, the sequential search [6] and Newton-Hessian [15] methods cannot find the optimal solution because they optimize different decaps individually rather than collaboratively. The sorting search method [16] cannot find a feasible solution even after a long search. It should be pointed out that we have only reproduced the core concepts of these three methods. The time consumption may be affected by various factors in the algorithm implementation. Thus, the time consumption of the three methods [6], [15], [16] is not compared in Table II. Nevertheless, the comparison in Table II shows that the solution quality of the proposed method is the highest, while a high time efficiency is also guaranteed.

The optimized PDN impedance results of different methods are plotted in Fig. 4. It is shown that the solutions found by the sequential search [6] and Newton-Hessian [15] methods

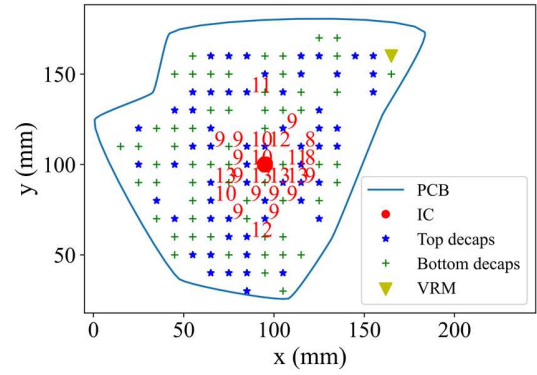


Fig. 5. Decap solution distribution of the proposed method for Case 1. The annotations stand for the decap types in the decaps library.

have a severe over-design problem. Too many decaps with large capacitance values are used in these solutions, which is unnecessary to satisfy the target impedance. In addition, the decap solution distribution of the proposed PAGA is shown in Fig. 5. The 24 decaps are placed on 24 ports with the highest priorities near the IC, which agrees well with our engineering experience. The results show that the proposed PAGA can find a high-quality solution in an extremely short time, thus well-balancing solution quality and time consumption.

B. Case 2: Two Real-Product Applications

To compare the proposed PAGA with the commercial tools, two PCBs in practical industry applications are adopted. The first board has 16 layers in total with a size of approximately 160 × 100 mm. There are 123 candidate board-level decap locations in total. Due to product confidentiality concerns, more details of the PCB are not shown. Decap optimization can be performed after the Z-parameter matrix defined at the IC port and decap ports is simulated and exported. This can also be extended to handle package-level decap optimization problems. We first compare the performance of the proposed PAGA with the Ansys SIwave tool. We optimize the PDN impedance to meet a piecewise target impedance. The first segment of the target impedance is set to 5 mΩ from 1 to 3.5 MHz, and the second segment is set to 11 mΩ from 3.5 to 10 MHz. All the parameters of the GA methods are set to be the same, and the maximum number of iterations is 100.

The optimization results of different approaches are listed in the upper part of Table III, and the impedance results are compared in Fig. 6. It can be found that the solution provided by the Ansys SIwave tool also has an over-design problem. In addition, the SIwave tool performs a parallel computation with a 24-core CPU, while the other methods are implemented without parallel computation. Even so, the proposed method still finds the final solution faster than the SIwave tool, and the solution quality of the proposed method is also much better.

It is worth mentioning that when we lower the second segment of the target impedance to 10 mΩ, the SIwave tool fails to find a feasible solution within 100 iterations, while the proposed method can still rapidly find a solution with 14 decaps. This indicates that the proposed method has stronger robustness than the algorithm used in the SIwave tool.

The second board has 12 layers in total with a size of approximately 160 × 30 mm, and there are 68 candidate

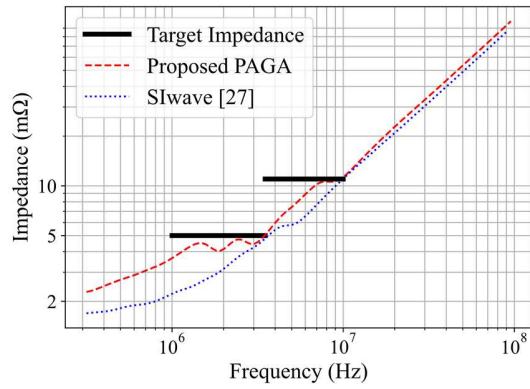


Fig. 6. Optimized impedance curves by the final solution of SIwave and proposed method for the first board of Case 2.

TABLE III
TIME AND DECAP NUMBER COMPARISON—CASE 2

Boards	Methods	Time (s)	Decaps Number
1 st Board	GA in [7]	595	78
	GA in [8]	441	32
	GA in [9]	140	10
	SIwave tool [27]	57	34
	Proposed PAGA	18	10
2 nd Board	GA in [7]	188	37
	GA in [8]	161	32
	GA in [9]	55	29
	OPI tool [28]	52	34
	Proposed PAGA	31	29

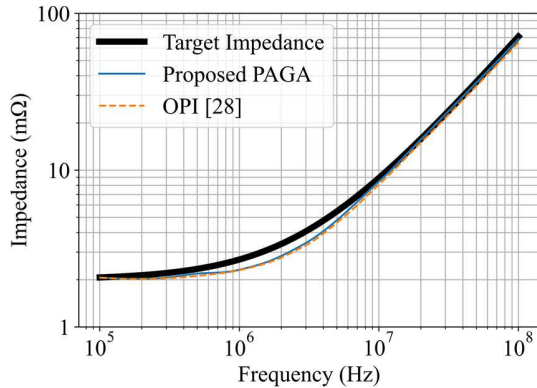


Fig. 7. Optimized impedance curves by the final solution of OPI and proposed method for the second board of Case 2.

board-level decap locations. The optimization target of this PDN board is an R - L -type target impedance, which means that the optimization target is an impedance curve equivalent to the series connection of a resistor and an inductor. The R -value is set to 2 mΩ, and the L value is set to 0.11 nH. Here, we compare the performance of the proposed PAGA with the OPI tool [28].

The optimization results of different methods are listed in the lower part of Table III, and the impedance curves are plotted in Fig. 7. Similar to the SIwave tool, the OPI tool also performs a parallel computation with a 24-core CPU. It can be found that the proposed method can find a solution with an impedance curve similar to that of the OPI tool. However, it has a notable advantage in decap number and time consumption. The optimization results of these two real

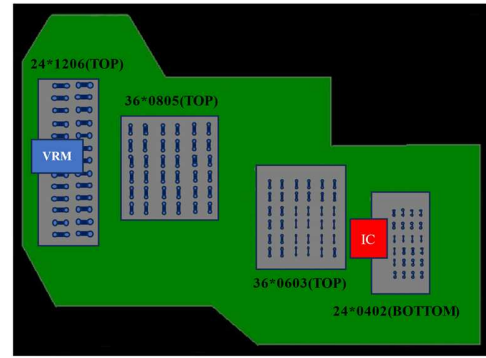


Fig. 8. Arbitrary-shaped PDN board model with size constraints for Case 3.

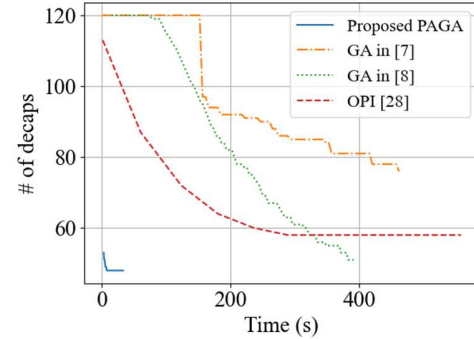


Fig. 9. Comparison of convergence process between different methods for Case 3.

production applications show that the proposed PAGA exhibits a noticeable advantage regarding the optimization efficiency and solution quality compared to the other GAs in [7], [8], and [9], and commercial tools [27], [28].

C. Case 3: With Package Size Constraints

In this case, the layout of the PCB and the decap ports have been predesigned, which means each decap port has a constraint on the decap package size. We assume that each decap port only allows the placement of a decap with the same package size compared to the original port design. A PCB layout that contains 120 decap locations with different package sizes is shown in Fig. 8. The decap ports are grouped according to their package sizes. The decap ports with the 0402 package are on the bottom layer under the target IC, and the other ports are on the top layer. Other unused areas are reserved for traces and other components. The VRM is modeled as an R - L circuit with R equal to 0.3 mΩ and L equal to 1 nH.

In the proposed PAGA, the global priorities of the decap ports are first determined using the approach proposed in [16]. For each package size, the subpriorities of all the corresponding ports of this package size are defined by maintaining the same order as the global priority. Then, an initial solution is rapidly determined by Algorithm 1 and continuously improved toward the optimal solution by Algorithm 2. During each iteration, those unused ports with lower subpriorities will be removed according to the proposed port removal scheme in Algorithm 2.

The convergence of decap optimization is shown in Fig. 9, and the optimized PDN impedance curves by different methods are shown in Fig. 10. The target R is set to 1.2 mΩ, and the target L is set to 0.08 nH. Since other methods [6],

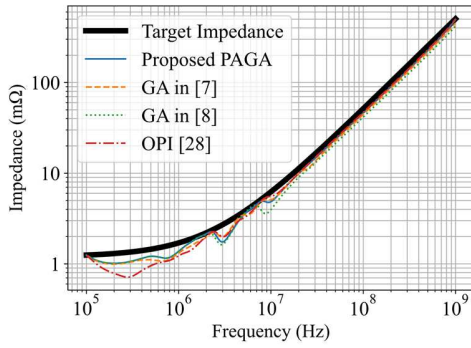


Fig. 10. Optimized impedance curves by the final solution of different methods for Case 3.

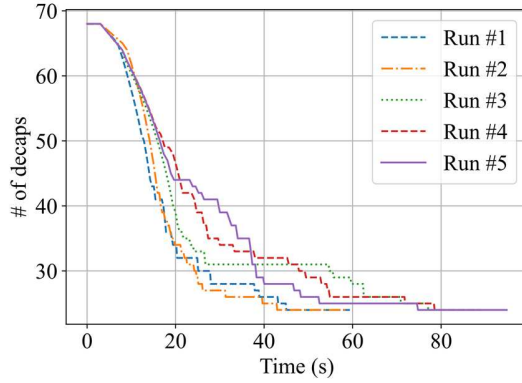


Fig. 11. Convergence process of the proposed method for five independent runs. The PDN board is the same as the board in Case 1. The flatten region at the beginning stands for the time consumed in initial solution determination.

[9], [15], [16] cannot deal with the scenarios with decap size constraints and the SIwave tool does not support R - L -type target impedances, here, we focus on the comparison with the OPI tool [28] and the GA methods [7], [8]. The Z-parameter matrix used in this example is also extracted using the OPI tool. The optimization result shows that the OPI tool takes approximately 600 s to find a solution with 58 decaps within 500 iterations, while the proposed PAGA converges to a solution with 48 decaps within less than 100 s. The final solution of the proposed PAGA includes six decaps with a 0402 package, nine decaps with 0603 package, ten decaps with 0805 package, and 23 decaps with 1206 package, while the OPI tool uses 12, 13, 10, and 23, respectively. The optimized impedance curves also indicate that the OPI tool has an over-design problem. Therefore, the validation result of this case demonstrates that the proposed PAGA can also tackle the decap optimization scenarios with decap size constraints and has a noticeably better performance than the OPI tool and other GA methods [7], [8].

D. Robustness Validation

In this section, the robustness of the proposed method is validated in two aspects: repeatability and scalability. First, the repeatability of the proposed method is validated by conducting five independent runs on the optimization of the PDN board of Case 1. As shown in Fig. 11, all five runs converge to a solution with 24 decaps within 80 s, which demonstrates the high repeatability of the proposed method. Additionally, the repeatability of different GA methods is also compared and

TABLE IV
REPEATABILITY COMPARISON OF DIFFERENT METHODS FOR CASE 1:
TIME (S)—DECAP NUMBER

	Run #1	Run #2	Run #3	Run #4	Run #5
Proposed PAGA	61 - 24	57 - 24	79 - 24	84 - 24	94 - 24
GA in [7]	1266 - 78	1288 - 81	1377 - 85	1337 - 83	1291 - 80
GA in [8]	887 - 43	925 - 45	994 - 48	974 - 46	911 - 44
GA in [9]	187 - 24	191 - 24	202 - 24	195 - 24	205 - 24
Newton method [15]	/-101				
Sequential search [6]	/-61				

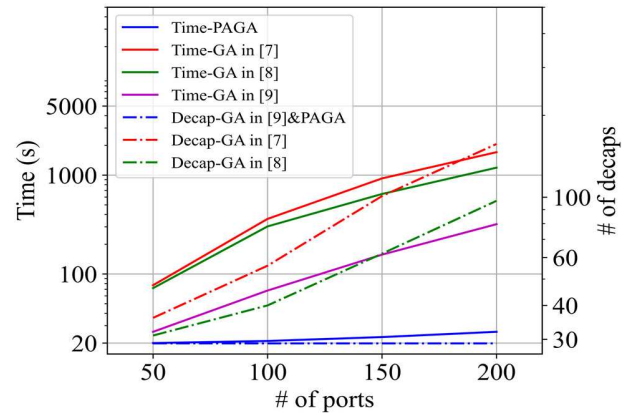


Fig. 12. Time consumption and solution quality of different GA methods for Case 3 as the number of decap ports increases.

listed in Table IV. The sequential search [6] and Newton-Hessian [15] methods are performed only once since they will give a deterministic result without randomness. The result shows that the proposed PAGA has excellent repeatability and stability in converging to a high-quality decap solution (the best solution among all the existing approaches). The exceptional repeatability of the proposed PAGA is achieved by three main reasons. First, the determined initial solution using Algorithm 1 provides a reasonable starting point. Second, the port removal scheme significantly narrows the search space. Third, the modified mutation operation (i.e., the elite port scheme) can better guide the optimization toward the optimum solution.

Moreover, the scalability of the proposed PAGA when dealing with large-scale problems is also validated. When the total number of decap ports becomes enormous, the total search space will increase exponentially. Fortunately, the time demanded by the proposed PAGA will not increase severely due to the several proposed techniques, including the initial solution determination, the port removal scheme, and the modified mutation operation. Fig. 12 demonstrates the trend of time consumption and decap solution as the number of ports increases. The result shows that the proposed PAGA can maintain high time efficiency in large-scale problems while the efficiency of other GA methods degrades significantly. Namely, the proposed PAGA exhibits exceptional scalability.

V. CONCLUSION

This article proposes a powerful PAGA for high-speed and high-quality decap optimization, which has a noticeable advantage over other state-of-the-art approaches and commercial tools. Some auxiliary schemes that narrow the search space and incorporate physical knowledge into the GA are proposed to accelerate the convergence process significantly. Various application scenarios with different-shaped target impedance and decap size constraints validate the effectiveness of the proposed approach. Strong robustness, high time efficiency, and high solution quality can be simultaneously achieved by the proposed PAGA for large-scale PDN problems. The proposed PAGA paves a novel path and builds a new benchmark for decap optimization given the simulated Z -parameters (or S -parameters) of a PDN structure.

The proposed method can be extended to other PDN decap optimization scenarios, such as package-level decaps or 3-D heterogeneous ICs [29], [30], as long as the impedance observation port and decap ports are well-defined and the corresponding Z -parameters (or S -parameters) are provided. Also, the proposed PAGA can be applied to other decap optimization scenarios with different objectives, such as minimizing decap cost or area, suppressing transient PDN noise, or reducing power supply-induced jitter [7]. Moreover, optimizing the decap locations as continuous variables for arbitrarily shaped PDN structures will be pursued without requiring Z -parameter (or S -parameter) simulations.

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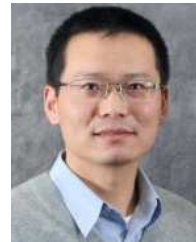


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