Modeling of a Voltage Regulator Module for Power Integrity: Power Supply Induced Jitter

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***Abstract*—This article analyzes different methods for modeling a buck regulator among the variety of voltage regulator modules from the perspective of power integrity and assesses the accuracy of power supply induced jitter (PSIJ) predictions for each buck regulator model. To compare the buck regulator modeling approaches, methods for conventional passive component modeling and behavior modeling are introduced. Four different buck regulator models are compared with measurements in terms of time-domain voltage ripple and nonlinearity. Then, each model is applied to a simulation-based system-level PSIJ prediction setup to quantify the accuracy of the buck regulator models from the perspective of PSIJ. A printed circuit board with an inverter chain powered by an external buck regulator is selected as the device under test. In the presence of power supply fluctuations due to load current injection on the buck regulator, the time interval error of the inverter is measured. The measured peak-to-peak jitter is then reproduced by various simulation setups with the different buck regulator modeling methods. Finally, the PSIJ simulation accuracy is investigated for each buck regulator model.**

***Index Terms*—Nonlinear buck regulator behavior modeling, power distribution network (PDN), power supply induced jitter (PSIJ), voltage regulator module (VRM).**

I. Introduction

As INPUT/OUTPUT (I/O) speeds increase to multigigabit data rates and supply voltages decrease because of power efficiencies, the jitter of I/O buffers has become one of the greatest challenges in today's electronic devices. Specifically, power supply induced jitter (PSIJ) due to fluctuations in the power supply rail has become severe; thus, the prediction of PSIJ is essential. PSIJ prediction requires a knowledge of the design parameters of the power distribution network (PDN), voltage fluctuations in the power supply rail, and the jitter sensitivity of victim integrated circuits (ICs). For the analysis of voltage fluctuations in the power supply rail, each component from the on-chip PDN to the off-chip voltage regulator modules (VRM) is required. Therefore, accurate PSIJ prediction requires not only a VRM simulation model but also jitter characteristics and PDN parameters.

For the modeling of VRMs, the small-signal modeling methods for the various dc–dc converters are widely studied. Among the dc–dc converters, the small-signal boost converter modeling methods based on the voltage and current transfer functions are proposed [1], [2] and extended to include the printed circuit board (PCB) parasitics in [3]. The different types of dc–dc converters, buck–boost, is modeled by considering the parasitic components of the PCB in [4] and [5]. For the buck converters, the behavior modeling method is proposed to replace the simple inductor model [6].

Over the past few decades, buck regulator modeling methods among the variety of VRMs have been widely studied. Commonly used methods for modeling buck regulators include linear passive component models, such as the first-order resistor–inductor (RL) model and the four-element RL model. The current capabilities of buck regulators in current switching and dc drops are characterized by an inductor and resistor, respectively, in the first-order modeling method [7]. However, the first-order RL model cannot isolate low-frequency impedance and damping resistance, resulting in a low time-domain simulation accuracy. To overcome this drawback of the first-order RL model, a four-element RL model has been developed, which uses two different parallel resistor–inductors [8], [9]. Because the four-element RL model utilizes two resistors, the dc resistance and damping behavior at the resonance frequency are successfully isolated. Nevertheless, these modeling methods have limitations in capturing the nonlinear behavior of buck regulators because only passive components are applied.

To overcome these drawbacks, some studies have utilized encrypted buck regulator models provided by manufacturers or have developed accurate simulation models in SIMPLIS [10]. However, the limited flexibility of encrypted models and compatibility issues with SIMPLIS restrict the options for running power integrity (PI) simulations. Therefore, simpler methods for behavior modeling that are compatible with simulation program with IC emphasis (SPICE) simulators have been employed to enhance the nonlinearity and flexibility of buck regulator simulation models.

Manuscript received 19 October 2023; revised 19 February 2024 and 13 May 2024; accepted 12 June 2024. Date of publication 19 June 2024; date of current version 1 July 2024. This work was supported by the National Science Foundation under Grant IIP-1916535. *(Corresponding author: Junho Joo.)*

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Digital Object Identifier 10.1109/TSIPI.2024.3416088

To achieve both compatibility with SPICE models and flexibility of buck regulator models, methods for modeling the behavior of nonlinear multiphase buck regulators have been developed. In [11], a switching-based single-phase buck regulator modeling method is proposed. Specifically, the nonlinear feature of load line regulation, also known as adaptive voltage positioning (AVP), is developed for the simulation of PDN optimization. A continuous time-modeling method for the constant-on-time feature is proposed in [12], while the pulsewidth modulation (PWM) is modeled in [13]. In [14], the PWM-based buck regulator modeling method is extended to multiphase operation as well as the pulse frequency modulation schemes. In the continuous time models, because the switching behaviors of [11] are averaged in time domain, the computing requirements are greatly reduced. These buck regulator behavior modeling methods have been successfully validated by output voltage measurements.

In addition to buck regulator modeling methods, the prediction of timing jitter has also been widely studied. Among the variety of jitter prediction studies, transfer-function-based PSIJ analyses have been extensively performed. In [15], the transfer function of supply voltage fluctuations in jitter at an inverter chain side is studied. Large- and small-signal expressions of transistor switches, depending on the supply voltage fluctuation, are analytically derived and validated with the measured peak-to-peak jitter [17]. In [16], a prediction method is proposed that considers not only the power but also ground voltage fluctuations at a single-ended full-swing buffer I/O. In [18] and [19], the PSIJ sensitivity is characterized based on the power supply rejection ratio (PSRR), as well as transfer function methods. In those works, separate analyses of the PSRR of the voltage regulator and the buffer PSIJ sensitivity are performed. Because the voltage regulator is a linear low-dropout regulator, the PSRR response can be easily calculated. Finally, a system-level PSIJ sensitivity analysis is completed in which the regulator PSRR response is multiplied by the buffer PSIJ sensitivity in the frequency domain. This article has been verified by simulations but is not applicable when the nonlinearities of modern complex buck regulators are applied.

In addition to transfer-function-based prediction methods, the premeasured jitter sensitivity of a victim IC can be applied to the prediction process. In [21] and [22], the numerous different clock schemes for TX-RX circuits are used resulting in various jitter sensitivity functions. Based on the jitter sensitivity in different clock schemes, a comprehensive dynamic noise modeling is presented to analyze and model the jitter impact and tracking, respectively. In [20], the conventional jitter sensitivity in the frequency domain is replaced by a time-domain sensitivity function. To estimate the timing jitter induced by power supply fluctuations at the simple inverter chain, the convolution between time-domain jitter sensitivity and power supply fluctuations is calculated. The supply voltage fluctuations in this method are simply estimated by combining the known PDN impedance and load current profile. However, the voltage fluctuations calculated in this method can only reproduce a simple linear voltage regulator, which is insufficient for predicting the behaviors of modern buck regulators. Thus, PSIJ prediction with a combination of the jitter transfer function, PDN impedance, and an accurate buck regulator behavior model is still required.

In this article, the various buck regulator modeling methods are introduced from the perspective of PI, and their impacts on PSIJ prediction accuracy are discussed. For buck regulator behavior models, conventional passive component modeling methods, such as the first-order RL and four-element RL models [7], [8], the switching buck regulator model [11], and the continuous time model are applied. Each buck regulator model is adequately modeled and tuned to reproduce a target multiphase buck regulator mounted on an evaluation board (EVB). The time-domain voltage waveforms and nonlinearities are compared with measurement results to verify the simulation models. Then, the PSIJ simulation accuracy for each buck regulator modeling method is discussed. For the victim IC, an eight-stage inverter chain is applied, to which the power is supplied by the multiphase buck regulator on the EVB. The inverter chain is installed on a small PCB, for which the PDN parameters are easily measurable. An equivalent circuit of the inverter chain and the PDN impedance are implemented in the SPICE simulator along with the buck regulator models. To inject voltage fluctuations into the supply rail of the inverter chain, an embedded load current circuit of the buck regulator is used. Finally, the buck regulator output voltage noise is coupled to the inverter chain, resulting in a timing jitter. For comparison of the buck regulator models, the same load current profile is applied for each simulation. Transient analyses using different buck regulator models are performed, and the time interval errors (TIEs) for each simulation model are compared. Based on the TIEs, the advantages and disadvantages of each buck regulator modeling method from the perspective of PI, particularly PSIJ, are discussed.

II. Buck Regulator Modeling Methods

This section introduces several buck regulator modeling methods that have been developed over the past few decades and discusses the advantages and disadvantages of each model from the perspective of PI. Buck regulator models ranging from the most conventional and simplest linear RL model to the recently published continuous time behavior model are introduced. Then, the appropriate tuning and optimizing procedures for each buck regulator model are presented. The validity of each modeling method is also assessed based on a comparison between the output voltage waveform and measured results. Finally, each model is applied to the simulation setup for system-level PSIJ prediction, and jitter estimation results are discussed. First, for completeness, the modeling method of each buck regulator model is reiterated here.

Fig. 1 presents a typical current mode control topology that uses dual voltage and current feedback loops. Through remote sensing, the voltage feedback loop detects the output voltage as near to the current load as possible. This voltage is compared with the internal voltage level, generating an error signal that is processed by the proportional–integral (P–I) controller. The output from this controller and the feedback current are used as inputs for the digital comparator. The set–reset flip-flop, synchronized with the clock frequency, ultimately generates the

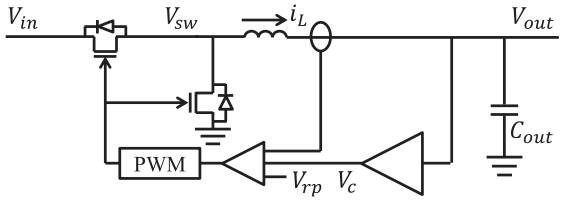

Fig. 1. Block diagram of a typical current-mode buck regulator.

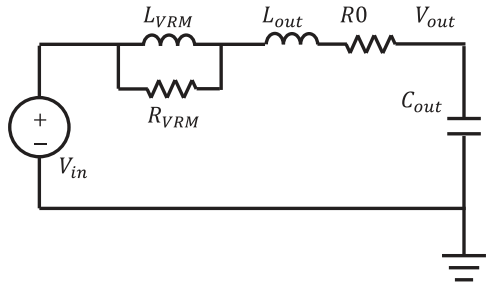

Fig. 2. Simplified block diagram of a typical buck regulator.

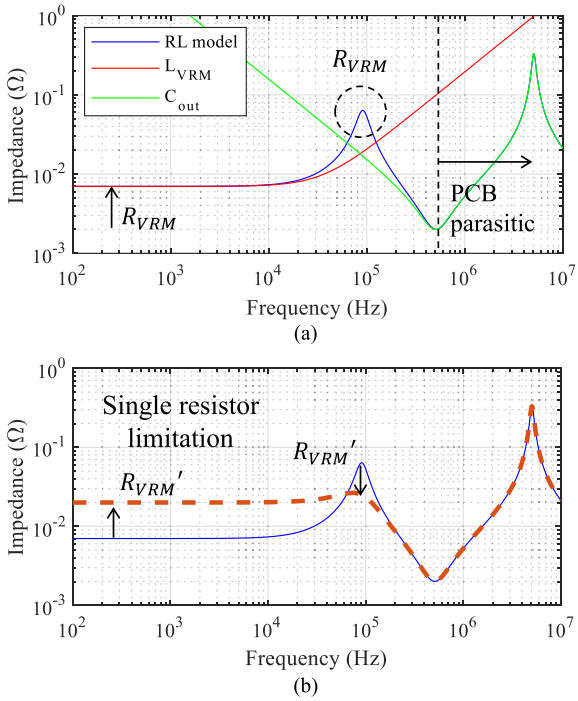

Fig. 3. Impedance described by a linear RL model. (a) Role of each component. (b) Limitation of a single resistor.

turn-ON signals to control the MOSFET switches. The dc output voltage is dependent on the input voltage and its duty cycle. Generating the appropriate duty cycle is vital to replicate an identical output voltage in the simulation model.

A. Linear RL Model

Fig. 2 depicts a simplified block diagram of a typical buck converter circuit. In this model, the current loop in Fig. 2 is ignored, and only the voltage loop is replaced by the resistors and inductors. The modeling of this method is straightforward. R_{out} is the resistance from the board between the output voltage sensing and the actual load connection points. Because remote sensing is common in modern buck regulator designs, R_{out} is usually only a few mΩ. L_{out} is the output inductance of the board, which connects the buck regulator to the load or pin headers. Generally, the output capacitor will determine the impedance after this effective frequency of the buck regulator. As introduced in this paragraph, R_0 and L_{out} are usually determined by the PCB parasitics. For the buck regulator itself, R_{VRM} and L_{VRM} must be adequately modeled. The impedance plot generated by this model is shown in Fig. 3(a). R_{VRM} represents both the damping and low-frequency impedance behavior of the buck regulator. The IR drop and dc gain limitation of the buck regulator control loop are determined by this resistance. L_{VRM} describes the impedance peak of the buck regulator. The initial voltage drops, recovery period, and fluctuation frequency are determined by this inductance, as well as the output capacitors. Thus, R_{VRM} and L_{VRM} generally describe the dc and ac behaviors, respectively. The fitting of R_{VRM} and L_{VRM} can be simply performed by measuring the output impedance of the buck regulator. With the help of a vector network analyzer or ac impedance analyzer, both the magnitude and phase can be measured.

This modeling method was developed in 1999 [7] but has still been widely used for system-level simulations among recent publications. This method can be easily applied to system-level simulations to represent a buck regulator in a simple way instead of using an ideal voltage source. The ability to perform SPICE analysis with this buck regulator model is another advantage. This model runs rapidly in both the frequency and time domains, with almost no convergence issues. This model is also highly compatible and can be applied to various simulation setups. Simple buck regulators can be sufficiently modeled by this method; however, this modeling method does have some limitations. The first limitation is flexibility. As stated above, a simple buck regulator can be easily modeled, but this model can only provide linear behavior due to the passive components. Nonlinearities of modern buck regulators with integrated functions, such as automatic phase drop (APD), AVP, or dynamic current sharing, cannot be modeled by this method. Another drawback is the limitation of a single resistor. In Fig. 3(b), two different impedance curves are described with different resistances. The low-frequency and resonance impedance of buck regulators must be modeled separately to describe the dc voltage drop and step response, respectively. However, when the resistor is required to be updated to adjust the low-frequency impedance, the damping behavior at the resonance frequency created by L_{VRM} and C_{out} will also be changed, failing to achieve a separated frequency-dependent behavior of buck regulators. These flexibilities and the single resistor limitations have hindered engineers from using this method in their simulations.

B. Four-Element RL Model

Although the linear RL model has some drawbacks, it has been widely used in recent studies [7], [8]. However, the need

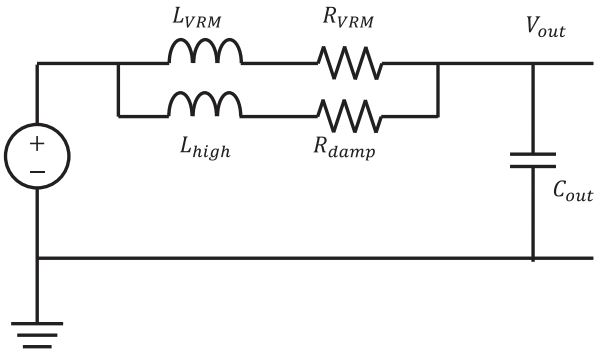

Fig. 4. Buck regulator modeling method: four-element RL model.

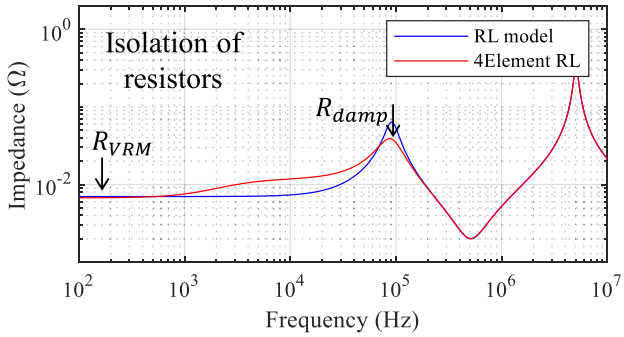

Fig. 5. Impedance described by the four-element RL model.

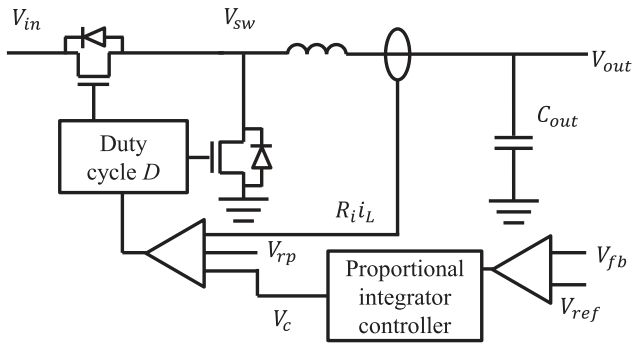

Fig. 6. Switching buck regulator model.

for a more accurate buck regulator model has emerged in the industry in order to predict system-level PI performance. Thus, a four-element RL model, which is a more advanced buck regulator model, has been developed [9]. Fig. 4 shows a simple four-element RL model that represents a buck regulator. In this model, series combinations of two RL branches are connected parallel to each other, enabling the modeling of advanced dc or low-frequency impedance, active inductance of dual current and voltage control loops, and damping behavior of the first resonance peak of the buck regulator.

Unlike the linear RL model, this model uses two different resistors, which enables the isolation of low-frequency impedance and damping behavior at the resonance peak. While the first resistor R_{VRM} is used to set the low-frequency impedance, the second resistor R_{damp} is used to independently damp the resonance peak. Because an actual buck regulator will not deliver a large amount of current at high frequencies, an appropriate inductance must be used to block the high-frequency current. L_{VRM} is used to describe the active inductance of control loops, which shows a high-impedance resonance combined with the output capacitor. Thus, the high-frequency current can be blocked by a smaller inductance L_{high} combined with a damping resistor R_{damp}. Finally, one can fit the isolated low-frequency impedance, damping behavior, and active inductance of control loops by adjusting each component until the model shows a good correlation with measurements.

The advantages and disadvantages of this modeling method are similar to those of the linear RL buck regulator model. Because this modeling method uses a pair of passive components, the tuning and optimization process is relatively simple. Compared with the linear RL model, the four-element RL model enables the isolation of resistances, which overcomes a significant drawback of the previous buck regulator model. The isolation of resistance behaviors is displayed in Fig. 5, which shows that one can adjust the low-frequency impedance without changing the damping behavior at the resonance frequency. In addition, this modeling method can be rapidly applied in SPICE simulations in both the time and frequency domain. However, the flexibility of this method still presents a limitation. Although the four-element model allows for versatile applications because of its second-order expression, the nonlinearity of recent buck regulators cannot be modeled by passive components. Therefore, rigorous buck regulator modeling methods are required to simulate an accurate end-to-end PI analysis.

C. Switching Buck Regulator Behavior Model

To overcome the limitations of passive component modeling methods, such as the first-order RL and four-element RL methods, a buck regulator model based on nonlinear switching behavior has been proposed [11]. This model utilizes physical switches, dual voltage and current control loops, and a set–reset flip-flop to generate PWM operating signals. As depicted in Fig. 6, the input voltage V_{in} is stepped down to V_{out} with voltage and current feedback loops. In this model, the power transistors are replaced by the simple switches with turn-ON resistance r_{on}. The error between the reference and feedback voltages V_{ref} and V_{fb} is fed to the P–I controller and generates V_c. Finally, the controller voltage V_c, feedback current $R_i i_L$, and ramp compensation voltage V_{rp} generate pulses with duty cycle D determining the output voltage. The detailed modeling process is presented in the upcoming paragraphs.

The nonlinear behaviors observed in buck regulators are primarily influenced by the voltage and current control loops. The voltage feedback and the control loop are stimulated by the feedback voltage V_{fb}, as shown in Fig. 6. The control loop, comprising components, can be represented as a typical P–I controller. Therefore, design parameters, such as the proportional gain K_p, integral gain K_i, dc gain limitation K_{dc}, and cutoff frequency of the low-pass filter (LPF) f_c, must be considered in this controller. The control voltage V_c is fed to the comparator to

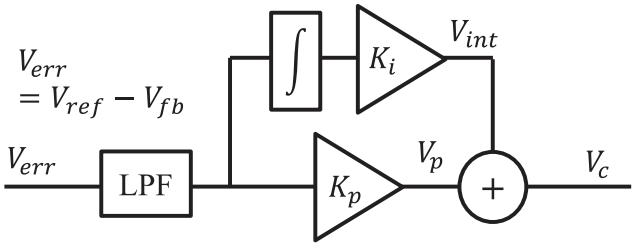

Fig. 7. Proportional–integrator controller of voltage feedback loop.

generate an alternating turn-ON signal in the PWM controller. An equation for the voltage feedback loop is as follows [13], [14]:

$$V_c = V_P + V_{\text{int}} = \left(K_p + \frac{K_{\text{dc}}}{sK_{\text{dc}}/K_i + 1}\right) V_{\text{err}} \qquad (1)$$

where $V_{\text{err}} = V_{\text{ref}} - V_f$, V_P, and V_{int} are the output of PI controllers as shown in Fig. 7. In recent buck regulators, the current feedback loop is also utilized to collect the inductor current and generate the control signal [11], [13], [14]. The current feedback loop incorporates several design parameters. In Fig. 6, the generic current feedback loop includes R_i, the current sensing gain, to sense the inductor current as a voltage. The control signal is then fed to the comparator and generates a turn-ON signal in the PWM controller. In this design, a slope compensator V_{rp}, which is used to improve the PSRR performance of the buck regulator, is applied.

The external buck regulator components must be modeled as well as the control loops. Since the passive elements significantly influence the behaviors, the output capacitor and external inductor must be applied to the behavior model first. After the passive elements modeling of the switching buck regulator is completed, the design parameters of control loops, power stages, and external circuits must be optimized secondly. A two-step design parameter optimization process has been well described in [12]. In the two-step optimization, first, the steady-state response parameters of the buck regulator are tuned. From measurements of the output voltage depending on the load current, an IV curve of the buck regulator can be easily characterized. Then, the steady-state response parameters, such as K_{dc}, V_{rp}, and R_i, must be optimized until the simulated IV curve is fitted to the measurement results. After the steady-state response of the buck regulator has been optimized, the step response must be optimized. In this stage, the design parameters K_p and K_i, which impact the initial drop and recovery period, can be tuned. If both the steady-state and step responses are optimized, the buck regulator model can be further validated under various loading current conditions. Although this modeling method implements dual control loops with physical switches, some additional features of modern buck regulators are still required. The most general nonlinear features of complex multiphase buck regulators are load line regulation and APD. Herein, to simulate realistic cases of actual buck regulators, the modeling methods of load line regulation and APD are introduced.

Load line regulation has been introduced as AVP in [23] and [24]. AVP has become increasingly important because of its ability to meet strict load transient requirements and spatial

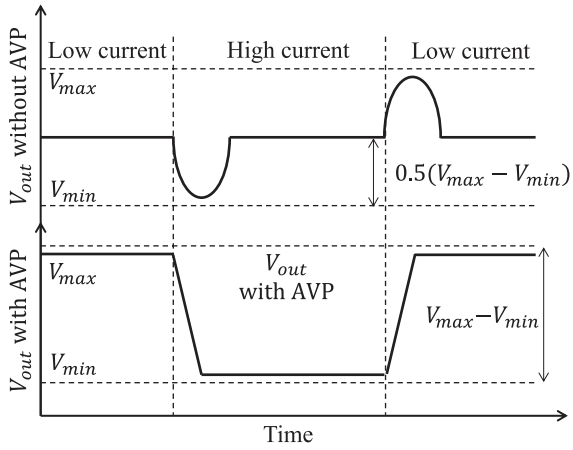

Fig. 8. Output voltage waveforms depend on the AVP.

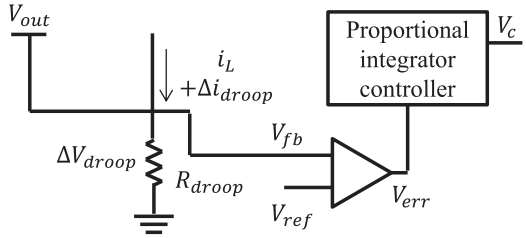

Fig. 9. AVP function blocks in the voltage control loop.

constraints. AVP is closely related to the step response of the buck regulator under heavy load conditions. The output voltage waveform depends on the AVP design that is depicted in Fig. 8 [11]. Without AVP design, the output voltage exhibits undershooting and overshooting voltages associated with the load current. In this case, the noise margin of each voltage fluctuation is limited by half of the max-to-min voltage window. However, when the buck regulator activates AVP, the allowable noise margin is doubled for the same number of output capacitors. This result allows for a reduction in the number of required output capacitors, making AVP design a more efficient and space-saving solution. To model AVP in the simulation, the voltage control loop must be updated. Fig. 9 shows a simple block diagram of a voltage loop that includes a droop resistance. R_{droop} compensates for the error voltage when a significant voltage drop is detected in the feedback voltage V_{fb}. Thus, the voltage control loop will not regulate the voltage drop of the buck regulator, and an intentional voltage droop is created on the output, as shown in Fig. 8. In this design, the intentional voltage droop is controlled by resistance applied to the control loop. This equivalent resistance load line regulation is denoted herein as R_{LL}. The buck regulator operates as a simple resistor if AVP is activated, but still achieves a low quiescent current because of the dual voltage and current control loops.

To further improve the switching behavior of the buck regulator model, APD is applied to provide phase transitions according to the change in load current [14]. This feature is usually designed for multiphase buck regulators shown in Fig. 10, which

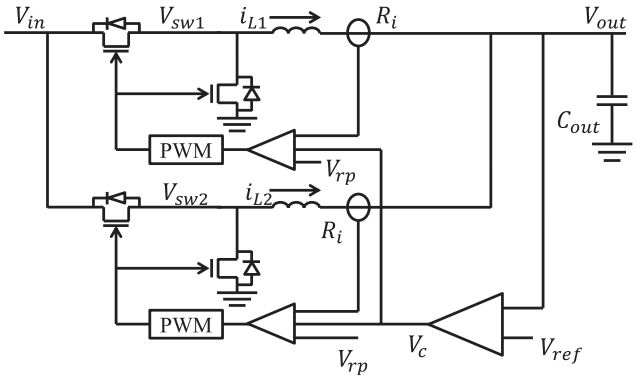

Fig. 10. Multiphase switching buck regulator model.

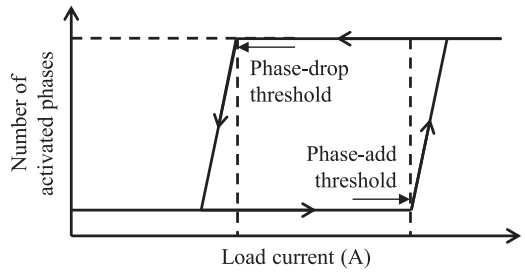

Fig. 11. Hysteresis of phase activation control.

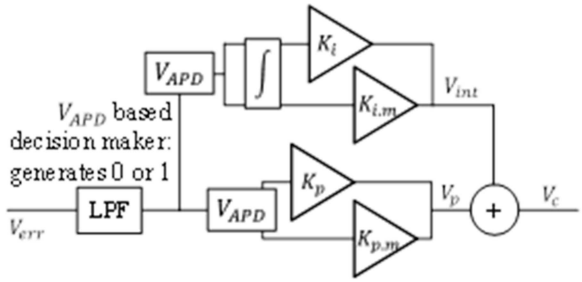

Fig. 12. Load current dependent proportional–integrator controller.

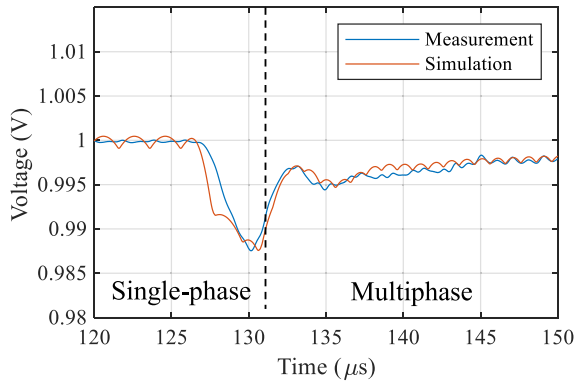

Fig. 13. Nonlinear behavior of output voltage with phase transition.

use a number of identical power stages in parallel. Multiphase operation in buck regulators ensures a stable voltage supply during heavy loading conditions. However, activating auxiliary phases under light loading conditions is inefficient because of the increase in switching loss, resulting in decreased power efficiency. To address this issue, an activation control mechanism for power stages, known as phase shedding/adding or auto phase adding/dropping, has been developed. In [14], the simulation model activates auxiliary phases based on the hysteresis of load current and the number of phases. Under light loading conditions, the buck regulator uses only the primary phase. When the load current increases and exceeds the threshold described as I_{add}, the secondary phase is activated after the delay T_{add}, and design parameters preoptimized for multiphase operation are applied. For the activation of auxiliary phases, a Schmitt trigger, which is synchronized with the hysteresis as shown in Fig. 11, is used. This circuit generates V_{APD}, which triggers a design parameter update and activation of the secondary phase. The proposed equation in [14] for the multiphase voltage control loop can be found as

$$V_P = K_p\, V_{\text{err}}\,(1 - V_{\text{APD}}) + K_{p.m} V_{\text{err}} V_{\text{APD}} \tag{2}$$

$$V_{\text{int}} = V_{\text{err}}\,\frac{K_{\text{dc}}}{sK_{\text{dc}}/K_i + 1}\,(1 - V_{\text{APD}}) + V_{\text{err}}\frac{K_{\text{dc}.M}}{sK_{\text{dc}.m}/K_{i.m} + 1} V_{\text{APD}} \tag{3}$$

where $K_{p.m}$, $K_{\text{dc}.m}$, and $K_{i.m}$ are the design parameters of the P–I controller which describes the multiphase behavior shown in Fig. 12. Unlike [7], the control signal V_c can then be characterized by two different parameter sets. Because the output of each phase is merged at the output capacitor, a single voltage loop described by the above equations can dictate the phase transition behaviors. To activate the multiphase operation, a simple digital circuit that uses V_{APD} as an input is applied. When V_{APD} is set to 1 based on the hysteresis, the design parameters for multiphase behavior are activated and begin to regulate the output voltage. The similar behavior of phase drop can also be described with additional parameters, such as I_{drop} and T_{drop}, based on the hysteresis. A phase transition example of the output voltage with designed APD is shown in Fig. 13. This figure clearly shows that a small fluctuation in the measured voltage drop is successfully reproduced in the simulation model. More detailed descriptions of design parameters and voltage waveform comparison will be introduced in the next section.

The overall design parameters for the multiphase operation are summarized in Table I. In this modeling method, the design parameters are distinguished by two different types: known parameters and tuned parameters. The known parameters can be easily found from the buck regulators' datasheet or the simple measurement. The extracted and tuned parameters describe the control loops and can be characterized by the two-step parameter extraction methods introduced in the previous paragraph. With the appropriately characterized design parameters, the buck regulator model can imitate the transient behaviors of the actual circuit.

The biggest advantage of this modeling method is its flexibility. Because the buck regulator model includes physical

TABLE I
DESIGN PARAMETERS OF A MULTIPHASE BUCK REGULATOR

Type	Parameter	Description
Known parameters	L	External inductor
	C_{out}	Output capacitance
	r_{on}	Turn-on resistance
	r_L	DC resistance of inductor
	V_{ref}	Reference voltage
	V_{in}	Input voltage
	T_{sw}	Switching period
	T_{add}	Phase add delay
	T_{drop}	Phase drop delay
	I_{add}	Phase add threshold
	I_{drop}	Phase drop threshold
Extracted and tuned parameters	R_i	Current sense gain
	V_{rp}	Ramp compensation
	$K_{P,S}$	Proportional gain: single-phase
	$K_{P,M}$	Proportional gain: multiphase
	$K_{I,S}$	Integrator gain: single-phase
	$K_{I,M}$	Integrator gain: multiphase
	$K_{DC,S}$	DC limitation: single-phase
	$K_{DC,M}$	DC limitation: multiphase

switches, dual voltage and current control loops, and add-on functions, such as AVP and APD, it can be widely applied to the complex multiphase buck regulators on the market. Furthermore, the various steady-state and step responses of different buck regulators can be reproduced by updating the design parameters summarized in Table I. The buck regulator model shown for this method can be implemented in a conventional SPICE tool and can be easily combined with system-level PI analysis as well. However, the complicated modeling process is a substantial drawback of this method. To generate the switching buck regulator behavior model, a measurement-based control loop model must be carefully designed, as well as the parasitics of passive components and the PCB. Another limitation is the computational load. The buck regulator model activates physical switches based on PWM signals. If the number of phases increases with a high switching frequency to mimic modern multiphase buck regulators, the simulation time is greatly increased. Thus, a new modeling method must be developed to reduce the computational load while maintaining simulation accuracy.

D. Continuous Time Buck Regulator Model

To address the drawbacks, such as the complexity of the model and computational load of the switching buck regulator modeling method, a continuous time buck regulator modeling method has been developed [13], [14]. This section introduces the buck regulator modeling method described in [14]. A simplified circuit of the continuous time buck regulator model is shown in Fig. 14. The continuous time model calculates the real-time averaged voltage and current information of the buck regulator based on the design parameters. The modeling methods of dual voltage and current feedback loops are identical to the switching

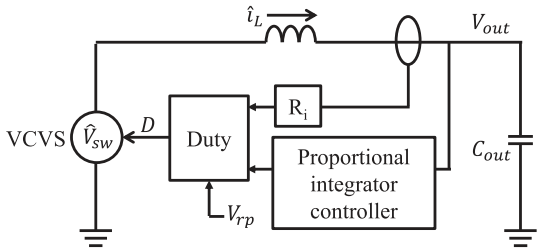

Fig. 14. Simplified block diagram of a continuous time single-phase buck regulator model.

buck regulator modeling method. The design-parameter-based control loops are then combined to update the time-averaged duty cycle D [13]

$$D = \frac{1}{2} + \frac{V_{\text{rp}}}{T_{\text{SW}}\Delta S R_i} - \sqrt{\left(\frac{1}{2} + \frac{V_{\text{rp}}}{T_{\text{SW}}\Delta S R_i}\right)^2 - \frac{2}{T_{\text{SW}}\Delta S}\left(\frac{V_C}{R_i} - \widehat{i_L}\right)}. \tag{4}$$

Because this model is a simplified version of the switching behavior model, the design parameters and control loops are the same as those used in the previous section. In this model, an additional variable ΔS is used to describe the slope changes of the inductor current as follows [13]:

$$\Delta S = \frac{V_{\text{in}} - \hat{i}_L\left(r_{\text{on}.H} + r_L\right) - V_{\text{out}}}{L} + \frac{\hat{i}_L\left(r_{\text{on}.L} + r_L\right) - V_{\text{out}}}{L}. \tag{5}$$

The hat symbols in (4) and (5) indicate the average terms for this modeling method. The voltage-controlled voltage source (VCVS) $\hat{V}_{\text{sw}}$, which represents the time-averaged voltage behavior of the switching node shown in Fig. 14, is calculated as follows [13]:

$$\hat{V}_{\text{sw}} = D\left(V_{\text{in}} - r_{\text{on},H}\hat{i}_L\right) - (1-D)\, r_{\text{on},L}\hat{i}_L. \tag{6}$$

The combination of D and other parameters in (6) can be updated to mimic any type of PWM- or continuous conduction mode based buck regulator.

This modeling method can be further extended to reproduce multiphase buck regulator behaviors. In Fig. 15, multiple VCVSs representing the primary and secondary switching node voltages are implemented. Similar to the previous modeling method, the continuous time model uses a single voltage and current loop in the multiphase buck regulator. For realistic modeling of multiphase behaviors, a switching delay between the primary and secondary phases is applied to the voltage loop. Furthermore, nonlinear behaviors, such as AVP and APD, for multiphase operation are applied. The AVP, which converts the behavior of the buck regulator as a simple resistor, can be modeled in the continuous time model by applying a droop resistance to the voltage loop [11]. To control the phase activation of the

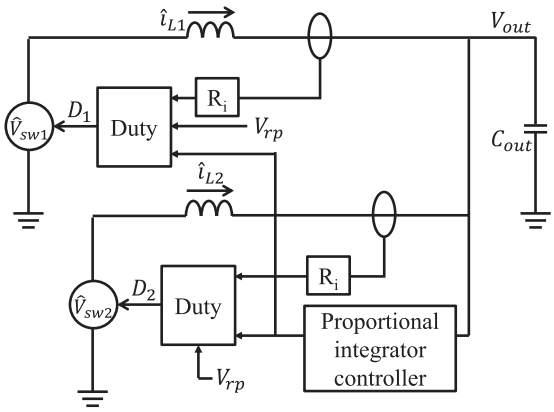

Fig. 15. Block diagram of the continuous time multiphase buck regulator model.

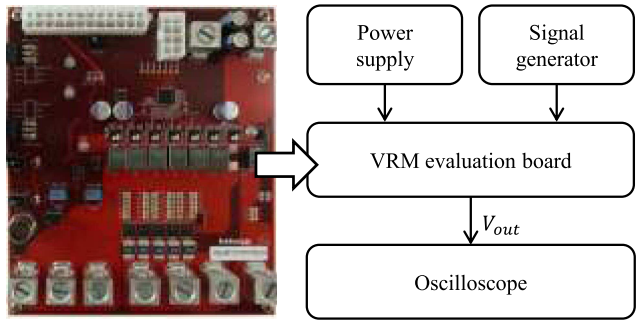

Fig. 16. Evaluation board (EVB) for validation of buck regulator modeling methods.

multiphase buck regulator, an identical hysteresis of the phase control introduced in the previous switching VRM modeling method according to the load current is used. In the previous section, the trigger circuit was utilized to generate V_{APD} to select the proper equation and parameters for multiphase operation. However, the physical switches are replaced by VCVSs in Fig. 15, and the behaviors can be modeled with an analytical equation. The average switching voltage of the secondary phase $\hat{V}_{\text{sw2}}$ can be described as follows [14]:

$$\hat{V}_{\text{sw2}} = \left(D_2\left(V_{\text{in}} - r_{\text{on},H}\hat{i}_{L2}\right) - (1-D_2)\, r_{\text{on},L}\hat{i}_{L2}\right) V_{\text{APD}} + V_{\text{out}}\left(1 - V_{\text{APD}}\right) \quad (7)$$

where $\hat{i}_{L2}$ and D_2 are the average inductor current and duty cycle of the secondary phase, respectively. Like the previous modeling method, the multiphase operation is described by (2) and (3) and dictates the overall duty cycles D and D_2. Finally, APD is implemented with the design parameters summarized in Table I and by combing (2)–(7).

This modeling method has the advantages of accuracy and flexibility. Because this model utilizes nonlinear multiphase behaviors, it can be applied to simulation setups for modern buck regulators. Furthermore, compared with the previous method, the computational load is improved. The continuous modeling method uses time-averaged VCVSs without any physical switches. Without the switching behaviors, this modeling method can complete simulations with multiple phases approximately 10-fold faster than the switching method. However, the time-averaged behavior presents a drawback of this method. Because this model sacrifices the switching behaviors, it cannot perform simulations that require switching noise generation. Consequently, this method is applicable to simulation setups that are focused on the conduction noise on the power rail.

III. Measurement Validation and Comparison of Buck Regulator Modeling Methods

In the previous section, buck regulator modeling methods for PI simulation were introduced, and the pros and cons of each model were discussed. In this section, each modeling method is validated by comparing the output voltages with measurements. The buck regulator models in various simulation platforms are tuned or optimized to reproduce the same multiphase buck regulator EVB for a fair comparison. An ISL68137-61P-EV1Z target multiphase buck regulator EVB is utilized, as shown in Fig. 16 [29]. For activation of the EVB, an external dc power supply and signal generator are used. While the multiphase buck regulator is in normal operation, the step and steady-state responses controlled by the signal generator are injected. With a known load current profile, the buck regulator behaviors, such as phase activation control, load line regulation, and simple multiphase operations, are measured.

The design parameters to imitate the target EVB are summarized in Table II. The switching frequency and the cutoff frequency of the LPF of ISL68137-61P-EV1Z are configured as

TABLE II
Characterized Multiphase Buck Regulator

Type	Parameter	Value
Known parameters	L	120 nH
	C_{out}	2830 µF
	$r_{on,H}$,	10 mΩ
	r_L	0.9 mΩ
	V_{ref}	1 V
	V_{in}	12 V
	T_{sw}	2 µs
	T_{add}	3 µs
	T_{drop}	9 µs
	I_{add}	20 A
	I_{drop}	15 A
Extracted and tuned parameters	R_i	0.2
	V_{rp}	0.32 V
	$K_{P,S}$	320
	$K_{P,M}$	180
	$K_{I,S}$	40 000 000
	$K_{I,M}$	30 000 000
	$K_{DC,S}$	4000
	$K_{DC,M}$	2200

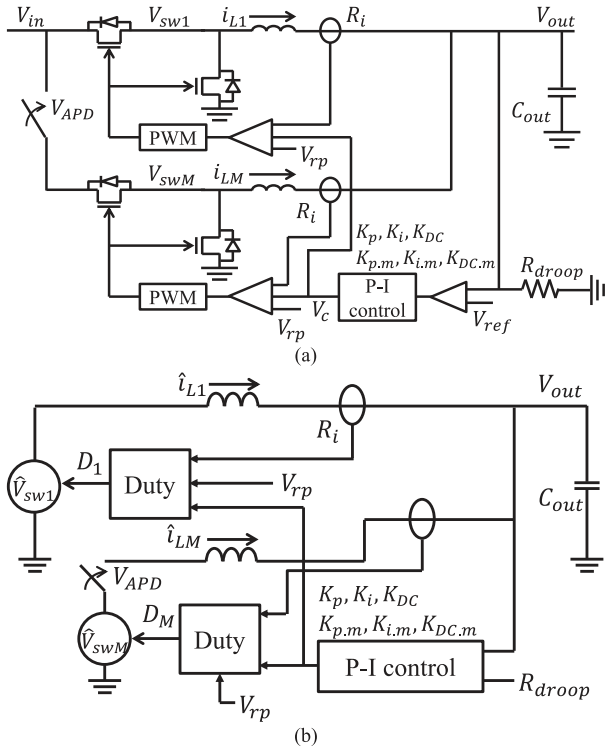

Fig. 17. Simulation setups: (a) switching model and (b) continuous-time model.

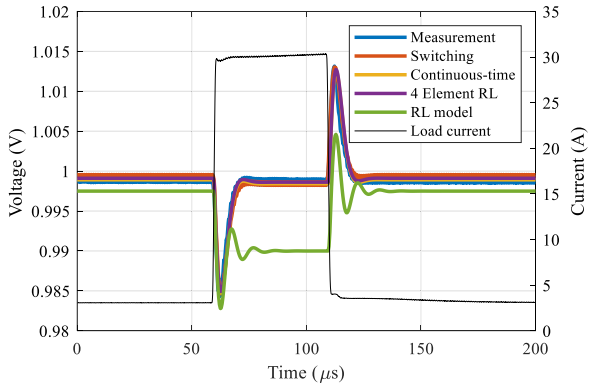

Fig. 18. Full multiphase operation with a load current of 3–30 A/μs.

500 KHz and 6 MHz, respectively. The remaining known parameters summarized in Table I are applied based on the datasheet of EVB. To reproduce the output voltage waveforms of a target buck regulator, the required design parameters for switching and continuous-time buck regulator models are extracted with the two-step parameter extraction method.

The simulation setups of switching and continuous-time models are shown in Fig. 17. For the switching model, multiple switches, external inductors, and a capacitor are implemented in Keysight ADS with equation-based function blocks SDDnP. The continuous-time model is modeled in Synopsys HSPICE with equation-based user-defined voltage sources VCVSs to describe the basic regulation and add-on functions of buck regulators. For the validation of modeling methods, the design parameters summarized in Table II are applied to both switching and continuous-time models.

A. Simple Multiphase Operation

The input voltage for the multiphase operation is 12 V, and the output voltage is set to 1 V. For a fair comparison of each simulation model, the design parameters summarized in Table II are used for all validation cases along with nonlinear functions to evaluate the flexibility of each model. The measured voltage waveform with the known loading condition is shown in Fig. 18. For simplicity of the experiments, three phases are activated rather than all seven phases in the EVB. Overall, the measured and simulated voltage waveforms show good correlations, except for the simple RL model. The root-mean-square (rms) error of each modeling method from the simple RL model to the continuous time model is 3.14%, 0.71%, 0.69%, and 0.71%. Because the RL model fails to isolate the low-frequency impedance and resonance damping, this model cannot provide step or steady-state responses for a multiphase buck regulator. However, the four-element RL model still provides a high accuracy owing to the isolation of resistance behaviors.

B. Phase Activation Controls

To further validate the simulation models, APD is triggered in the EVB. With the modeled phase activation control, the switching and continuous time models can reproduce the phase transition in time-domain simulations. The phase transitions from single-phase to multiphase are compared in Fig. 19. Overall, the switching and continuous time modeling methods effectively capture the phase transitions at both the rising and falling edges of the load current. However, the passive component models, such as the simple RL and four-element RL models, fail to provide the phase transition. In particular, the four-element modeling method fails to reproduce the steady-state behavior under light loading conditions shown as a single-phase period. Because this model only targets the multiphase design parameters, the steady-state response of the single-phase period and the initial voltage drop at the phase transition are not captured. This comparison clearly shows that the conventional passive component modeling methods fail to mimic the output voltages when additional nonlinear behaviors are added in an actual buck regulator.

C. Load Line Regulation

Last, load line regulation or AVP is activated in the EVB, and the output voltage is compared. To validate the AVP under various conditions, the droop resistor that compensates for the initial error voltage is set to 0.9 mΩ. The load current is stepped up from 3 to 30 A with a rise time of 1 μs. The comparison results of four different buck regulator modeling methods are shown in Fig. 20. Only the switching buck regulator and continuous time models can reproduce the load line regulation sometimes referred to as AVP. These two simulation models show a dc voltage droop of 24.36 mV associated with the load current.

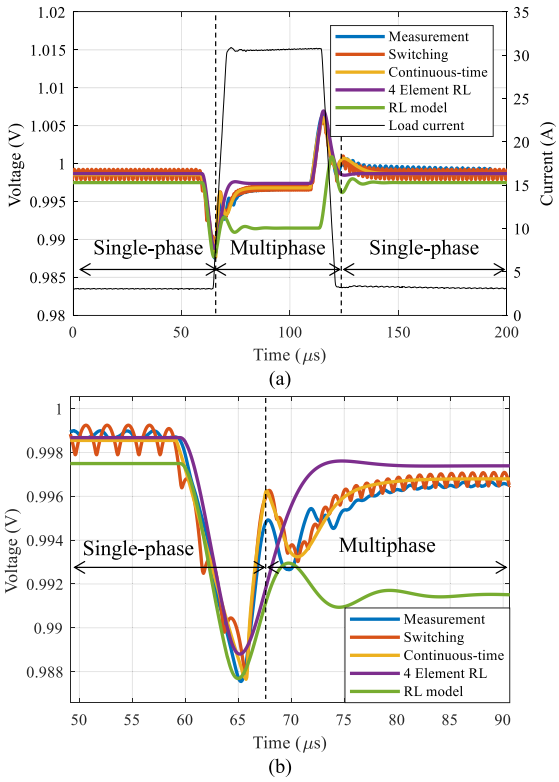

Fig. 19. Phase activation control with a load current of 3–30 A/5 μs. (a) Transient response. (b) Zoomed-in figure of undershooting voltage.

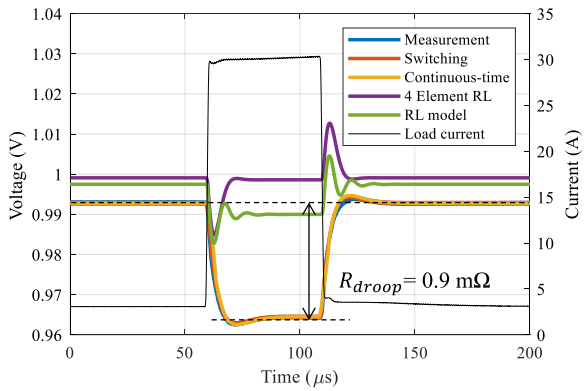

Fig. 20. Load line regulation with a load current of 3–30 A/μs.

However, the passive component modeling methods fail to generate the load line regulation of the multiphase buck regulator. The overall comparison results are summarized in Table III.

The rms errors calculated from the measurement results clearly show that the buck regulator models that include voltage and current feedback loops are superior to the passive component modeling methods. Compared with the switching model, the continuous time model has a slightly higher rms error because the switching voltage behaviors are excluded. With respect to running time, the passive component modeling methods are faster than the other modeling methods. Based on the comparison results, one must consider the purpose of the analysis when selecting a buck regulator modeling method. When the

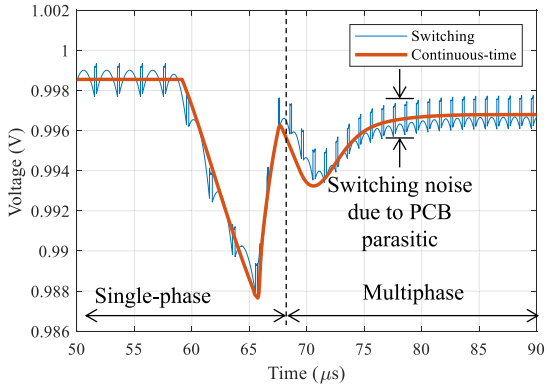

Fig. 21. Additional noise due to PCB parasitic in the switching model.

conduction voltage noise on the power rail must be simulated as rapidly as possible, the passive component and continuous time modeling methods are suitable. However, a switching noise created by the parasitics of PCB cannot be created by the continuous-time model. The voltage waveforms of the switching and continuous-time model with PCB parasitics, such as inductance and resistance, are shown in Fig. 21. Due to the parasitic of PCB, the switching model creates the additional noise at every turn-ON and -OFF period. If the PI analysis requires this switching noise associated with the PDN and switch parasitics, the switching buck regulator modeling method would be the best option.

IV. PSIJ Simulation Accuracy of Each Buck Regulator Modeling Method

In this section, the buck regulator modeling methods are discussed from the perspective of PSIJ from the buck regulator to the victim IC. Thus, the buck regulator modeling methods from the previous chapter are applied to a PSIJ simulation setup as the power supply of a single-ended buffer circuit.

For the typical PSIJ analysis method, the jitter sensitivity, which is a function of output jitter when a single frequency noise is applied to the power supply voltage, is used. The jitter sensitivity assumes that the output jitter is linearly associated with the magnitude of the noise on the power supply rail [26], [27], [28]. In this analysis, the jitter sensitivity and power supply rail noise for the PSIJ simulation are replaced by the circuit model and output voltage of the buck regulator, respectively. The introduced buck regulator modeling methods have been validated in time-domain measurements; thus, the PSIJ injected by the buck regulator is simulated by defining the TIE. The TIE is introduced to describe the real-time difference between the ideal and actual clock edge at any arbitrary switching time. The total timing jitter can then be determined from the peak-to-peak amplitude of the simulated TIE. The jitter sensitivity for PSIJ simulation is replaced by the equivalent circuit of the inverter chain in the SPICE-based simulator as follows.

A. PSIJ Simulation Setup and DUT

In PSIJ simulation, an inverter-type CMOS buffer is selected as the device to be tested. The inverter chain circuit is

TABLE III
OVERALL COMPARISON OF BUCK REGULATOR MODELING METHODS

Simulation model	Simple multiphase operation		Phase activation control		Load line regulation	
	RMS error	Simulation time	RMS error	Simulation time	RMS error	Simulation time
Switching model	0.69 %	4.07 sec	0.61 %	4.68 sec	0.46 %	4.24 sec
Continuous time model	0. 71 %	1.14 sec	0.81 %	1.15 sec	0.56 %	1.23 sec
4-element RL model	0.71 %	1.10 sec	1.83 %	1.10 sec	11.89 %	1.10 sec
Simple RL model	3.14 %	1.08 sec	2.08 %	1.08 sec	9.11 %	1.08 sec

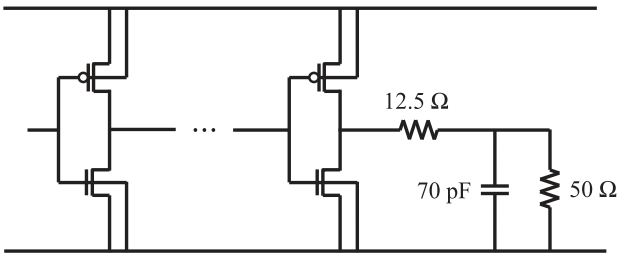

Fig. 22. Equivalent circuit of the output resistance and capacitance.

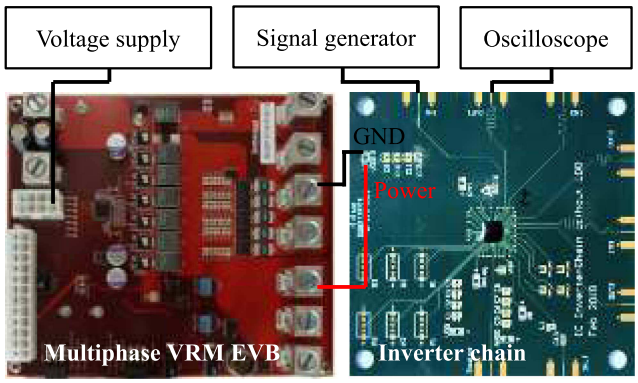

Fig. 23. Measurement setup for determining the TIE due to buck regulator behavior.

designed and fabricated on a simple PCB with external activation connectors for the inverter circuit. To provide power to the inverter chain, external voltage connection pads and decoupling capacitors are applied to the PCB. The inverter chain circuit with the equivalent load implemented in the simulation setup is shown in Fig. 22. The same transistor library used in [20] is applied to describe each MOSFET switch to achieve the feasibility of PSIJ simulation. At the output of the inverter chain, the equivalent resistor and capacitor are applied. During dc behavior measurements, an inverter output of 1.2 V is measured when 1.8 V of dc power is supplied. Thus, the equivalent resistance applied in the simulation is determined as 12.5 Ω. With 18 MHz sinusoidal noise injected into the power rail, the low-frequency jitter sensitivity is measured. Originally, the equivalent capacitance determined in [20] was set to 90 pF to reproduce the measured jitter sensitivity. However, in this article, an equivalent capacitance of 70 pF is applied to the simulation setup. Finally, the target inverter chain circuit is implemented in the SPICE simulator and validated through a comparison between PSIJ sensitivity simulation and measurements [20].

B. Buck Regulator Modeling Methods From the Perspective of PSIJ

With the inverter chain circuit, the PSIJ injected by external buck regulator behavior is analyzed. The setup for measuring the TIE is shown in Fig. 23. As mentioned in the previous section, the EVB of the multiphase buck regulator is used as an external power supply for the inverter chain. The output of the buck regulator is connected to the power node of the inverter chain PCB. Then, decoupling capacitors are applied at the same power node for the inverter chain. To trigger the inverter chain, an external signal generator is connected through the SMA connector, and a 20 MHz clock pulse is applied. The output of the inverter chain is connected to a 50 Ω oscilloscope, and the measured inverter output is compared with the ideal clock signal. To create a voltage fluctuation in the buck regulator output, the embedded load current circuit installed on the EVB of the buck regulator is used. With the intentional load current, the nonlinear behaviors are triggered in the actual buck regulator circuit and simulated in the simulation setup. The simulation setup with the simplified buck regulator block is shown in Fig. 24. After the buck regulator is implemented, PCB parasitics, such as on-die parameters, bond wire, and plane capacitance, are applied. The parasitics of the PCB were previously determined in [20]. Finally, an inverter chain circuit with the equivalent resistor and capacitor, which were introduced in the previous section, is applied. For activation of the inverter chain in the simulation, a clock pulse identical to the measurement is injected.

For the PSIJ measurement, a histogram of TIE caused by random thermal noise in the inverter output was measured by the oscilloscope, as shown in Fig. 25 first. Because the switching frequency of the inverter chain is 20 MHz, a long duration is required to measure and simulate the low bit error rate (BER). Thus, the random thermal noise within the time window of 500 μs, which targets a BER of 10^{-4}, is measured. The postprocessing for the TIE histogram calculation is as follows: first, the

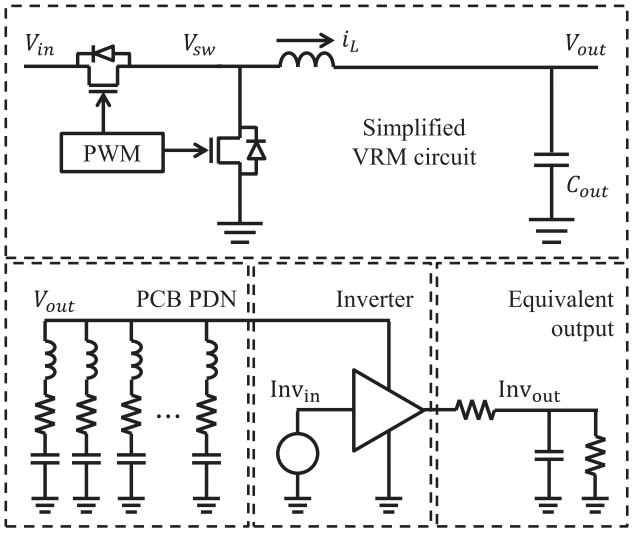

Fig. 24. Simulation setup for jitter analysis.

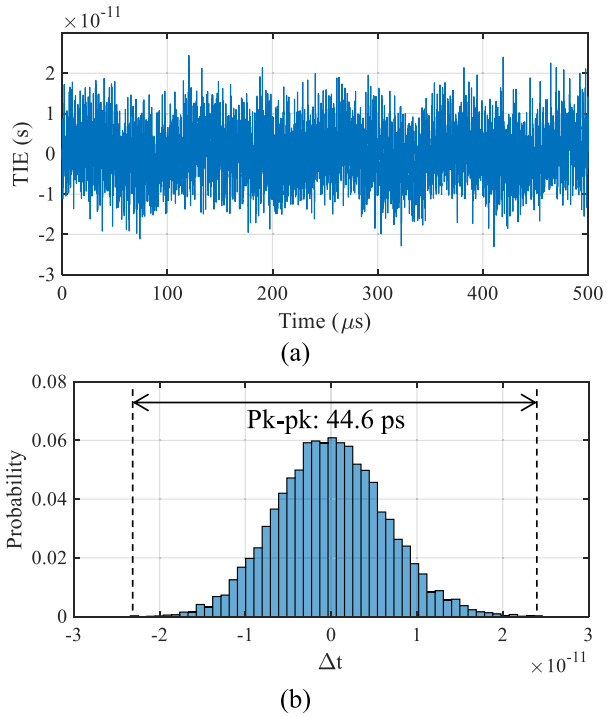

Fig. 25. Measured TIE caused by random noise. (a) TIE measurement results. (b) Histogram of measured TIE.

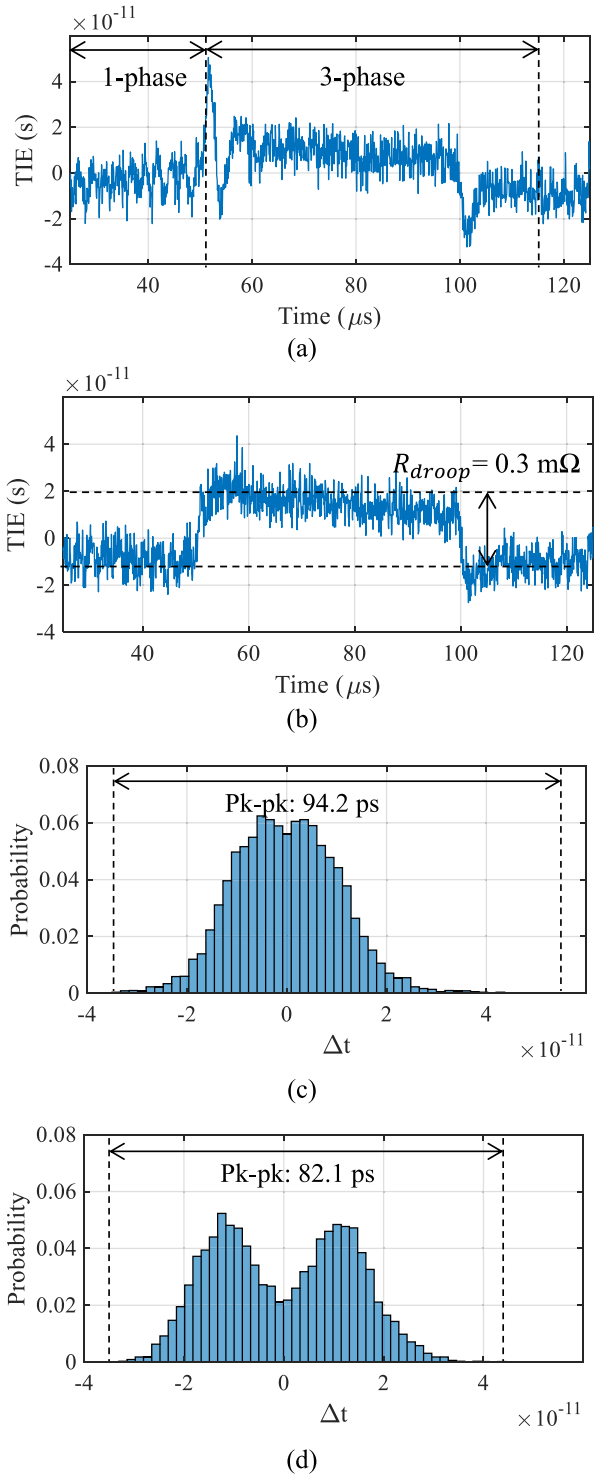

Fig. 26. Measured TIE injected by buck regulator behaviors. (a) TIE with APD. (b) TIE with AVP. (c) Histogram with APD. (d) Histogram with AVP.

output of the inverter chain is measured. Then, the total delay is extracted by subtracting the ideal clock edge from the rising edge of the inverter output. This total delay is a combination of the propagation delay of the inverter chain and the random delay caused by the random thermal noise. Finally, the pure propagation delay of the inverter chain is subtracted from the total delay extracted in the previous step. The remaining random delay is the TIE, which can be displayed as a histogram, as shown in Fig. 25(b). The measured peak-to-peak random jitter (RJ) is 44.6 ps, with a standard deviation of 5.81 ps. This measurement is applied later to estimate the peak-to-peak total jitter from the simulation.

The same postprocessing can be applied to assess the effect of buck regulator behavior on PSIJ. The TIEs and corresponding histograms depend on the buck regulator behaviors are shown in Fig. 26. A load current of 3–45 A/μs with a pulse width of 50 μs

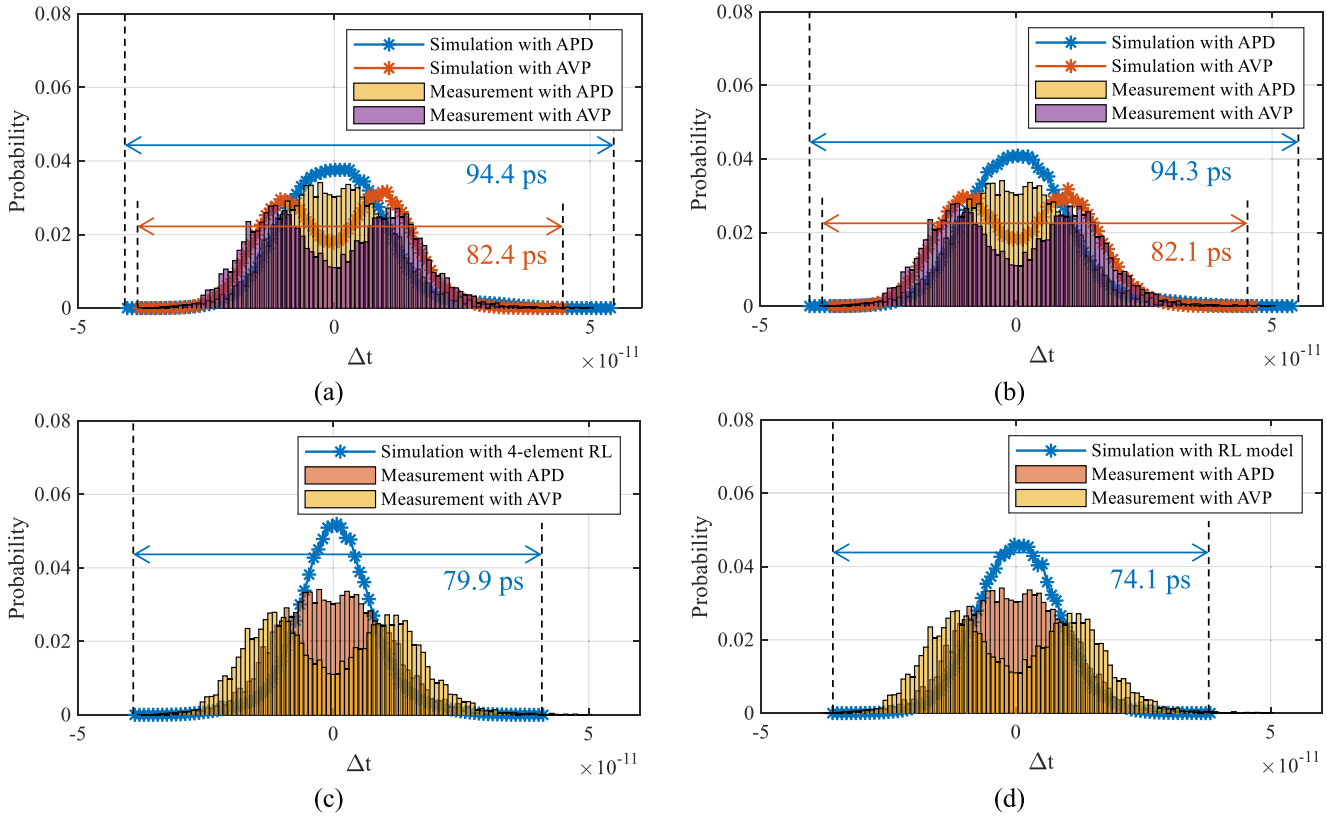

Fig. 27. Simulated PSIJ for each buck regulator modeling method. (a) Histogram of TIE for the switching buck regulator model. (b) Histogram of TIE for the continuous time model. (c) Histogram of TIE for the four-element RL model. (d) Histogram of TIE for the linear RL model.

is applied, and AVP and APD are activated in each measurement. In the operation of the inverter chain, the supply voltage affects the propagation delay. Thus, the fluctuation of the supply voltage causes variation in the propagation delay resulting in the jitter, called PSIJ. In this experiment, AVP and APD are applied to the buck regulator, resulting in two different power supply voltage fluctuations. The corresponding results of voltage fluctuations in terms of PSIJ histogram are shown in Fig. 26(c) and (d). When only APD is activated, a larger voltage drop in the buck regulator output can occur [Fig. 26(a)] because the buck regulator is still in single-phase operation. As a result, a large delay in the output of the inverter chain synchronized with the voltage drop can be measured, resulting in higher peak-to-peak jitter. In contrast, the case in which AVP is triggered shows a lower peak-to-peak jitter because the voltage droop is optimized by the load line regulation. From this measurement, total peak-to-peak PSIJ values of 94.2 and 82.1 ps are measured.

To estimate the peak-to-peak PSIJ, the TIE is first simulated with the buck regulator and inverter circuit. Because there is no random thermal noise in the simulation, the TIE can be described purely by the deterministic jitter (DJ) of the buck regulator. Then, the total peak-to-peak PSIJ can be estimated with the convolution of RJ and DJ [30], [31]. The total PSIJs simulated with different buck regulator modeling methods are shown in Fig. 27. Because the switching and continuous time buck regulator modeling methods can reproduce the APD and AVP, the impact of buck regulator behavior on the jitter is successfully generated. In the PSIJ simulation, the supply voltage fluctuation caused by the buck regulator usually occurs at frequencies lower than the roll-off frequency of jitter sensitivity, the jitter sensitivity of the inverter circuit can be treated as a constant value at the frequency range of the buck regulator. Thus, PSIJ properties injected by the buck regulator behavior can be determined from the steady-state, step response, AVP, and APD behaviors discussed in the previous section. However, the conventional passive component modeling methods fail to simulate the nonlinear behaviors, as they only provide monotonic buck regulator behavior. From the simulation results, it is expected that the measured peak-to-peak jitter can be estimated by using the switching and continuous time modeling methods. Finally, the overall comparisons between the measured and simulated total PSIJ caused by buck regulator behaviors are summarized in Table IV. Obviously, the smallest errors between measurements and simulations are observed for the first two buck regulator modeling methods. From this analysis, the single-ended buffer connected to the buck regulator circuit can be significantly affected by the conduction noise created by the buck regulator behavior. Thus, appropriate strategies must be taken to handle the PSIJ injected by a buck regulator. In addition, depending on the purpose of the PI analysis, suitable buck regulator modeling methods must be selected to simulate the system's performance in terms of PSIJ.

In this context, a straightforward method to estimate PSIJ caused by the buck regulator is introduced here. In this analysis, the PSIJ is estimated by combining the measured peak-to-peak voltage and dc jitter sensitivity. To assess the PSIJ introduced by the buck regulator, the jitter sensitivity of the victim inverter chain is simulated as shown in Fig. 28. As the jitter sensitivity in both magnitude and phase are constant within the frequency

TABLE IV
OVERALL COMPARISON OF BUCK REGULATOR MODELING METHODS FROM THE PERSPECTIVE OF PSIJ

Activated nonlinear buck regulator behavior	Measurement (Pk-pk jitter / Pk probability)	Simulation (Pk-pk jitter / Pk probability)			
		Switching buck regulator model	Continuous time model	4-element RL model	Simple RL model
Phase activation control	94.2ps / 3.41%	94.4ps / 3.76%	94.3ps / 4.09 %	79.9 ps / 5.13%	74.1 ps / 4.56%
Load line regulation	82.1ps / 2.79%	82.4ps / 3.16%	82.1ps / 3.17 %		

TABLE V
OVERALL COMPARISON OF PSIJ ESTIMATION RESULTS

Activated nonlinear buck regulator behavior	Measurement (Pk-pk jitter / Pk probability)	Simulation (Pk-pk jitter / Pk probability)			
		Behavior model	Estimation	4-element RL model	Simple RL model
Phase activation control	94.2ps / 3.41%	94.4ps / 3.76%	93.8ps / 3.65%	79.9ps / 5.13%	74.1ps / 4.56%
Load line regulation	82.1ps / 2.79%	82.4ps / 3.16%	82.5ps / 3.17%		

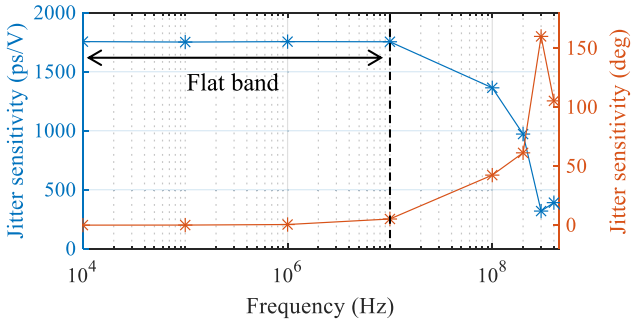

Fig. 28. Simulated jitter sensitivity of victim inverter chain.

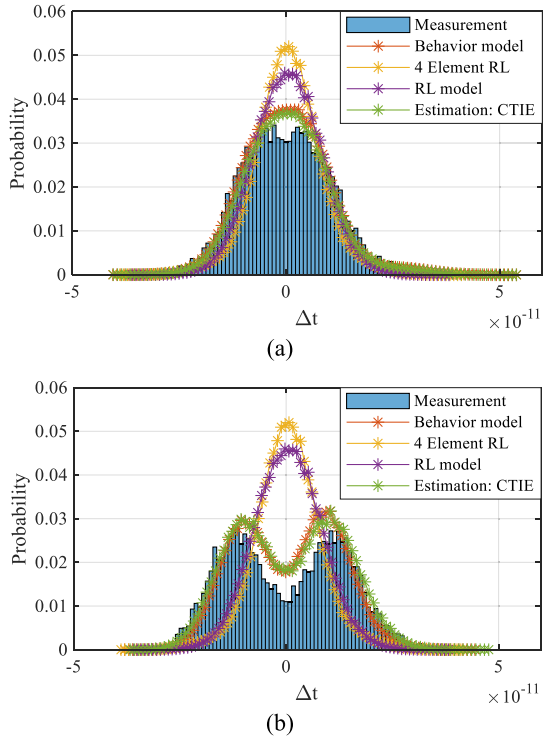

Fig. 29. Simulated PSIJ for each modeling method. (a) Histogram of TIE under phase activation control. (b) Histogram of TIE under load line regulation.

range of buck regulator operation, the jitter extracted from peak-to-peak TIE could be

$$\mathrm{PSIJ}_{\mathrm{pp}} = V_{\mathrm{pp}} \times H(f)_{\mathrm{dc}} \tag{8}$$

where $\mathrm{PSIJ}_{\mathrm{pp}}$, V_{pp}, and $H(f)_{\mathrm{dc}}$ are the peak-to-peak jitter, voltage waveform, and jitter sensitivity in the flat band. Furthermore, the continuous TIE (CTIE) can also be analyzed by simply combining the voltage waveform and dc jitter sensitivity. Fig. 29 presents a comparison of all PSIJ measurements, simulations, and estimation results. The behavior model in Fig. 29 is based on the nonlinear buck regulator modeling method introduced in the previous section. As the estimation method utilizes the measured voltage waveform, the CTIE histogram exhibits a strong correlation with the measurement. To summarize the peak-to-peak jitter comparison, the estimation results are provided in Table V. These numerical comparisons validate the accuracy of the simple PSIJ estimation method, not only for peak-to-peak jitter but also for the CTIE histograms under various conditions.

V. CONCLUSION

In this article, various buck regulator modeling methods were discussed from the perspective of PI and the prediction accuracy of PSIJ. The most widely used conventional methods are passive component modeling methods, such as linear RL and four-element RL models. The linear RL model describes the ampacity of the inductor determined by the voltage as a simple inductor. This model has the advantage of a simple structure but also has the drawback of being unable to isolate low-frequency impedance or damping at the resonance frequency. The next model for solving this limitation is the four-element RL model. With two different RL branches connected in parallel, isolation is guaranteed with this modeling method. Because the passive component modeling methods utilize only a pair of inductors and resistors, the computational

load is greatly reduced. However, the lack of nonlinearity presents a substantial limitation for these modeling methods. To overcome this limitation, behavior modeling methods, such as switching and continuous time models, have been developed. Dual voltage and current feedback loops are implemented in the SPICE simulator based on programable parameters. Thus, the add-on functions of modern multiphase buck regulator features, such as load line regulation and phase activation control, can be implemented in these modeling methods. Consequently, behavior modeling methods provide more accurate simulation results compared with passive modeling methods.

Along with the validation of these buck regulator modeling methods, each buck regulator modeling method was discussed from the perspective of PSIJ. To assess the impact of buck regulator modeling methods on PSIJ, measured and simulated TIEs were compared. This TIE comparison for each buck regulator modeling method showed clearly distinct results. Only behavior modeling methods distinguish a high peak-to-peak PSIJ injected by phase activation and AVP compared to the measurement. This result indicates that one must consider the purpose of the simulation when selecting a buck regulator modeling method. The passive components-based four-element RL model provides good results when the buck regulars operate without a change in the number of phases or operation mode, as shown in Fig. 18. However, if a complex modern buck regulator which has nonlinear add-on functions, such as load line regulation or phase activation, must be included in the system-level PI simulation, the behavior buck regulator modeling methods are the best option for PI engineers.

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