A Novel Vertical Conductive Structure for Printed Circuit Boards and its Scalable Model

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***Abstract*—This article proposes a new vertical conductive structure (VeCS) to replace the general via structure for signal connection on printed circuit boards (PCBs). Vias have been widely used as interconnects for in-between layers in PCBs. However, vias have limitations due to their discontinuous characteristic impedance. The VeCS consists of a conductive structure shielded vertically by a metal structure, which provides impedance control. Thus, the VeCS has the constant characteristic impedance that can get better signal integrity for the high-speed channel than the general via structure. This article also proposes a scalable 3-D electromagnetic simulation model of the VeCS for signal integrity analysis. Simulated annealing and linear regression revealed that the scalable model accurately represents the VeCS. The electrical performances of a VeCS and a via were compared up to 70 GHz. The measured insertion losses at 70 GHz for the VeCS and the via were 35 dB and 70 dB, respectively, because PCB vias exhibit significant reflection loss above 10 GHz. In conclusion, this article proposes a novel vertical interconnection for PCBs.**

***Index Terms*—Interconnect, printed circuit boards (PCBs), scalable model, signal integrity, vertical conductive structure (VeCS), vertical conductor, via.**

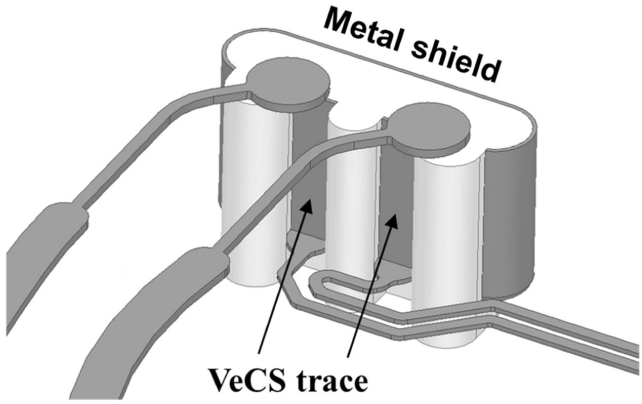

Fig. 1. VeCS has a single- or differential-ended configuration depending on the signal. The VeCS traces are surrounded by a conductive shield.

I. Introduction

HIGH-SPEED serial interface modalities, such as universal serial bus, peripheral component interconnect express, and high-definition multimedia interface, have been continuously revised to satisfy market demands. Furthermore, portable electronic devices, such as smartphones and smartwatches, require such modalities with small form factors. This has led to electronic devices having complicated structures to achieve high performance with limited space [1].

All electronic devices contain printed circuit boards (PCBs) to provide interconnections between components. The PCB consists of conductive traces for horizontal connection and conductive vias for vertical connection. Technical trends have led to PCBs having more traces and vias to achieve high performances in small form factors. Furthermore, data transfer rates have been continuously increased, leading to problems in data transmission. The problems were first observed in electromagnetic compatibility (EMC) [2]. Signal integrity first studied in [3] was defined as the ability of a signal to generate correct response in a circuit. The signal integrity has been studied in four areas: signal propagation on transmission lines, discontinuity modeling, and characterization, measurement techniques, and link-path design and analysis [4]. Thus, the signal integrity (SI) design becomes essential in the EMC [5].

The conductive traces and vias in PCBs are critical in terms of SI, but vias are also critical interconnects in high-performance systems [6]. Vias are fabricated by drilling stacked multilayers to make connections in between layers [7]. A large number of vias were modeled in the multilayer structures for the numerical calculation [8]. A via structure for differential signaling was also introduced in [9]. Due to vertical inhomogeneity, vias have different layer-dependent electrical characteristics. Thus, analytical [10], [11], [12] and empirical formula-based modeling approaches [13] were introduced to analyze and overcome the limitations of PCB vias. In the computational electromagnetics (EM) field, the partial electric element circuit [14] method was proposed for 3-D multiconductor systems [15], and the quasi-static approach was also proposed [16]. Furthermore, the

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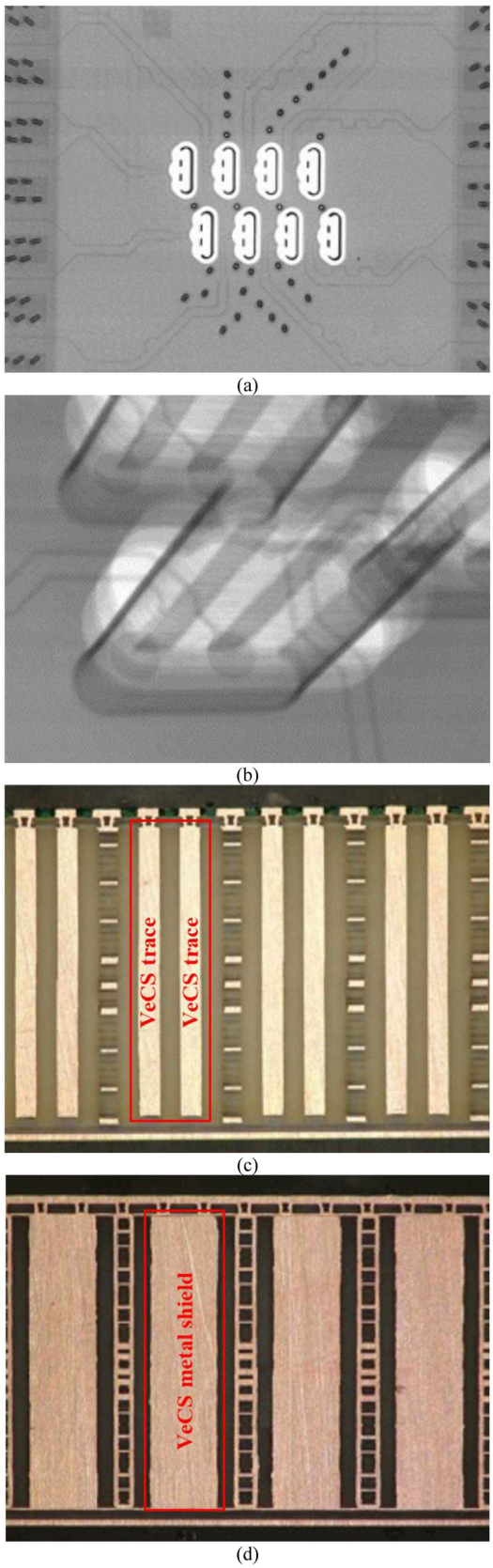


Fig. 2. Fabricated VeCS showing (a) top view and (b) transparent bird's-eye view. From the cross-sectional view, (c) VeCS trace and (d) VeCS shield. The fabricated VeCS has no discontinuity because the traces are surrounded by the VeCS shield.

finite difference time domain [17] and the method of moments approach [19] were introduced.

The 3-D integration silicon integration was introduced in [19], which is based on through-silicon vias (TSVs) [20]. The TSV is advantageous in high density due to its small size [21]. However, the PCB vias and TSVs [19], [20], [21] for off/on-chips have a common problem, i.e., impedance mismatches at the boundaries of different layers that result in significant signal reflections [22]. Therefore, to overcome these limitations, impedance mismatch has to be controlled. The vertical conductive structure (VeCS) is a new technology for PCBs that the impedance can be tuned to match the impedance of horizontal traces and the required impedance [23], [24], [25], as shown in Fig. 1. The VeCS consists of a metal trace in the middle shielded by a metal shield. Also, the VeCS can have many shapes with or without a metal shield. The inner trace refers to the metal shield; thus, the VeCS has no impedance mismatch with signal propagation.

The rest of this article is organized as follows. In Section II, the design of the VeCS is introduced and verified in time and frequency domains. For verification, a PCB via and a VeCS are compared by 3-D full-wave EM simulation. In Section III, a PCB via and a VeCS are fabricated with a test fixture and compared using a vector network analyzer up to 110 GHz. A scalable model for SI analysis of the VeCS is introduced in Section IV. Finally, Section V concludes this article.

II. Design of the VeCS

The VeCS was designed based on 2-D and 3-D full-wave EM simulation and compared with a typical PCB via in time and frequency domains. Because the VeCS has the same cross section along with the signal propagation direction, the VeCS is designed based on the characteristic impedance of the cross section.

A. Two-Dimensional and 3-D EM Simulation-Based Design of the VeCS

The VeCS has either single- or differential-ended conductive structures (depending on signaling) shielded by a conductive metal. Fig. 2 shows top, transparent bird's-eye, and cross-sectional views of the VeCS for differential signaling. As seen in the top view, the VeCS has two traces surrounded by a metal shield. The two lines in the middle represent the VeCS traces, and the bent line represents the metal shield. As can be seen from Fig. 2(a), the VeCS has a smaller area than that of the via. The transparent bird's-eye view shows a connection between the VeCS traces and the microstrip line. In other words, the transmission line is changed from in horizontal to a vertical direction by the VeCS. Fig. 2(c) shows the VeCS traces and Fig. 2(d) shows the metal shield surrounding the signal traces from the cross-sectional view. The four pairs of the differential VeCS traces and the metal shields are fabricated as well. The VeCS has constant characteristic impedance in the direction of signal propagation, so these geometrical characteristics give the VeCS advantages over typical PCB vias in terms of SI.

The VeCS was designed by the 2-D EM simulation (Q2D from ANSYS) based on a characteristic impedance because

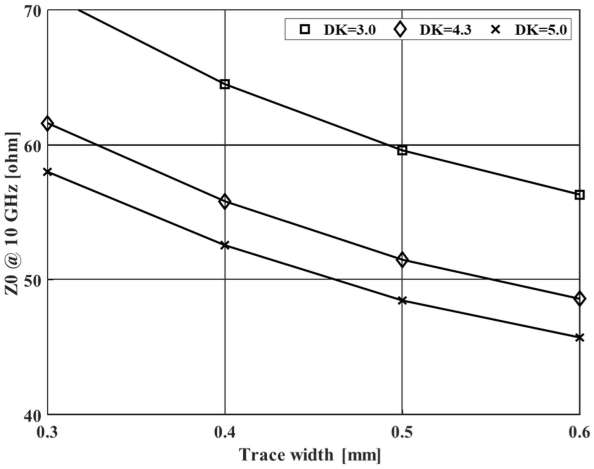


Fig. 3. Simulated characteristic impedance (*Z*0) depending on the VeCS trace width and the *DK* value at 10 GHz.

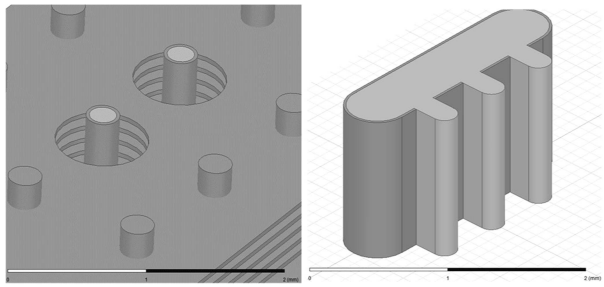


Fig. 4. Full-wave 3-D EM simulation models for the (a) via and (b) VeCS.

TABLE I
MODEL PARAMETERS

Interconnect	Parameter	Value [mm]
Via	Drill diameter (**D**)	0.25/0.20/0.15
	Via clearance	**D**+0.18/0.20/0.22
	Pitch	1
	Height	1.167
VeCS	Trace width	0.3/0.4/0.5/0.6
	Trace thickness	0.02
	Height	1.167

the VeCS has no geometry change in the signal propagation direction. The desirable characteristic impedance is typically either 50- or 100-Ω for single- and differential-ended signaling, respectively. The time-domain reflectometer (TDR) shows the reflected voltage over the incident voltage quotient; thus, the VeCS is designed based on the simulated TDR results. The TDR provides how much the wave is reflected by the characteristic impedance; thus, the change in the characteristic impedance is inferred. Let $p2p(x(t))$ denote a peak-to-peak value for an arbitrary function $x(t)$ in the time domain as follows:

$$p2p\ (x\,(t)) = \max|x\,(t)|\ - \min|x\,(t)|\,. \tag{1}$$

Then, three criteria for the VeCS design are defined as follows:

$$f_1\ (x\,(t)) = p2p\,(x\,(t)) \tag{2}$$

$$f_2\ (x\,(t)) = p2p\left(\frac{\partial}{\partial t}x\,(t)\right) \tag{3}$$

$$f_3\ (x\,(t)) = \int x\,(t)\,dt. \tag{4}$$

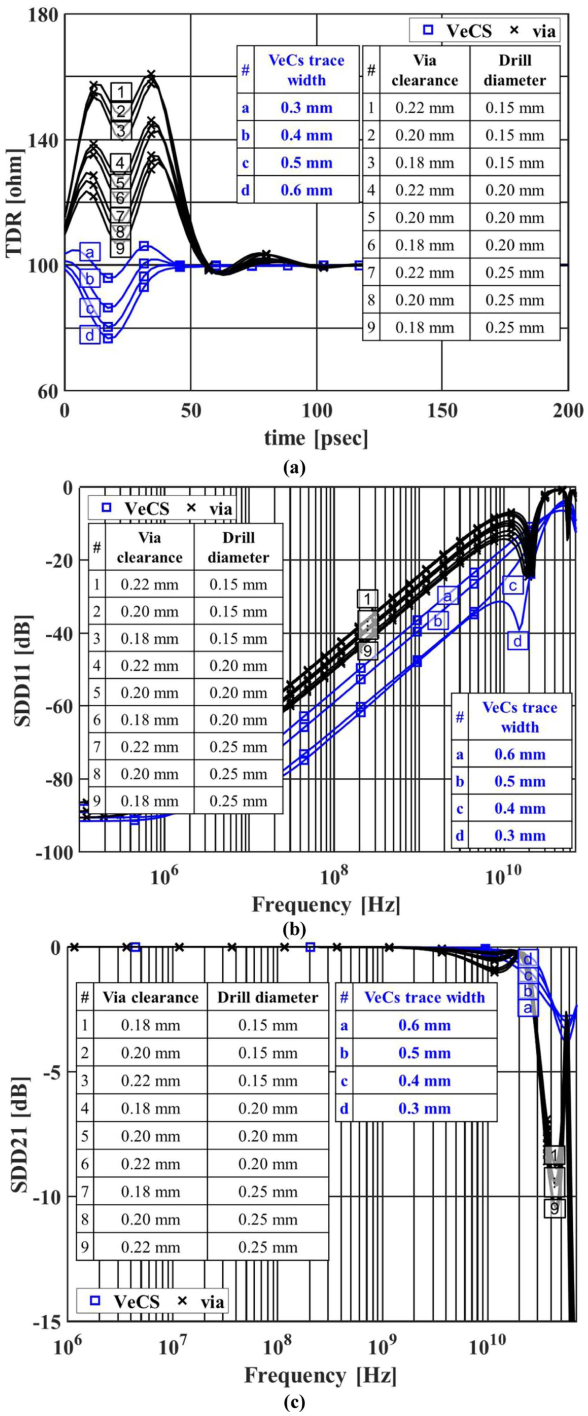
The first criterion $f_1(\cdot)$ shows the difference between the min and max values from the peak-to-peak value of the TDR result. This criterion represents the range of the characteristic impedance. The second criterion $f_2(\cdot)$ shows a slope from the peak-to-peak value of the derivative of the TDR and represents the range of how much the TDR rapidly changes. The third criterion $f_3(\cdot)$ shows an area from the integral for the TDR. This criterion represents how far the characteristic impedance distribution is from the target characteristic impedance. The $x(t)$ corresponds to the TDR response herein.

Characteristic impedance is determined by parasitic capacitances, parasitic inductances, and parasitic resistances. Because parasitic capacitances are determined by the geometry and dielectric constant (*DK*) value, the characteristic impedances of the VeCS that depend on the width and dielectric material can be obtained by 2-D EM simulation, as shown in Fig. 3. When the dielectric material has a lower *DK* value, the characteristic impedance of the VeCS is increased. The parasitic capacitance is proportional to the *DK* value and is inversely proportional to the characteristic impedance. Likewise, the inductance depends on the width of the VeCS. Therefore, the dielectric material in the VeCS and the geometric parameters were considered for the SI design.

B. Comparison With General PCB Vias

The VeCS is intended to overcome the limitations of the general PCB via. Thus, the VeCS and the general PCB via were compared in terms of TDR, differential reflection (SDD11), and differential insertion losses (SDD21). Fig. 4 shows the 3-D models of the general PCB via and the VeCS used for comparison by 3-D full-wave EM simulation. The fabricable design parameters for the general PCB vias and VeCS are shown in Table I. Besides the geometric parameters, other parameters, such as the height and number of layers, were the same to allow fair comparison because height determines the resonance frequency, which affects the return and insertion losses.

A set of fabricable vias was compared to a set of fabricable VeCS in the frequency and time domains, as shown in Fig. 5. The simulated TDR results are obtained by HFSS from ANSYS. An input signal of the step function is applied to the channels to obtain the TDR, and the rise time is 14.28 ps. The rise time is determined based on the solution frequency of 70 GHz in the HFSS. The TDR values for the general vias are distributed from 110 to 160 Ω. In contrast, the TDR values for the VeCSs are distributed from 70 to 110 Ω. Therefore, the via is inductive and the range of the via's characteristic impedances is wider than that of the VeCS. The obtained TDR values are also farther from



#	VeCs trace width
a	0.3 mm
b	0.4 mm
c	0.5 mm
d	0.6 mm

#	Via clearance	Drill diameter
1	0.22 mm	0.15 mm
2	0.20 mm	0.15 mm
3	0.18 mm	0.15 mm
4	0.22 mm	0.20 mm
5	0.20 mm	0.20 mm
6	0.18 mm	0.20 mm
7	0.22 mm	0.25 mm
8	0.20 mm	0.25 mm
9	0.18 mm	0.25 mm

Fig. 5. Electrical performance comparison between the VeCS and via for (a) TDR, (b) differential reflection loss (SDD11), and (c) differential insertion loss (SDD21).

100 Ω compared with those of the VeCSs. Thus, the via has a larger variation and wider range of characteristic impedance compared with the VeCS.

Also, a noticeable difference in end time between the via and the VeCS is identified from the simulated TDR result. The end time of the TDR is determined by the fly time of the input signal. The VeCS and the via have the same dielectric constant and the same height; thus, the difference in the TDR end time is from the reflection. The via has some impedance mismatches, which leads to multiple reflections. The substantial amount of the signal reflection causes a longer end time of the TDR response.

As can be seen from Fig. 5(b), the VeCS always has lower differential reflection (SDD11) loss up to 70 GHz compared with the via. The via has a resonance peak at 20 GHz, but this is caused by its height. The VeCS may have a resonance at 20 GHz; however, the VeCS has no resonance peak in most cases. The resonance may cause unexpected results; thus, it is always undesirable. Therefore, the VeCS has lower reflection loss and a suppressed height-related resonance peak. A lower return loss is strongly required for a short channel. The long channel is affected by both insertion loss and reflection loss; however, the short channel is dominantly affected by the reflection loss.

Fig. 5(c) shows the differential insertion loss (SDD21) for the via and the VeCS up to 70 GHz. The resonance peak identified from SDD11 also affects the differential insertion loss. The via and the VeCS are short; thus, they are nearly lossless up to 1 GHz. However, their dielectric loss becomes dominant from 1 to 10 GHz. The set of vias under the simulation has higher dielectric loss compared with the set of VeCSs in the above range. Therefore, the VeCS exhibits lower insertion loss up to 70 GHz compared with the general via.

The 3-D full-wave EM simulation showed that the VeCS has better performances in terms of TDR, differential reflection loss, and differential insertion loss up to 70 GHz. For the VeCS, reflection is significantly mitigated by the uniform cross section in the signal propagation direction. Because reflection and insertion losses are heavily related, the VeCS improves both losses. Furthermore, the height-related resonances are suppressed in the VeCS. The general via has multiple impedance mismatches, which results in complicated reflections. This leads to unexpected resonances that make it impossible to mitigate the reflection or insertion losses. In contrast, the VeCS has no impedance mismatching. Thus, the VeCS achieves better resonance suppression compared with the via. Therefore, the VeCS has several advantages in terms of impedance mismatching, loss, and resonance.

III. Scalable Model for the VeCS

In this section, a scalable model for the VeCS is introduced for SI analysis. The scalable model represents the VeCS in terms of electrical performance depending on height.

A. Introduction to the Scalable Model

The VeCS is basically a high-speed vertical channel for PCBs. According to the telegrapher's equations, when a high-speed signal is transmitted over a channel, the channel can be expressed by a distributed model consisting of R, L, and C [26]. The distributed model consists of cascaded unit parasitic blocks, and each block has inductance and resistance in series and capacitance in parallel. The introduced model has ten parasitic unit blocks to represent the electrical performance of the VeCS. The number of *RLC* blocks is determined by the height of the VeCS and the wavelength in 3-D EM simulation. The wavelength

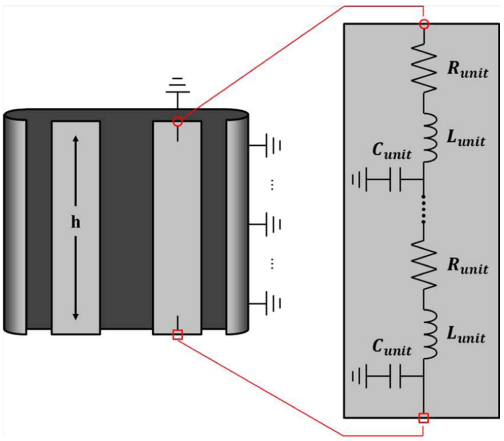


Fig. 6. Distributed scalable model for the VeCS. Each unit block consists of unit resistance, inductance, and capacitance, representing the VeCS depending on the height and distance to the metal shield. Two variables are used to define the scalable model for the VeCS. From the side view, the variable *h* represents the length of the VeCS signal.

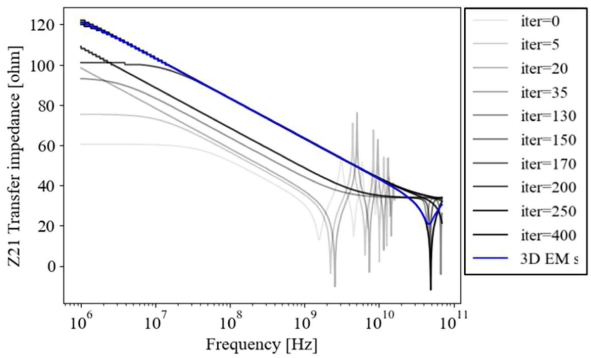


Fig. 7. SA algorithm to find the scalable model for the VeCS. As the iteration number increases, the scalable model reaches nearly the same performance as the 3-D EM simulation.

is determined by the solution frequency, which determines the mesh size in the 3-D EM simulation. The factor for the scalable model is the height of the VeCS signal trace, as can be seen in Fig. 6. Because height determines impedance and insertion loss, it is a critical design factor for the VeCS. The scalable model consists of lumped components with constant values, and the lumped components are cascaded to represent the frequency-dependent behavior, such as the transmission line. The purpose of the scalable model is to establish the relationship between the height and the electrical performances, such as parasitic resistance and resonance frequency. Thus, the scalable model is verified by comparing with the unit *R* and *LC* values depending on the height.

B. Scalable Model Derived by Simulated Annealing (SA) Algorithm

The values for unit resistance, inductance, and capacitance are determined by optimization. The SA algorithm is a random approach to optimize the given problem with a goal. The SA algorithm is well known as an optimizer for highly nonlinear models, chaotic and noise data, and many constraints [27]. The scalable model is a highly nonlinear model and has many constraints; thus, the scalable model was found by the SA optimizer in this study. The goal herein was to minimize the difference between the *Z*-parameters for the 3-D EM simulation and the scalable model for the VeCS. After that, the optimized scalable model would have similar or the same transfer impedance in the frequency domain. Because the *Z*-parameter represents the low-frequency behavior well compared with the *S*-parameter, the goal is based on the *Z*-parameter rather than the *S*-parameter. Thus, each step compares the least mean square values of the *Z*-parameter and finds candidates to obtain better results.

Fig. 7 shows transfer impedance *Z*21 depending on the iteration number by the SA optimizer. As marked in the grayscale, as the iteration number increases, the transfer impedance profile approaches that of the 3-D EM simulation result. When either the goal is satisfied or the iteration number reaches the limit, the corresponding *RLC* values are the scalable model for the VeCS. The above process was repeated for the VeCS heights 1.10–1.20 mm at a resolution of 0.1 mm. The limit for the iteration number was 1 K because the optimized models have saturated transfer impedance profiles when the iteration number is close to the limit.

The optimized results from the SA algorithm are shown in Fig. 8. The solid black lines represent the unit resistances, inductance, and capacitances depending on the given variable. When the VeCS height has values from 1.10 to 1.20 mm, the parasitic resistance is proportional to the height, as shown in Fig. 8(a). The *LC* resonance frequencies are identified by multiplying the inductance and capacitance, as can be seen from Fig. 8(b), because the parasitic inductance and capacitance do not clearly show the behavior depending on the height. Unlike the resistance, the inductance and capacitance have highly nonlinear behaviors, which makes it difficult to find a scalable model. Thus, the parasitic resistance and *LC* values are proportional to the VeCS height. In other words, the VeCS has a higher resistance value and lower resonance frequency.

To generalize the VeCS in terms of the height, linear regression was applied. Linear regression provides an equivalent linear expression for the given dataset [28]; thus, any dataset can be explained with a simple linear equation. The results are shown as the black solid line with square markers in Fig. 8. The parasitic resistance and *LC* values show linear relationships with VeCS height, and the linear regression provides linear equations

$$R_{\text{unit}} = 0.47 \cdot h + 0.0705 \tag{5}$$

and

$$L_{\text{unit}} \cdot C_{\text{unit}} = 1.325 \cdot h - 0.4333. \tag{6}$$

The relationships between the height h and the parasitic unit resistance R_{unit}, inductance L_{unit}, and capacitance C_{unit} are explainable with the above equations. Therefore, for any VeCS height value, the parasitic resistance and resonance frequency are calculable without the 3-D EM simulation program. In conclusion, the introduced scalable model provides efficient and accurate SI analysis for the VeCS.

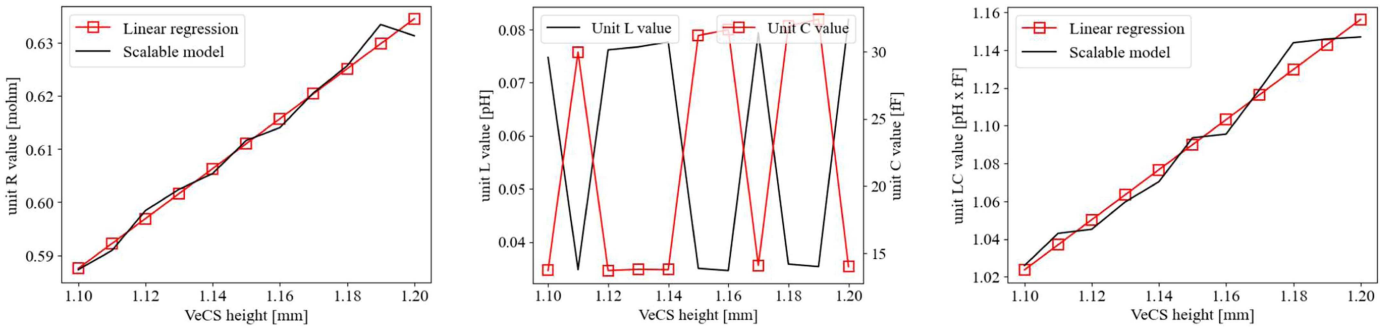


Fig. 8. Unit values for resistance, inductance, and capacitance depending on the height and distance between the VeCS trace and shield. The black line and black line with square markers represent the 3-D EM simulation and linear regression result, respectively.

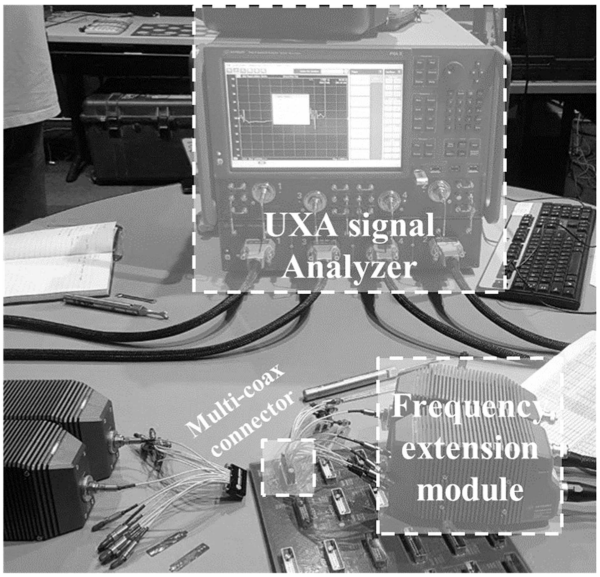


Fig. 9. Measurement setup for the comparison between the PCB via and the VeCS.

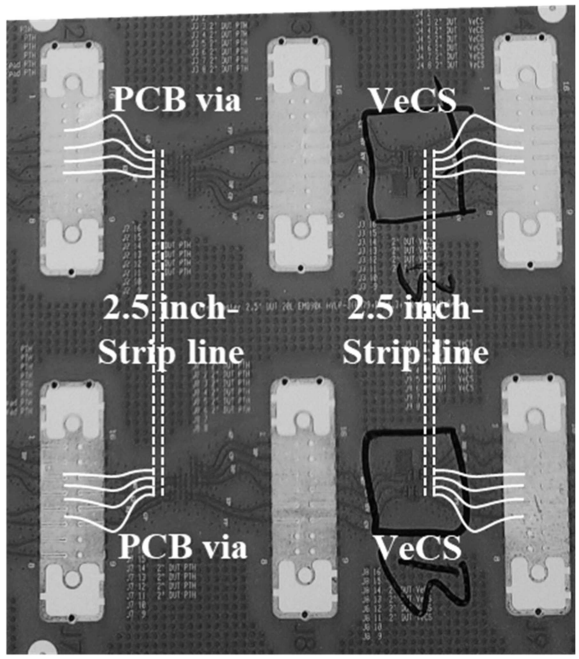


Fig. 10. Test vehicle used to compare PCB vias and the VeCS.

IV. Measurement Results for the VeCS and PCB Vias

The VeCS and PCB via were compared in terms of single-ended and differential insertion losses up to 70 GHz.

A. Test Vehicle for the Measurement

Fig. 9 shows the measurement setup, which consists of a KEYSIGHT UXA signal analyzer, a multicoaxial connector, and a frequency extension module. The extension module is used to increase the bandwidth of the signal analyzer. The connector is used to obtain accurate results by establishing a connection between the measurement instruments and the test vehicle. The test vehicle includes a 2.5-in metal trace between the vertical channel under test. In other words, the signal is transmitted over a channel, including a microstrip line, a VeCS, a 2.5-in strip line, a VeCS, and a microstrip line. The PCB via also has the same test channel, as shown in Fig. 10.

B. Measurement Results for the VeCS and PCB Vias

Single-ended and differential insertion losses were measured up to 70 GHz using the measurement setup, as shown in Fig. 9. Fig. 11 shows the measurement results for the VeCS and the PCB vias. Compared with the simulation results, the losses are significantly increased due to the strip line. The length of the strip line is 2.5 in; thus, most of the losses come from the strip line. Because the VeCS and PCB vias were measured under the same conditions, the difference in insertion loss was identified above 10 GHz. Single-ended reflection losses S11 and S33 for the PCB vias are higher over 10 GHz, and the single-ended and differential insertion loss is also higher. As discussed, the via exhibits impedance mismatching, which results in significant reflection loss in high-frequency regions. Therefore, the VeCS successfully provides vertical interconnection with less signal reflection and insertion loss above 10 GHz.

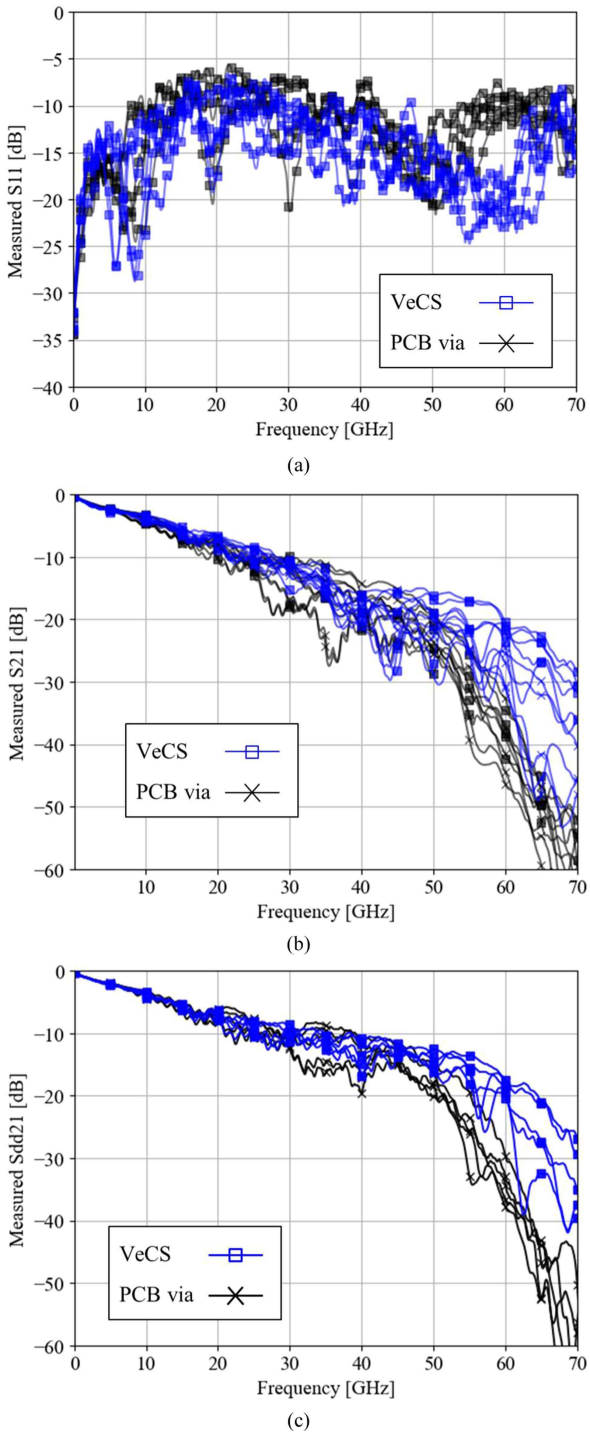


Fig. 11. Measurement results. (a) Single-ended reflection losses and (b) single-ended insertion losses above 10 GHz showing that the VeCS improves the SI. (c) Differential insertion loss, showing the same trend.

V. Conclusion

This article introduces a VeCS that overcomes the limitations of general PCB vias. Because the VeCS has no discontinuity in the vertical plane, it exhibits better electrical performance than the PCB via. PCB vias and the VeCS were compared in the time and frequency domains. The set of fabricable VeCS showed better TDR, differential reflection, and insertion losses up to 70 GHz compared with the set of fabricable PCB vias. Furthermore, a scalable model for the VeCS was also developed using the SA optimization algorithm. The proposed scalable model provides the accurate SI analysis. The reflection and insertion losses were also evaluated up to 70 GHz. In both the simulated and measured results, the VeCS shows better electrical performance compared with the PCB vias. Therefore, this article successfully introduces the VeCS and its scalable model.

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