Investigation of Voltage Regulator Module (VRM)-Induced Noise to High-Speed Signals With VRM via Design Factors

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***Abstract*—As the complexity of server platforms increases, the noise produced by switching voltage regulator modules (VRMs) is more likely to be coupled to nearby high-speed traces. This study aims to investigate the mechanism of noise coupling between the noise generated by a VRM and a high-speed signal trace, as well as to evaluate various noise-reduction methods. A VRM's rapid switching of field effect transistors generates an unintentional coupling region that primarily injects noise into high-speed traces routed in the inner signal layers of the printed circuit boards (PCBs) in server platforms. To analyze various VRM noise coupling mechanisms in practical high-speed channels, a simplified PCB design based on a high-speed server platform is designed and fabricated. In addition, case studies are conducted under various conditions to validate the most efficient VRM noise coupling reduction method by both simulation and measurement. Finally, various design factors that influence VRM noise coupling are evaluated to propose guidelines for high-speed channel designers. This study presents the first comprehensive analysis of different noise coupling mechanisms and an IR drop aware guideline to reduce noise in dense high-speed systems containing a VRM.**

***Index Terms*—High-speed signal trace, noise-coupling mechanism, printed circuit board (PCB), server platform, voltage regulator module (VRM).**

I. Introduction

With the increasing demand for high data rates in modern electronic devices, numerous modulation techniques have been developed in recent decades. Among the number of modulation techniques for high-speed digital communication, the nonreturn to zero (NRZ) is one of the widely used techniques developed to achieve a high and better bandwidth, bit error ratio (BER), and power efficiency, making it suitable for various modern applications. Recently, four-level pulse amplitude modulation (PAM-4) has emerged as a viable option for high-speed digital systems. These modulation techniques, along with their corresponding data rates and applications, are summarized in Table I [1]. The EHmin and EWmin represent the minimum eye height and minimum eye width, respectively. In this comparison, the smaller allowed EHmin/EWmin requires a smaller noise margin. With the technical advancement of high-speed digital communications, the noise margins with respect to voltage and time have become stringent to a few millivolts and a few picoseconds. Therefore, achieving a low-noise environment in highly integrated electronic devices is critical.

TABLE I
Data Rates and Noise Margins for Different Modulation Techniques

Data rate	Application	Modulation	EHmin/EWmin
1 Gbps	Ethernet	NRZ	250 mV/400 ps
2.5 Gbps	PCIe Gen1	NRZ	175 mV/310 ps
5 Gbps	PCIe Gen2	NRZ	120 mV/80 ps
8 Gbps	PCIe Gen3	NRZ	25 mV/37.5 ps
16 Gbps	PCIe Gen4	NRZ	15 mV/18.75 ps
32 Gbps	PCIe Gen5	NRZ	15 mV/9.37 ps
64 Gbps	PCIe Gen6	PAM-4	6 mV/3 ps
128 Gbps	PCIe Gen7	PAM-4	2 mV/1.5 ps

Multiphase voltage regulator modules (VRMs) are commonly used in modern server platforms to supply stable power to high power consumption circuits, such as the central procession unit (CPU) and random-access memory (RAM). However, the switching nature of VRMs generates high-frequency noise [2]. The upper/lower side field-effect transistors (FETs) in each phase of a multiphase VRM are alternately switched ON and OFF, resulting in ringing voltages at the transition edges of voltage and current due to package and interconnection parasitics. The noise frequency generated by a VRM can be a few hundred MHz, allowing it to couple to other devices [3], [4].

With the increasing integration levels of modern server platforms, the design and analysis of power distribution networks (PDNs) associated with VRM noise coupling are becoming increasingly critical. Therefore, power noise coupling through PDN structures to victim circuits has been extensively studied.

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A. Via-to-Via Noise Coupling

Among the electromagnetic interference (EMI) issues caused by VRM switching noise, noise coupling through vertical-to-vertical structures is introduced in [3] and [5]. In [5], the VRM-induced pollution region is identified around the victim vias, and the coupling is characterized by extracting the S-parameters from the VRM PDN to the victim vias. In contrast, the authors in [3] discussed the coupling through the current loop formed by the connector signal pins. The pin structure acts as a small loop antenna that captures the noise generated by the VRMs.

B. Radio Frequency Interference

Another way of modeling noise coupling is through near-field radiation/scanning methods [6], [7]. These methods involve field scanning to detect the dominant noise source of the VRM circuitry and analytical coupling expressions. Based on experimental results, a radio frequency interference (RFI)-perspective VRM noise mitigation method is proposed.

Recently, complex noise coupling paths in highly integrated printed circuit boards (PCBs) have started to be characterized using full 3-D simulators. In [8], the extracted PDN from the 3-D model was combined with the spice VRM to simulate the noise coupling while in [9] and [10] the noise current was directly imported to the 3-D simulator to predict the VRM pollution.

C. Via Transition

Another possible noise coupling through the PDN to via or via to PDN has been analyzed [11], [12], and the results indicated that avoiding the via transition would minimize VRM switching noise coupling. In [13], the via-to-via coupling is analyzed based on the wave propagation, and the equivalent circuit model and segmentation method are used to predict the PDN noise coupling in [14] and [15], respectively. However, these previous studies primarily focused on the noise coupling caused by via-to-via and via transitions. In modern server platforms, high-speed signal vias are routed farther away from the VRM, while transmission lines are still routed within hundreds of mils of VRM circuits. Thus, the mechanisms of direct coupling from switching VRMs to horizontal traces must be analyzed.

This article presents an analysis of the coupling of VRM noise to high-speed signal traces from the PDN, using a simplified PCB design based on an actual server platform. To model VRM-switching-noise propagation, a macro model is used to inject high-frequency noise voltage into VRM power planes, while a full-wave simulation is performed to simulate the return currents on the ground planes. Based on the simulation analysis, VRM via-to-transmission line coupling design factors that influence noise coupling are proposed. These proposals are validated by both transient simulations of VRM noise coupling from extracted S-parameter values and measurement data. Furthermore, an optimization of the number of VRM vias is performed as a means to minimize both VRM noise and dc IR drop. Finally, the article proposes and validates the effectiveness of ground shielding vias as a mitigation method for VRM noise coupling.

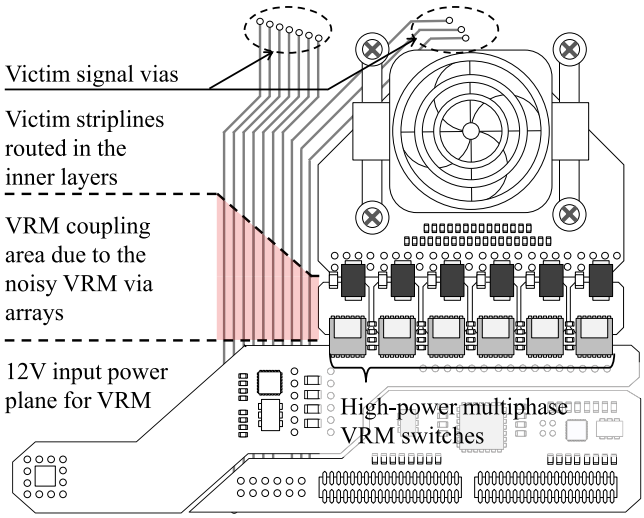

Fig. 1. Complex server platform includes components from small decaps to the CPU.

Overall, the results of this study demonstrate the importance of proper VRM noise coupling design and optimization in highly integrated electronic devices.

II. VRM Noise Radiation

The VRM noise coupling mechanism in a server PCB is investigated in [16]. For completeness, the noise coupling is briefly introduced in this section. The board design of a server system with a noisy VRM and victim transmission line is shown in Fig. 1. The victim signal vias are located as far as possible from the VRM circuitry to avoid via-to-via noise coupling. However, the high-speed traces are still routed around the VRM (highlighted in red). To investigate the mechanism of noise coupling between the VRM circuitry and traces, an equivalent circuit for a VRM generating a switching noise is also created.

According to the proposed circuit, the noise is mainly created by package and PCB interconnects and dissipated through the turned-OFF low-side FET. In [16], the effect of noise coupling on the microstrip was explained in terms of H-fields. In this analysis, the antipad of the VRM via is found to be the main radiation source, and coupling to the microstrip is extracted through the ANSYS 3-D simulator and applied to the SPICE tool with the equivalent circuit of the VRM. The VRM noise coupling to the microstrip is well simulated and one of the PCB design rules is validated. However, this analysis focuses on the microstrip transmission line, while most high-speed traces are routed in the inner signal layer. Thus, the VRM-to-stripline structure needs to be analyzed.

The stripline routed in the inner signal layer around the VRM via is shown in Fig. 2. Since the VRM noise is circulated from the VRM input plane to the ground (GND) on the top layer, the inner signal layer can only be interfered with by the power VRM via and its antipad on the GND plane. Thus, the noise coupling mechanism can be explained by two different factors: 1) VRM via transition and 2) leaked return current through the antipad. The vertical current on the VRM via surface can generate weak

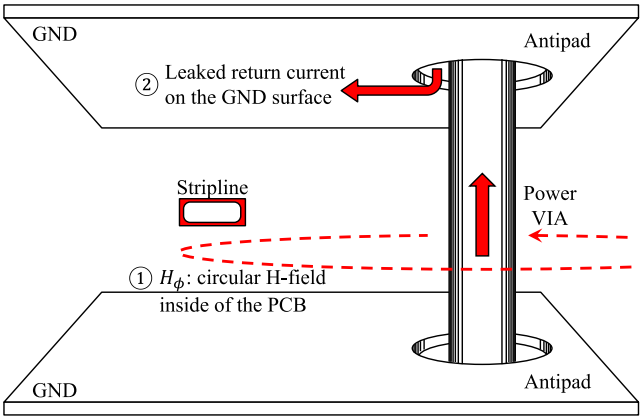

Fig. 2. Stripline routed on the inner signal layer at some distance from the power via.

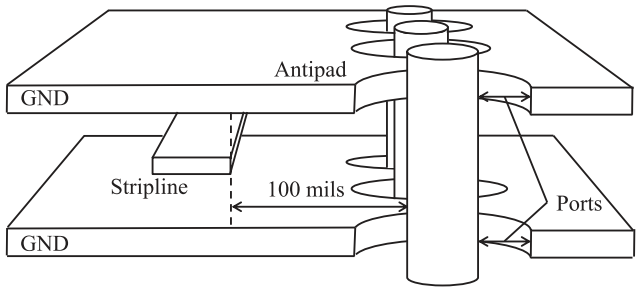

Fig. 3. VRM via radiation simulation.

circular H-fields inside the inner signal layer. This H-field is parallel with the stripline and can inject the current on the surface of the conductor of the stripline. However, the leakage current on the GND plane can also inject the VRM noise when the leakage current returns to its source in the same direction as the stripline. Therefore, to clarify the main troublemaker of VRM noise coupling, the contribution of the above two factors is simulated separately.

A. VRM via Radiation Effect

The coupling from power vias to nearby traces is analyzed in [17]. According to this analysis, the circular field generated by a via can inject weak current onto the surfaces of striplines. To mimic the via radiation, a simulation setup is proposed in Fig. 3. In this simulation, the nonrelevant structures of the PCB are removed. The ports to inject the surface current onto the via are assigned on the top and bottom of the VRM via. The victim stripline is located 100 mils from the antipad of the via, and each end is terminated by a 50-Ω port. In the 3-D simulation, the surface current through the ports on the vertical via is enforced to remove the leaked current on the GND planes.

To check the effect of coupling through via transition, a transient simulation is performed. In VRM noise coupling, the proper circulation of noise through the PDN structure is important. Thus, it would be better to do the transient analysis instead of just comparing the S-parameters. The extracted S-parameters from via ports to stripline ports are applied with the equivalent circuit of the VRM switches, as shown in Fig. 4 [16]. With the

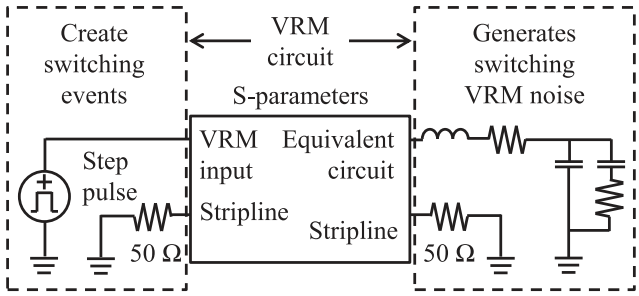

Fig. 4. Transient simulation setup with equivalent circuit and extracted S-parameters.

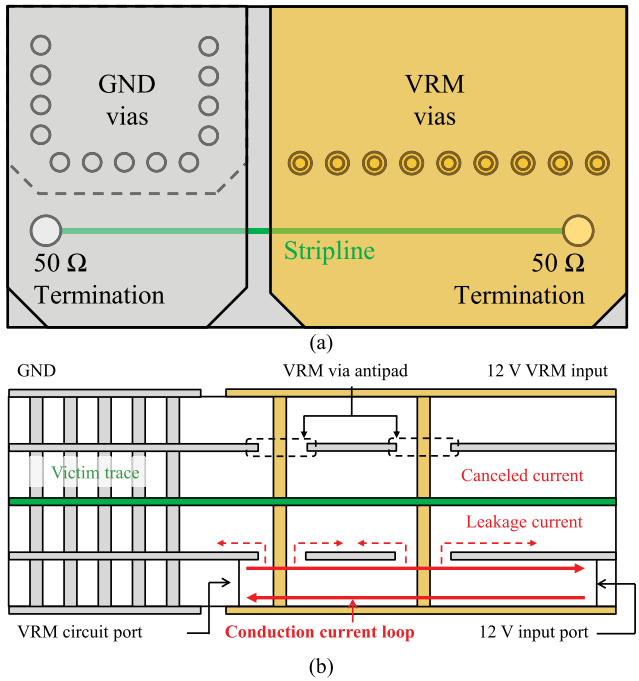

Fig. 5. Proposed 3-D model of VRM noise coupling to trace. (a) Top view. (b) Side view and expected conduction current path.

transient analysis setup, the coupled noise in the time domain is simulated and compared with the surface return current effect.

B. Surface Return Current Effect

To analyze the impact of leakage current on the nearby stripline noise coupling, a new simulation setup is proposed, as shown in Fig. 5. [17]. The proposed board design contains a VRM power plane on the top layer and an internal signal layer surrounded by GND planes. Since the VRM noise is generated and dissipated by VRM input and equivalent model, the two VRM-associated ports are assigned between the VRM plane and GND. To remove the via transition simulated in the previous section, the surface current is only returned to the GND plane through the ports between VRM and GND planes. Since the noise generating ports are applied on the bottom layer, the main current loop is formed on the bottom, and minor current leaks to the GND plane through the antipad of the VRM via. The expected surface return current on the main loop and minor leaked current are shown in Fig. 5. Based on the current distribution,

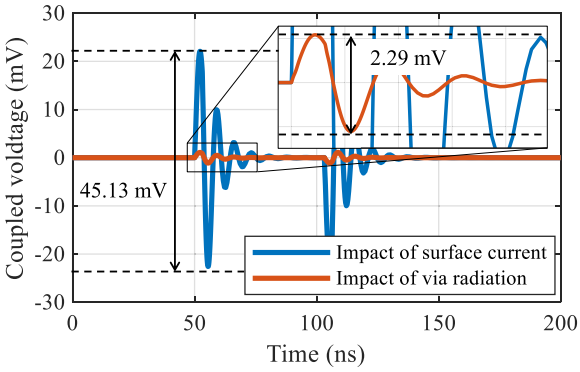

Fig. 6. Transient voltage analysis results for via radiation and conduction current.

it is expected that the return current can be leaked through the antipad and sprinkled out toward the noise source. As explained above, the S-parameters of VRM noise coupling are extracted and applied to the same transient analysis setup to check the numerical results.

The results for noise coupling due to the VRM via radiation and surface leakage current are shown in Fig. 6. The same equivalent circuit ensured identical noise generation, but the amounts of coupled noise voltage are different. Even though the same noise is generated in the two different setups, it is clearly shown that the effect of VRM via radiation is smaller than the leakage current effect. Thus, it is confirmed that the leakage current is the main contributor to the VRM-via-to-trace noise coupling in general PCB designs. Therefore, a rigorous analysis of VRM noise coupling in server PCBs in terms of leakage current through the antipad is required.

III. Parameter Analysis of VRM Noise Coupling

In previous studies, the coupling of VRM noise to high-speed traces has been analyzed using 3-D and 2.5-D full-wave simulations to extract S-parameters or equivalent circuit models of PCB layouts. In this study, we propose several 3-D models based on an actual server platform with various VRM related PDN designs to evaluate and compare their effectiveness. The objective of the proposed simulation models is to identify the factors that may affect VRM noise coupling.

The target complex server platform includes all components from small decoupling capacitors to large CPUs, as depicted in Fig. 1. However, running such simulations on large server boards can be computationally intensive. To address this issue, a simplified PCB design based on a practical server platform is proposed for multiple design analysis. Previous studies have primarily focused on localized PDNs in close proximity to VRM planes and vias. Similarly, in the proposed simplified PCB design, the potential VRM pollution area is localized around the MOSFET switches of the VRM. The simplified design comprises a VRM noise coupling region in the signal layers with a five-layer stack-up of Top–GND–SIG–GND–Bottom layers. A stripline that is routed near the edge of the VRM power via's antipad is used as the victim of VRM noise coupling. Fig. 7 depicts the layout of the inner signal layer from the practical server design

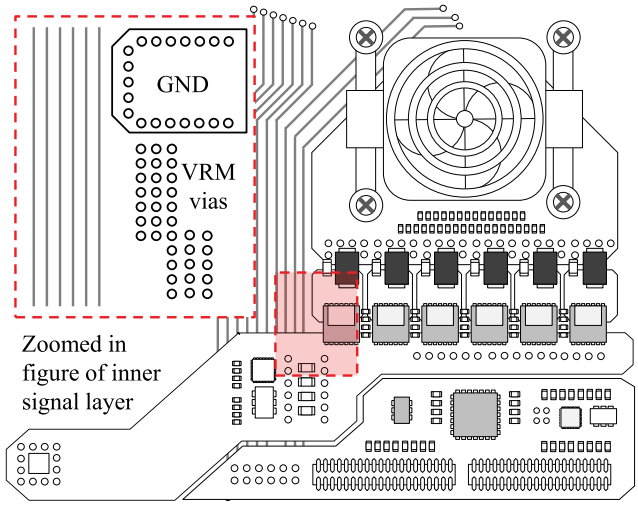

Fig. 7. Victim transmission line routed in the inner signal layer of the practical server platform.

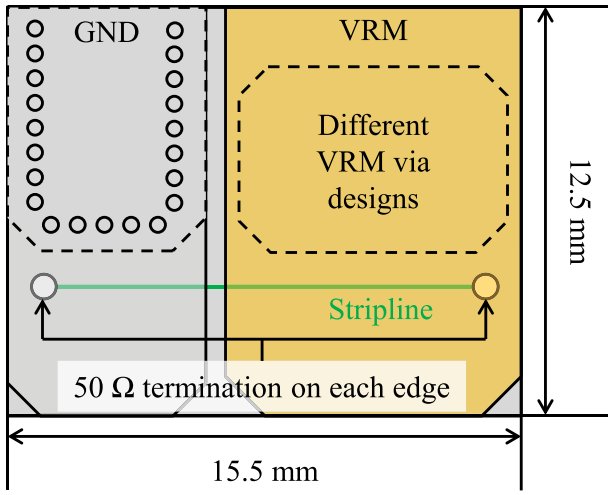

Fig. 8. Proposed simplified PCB design with different VRM via designs.

around the noisy VRM vias. Based on this practical design, the proposed 3-D models with different VRM via designs are shown in Fig. 8.

In the proposed design, the ports to mimic the VRM input voltage and equivalent model are assigned on the bottom layer to remove the interlayer via transition. As a result, the main current loop can be formed, as shown in Fig. 5. However, there are still some possibilities for the conduction current to leak to the upper surface of the return plane through the antipads of VRM vias. This conduction current can inject noise voltage onto the victim stripline, resulting in corrupted signal quality. Thus, the analysis and optimization of VRM noise coupling and VRM via designs must be carried out. In this section, case studies are performed to identify the design factors that have a significant effect on noise coupling. Then, the impact of each case in time domain simulation will be discussed later in this section. The design factors of VRM vias that have a significant effect on the noise coupling are as follows.

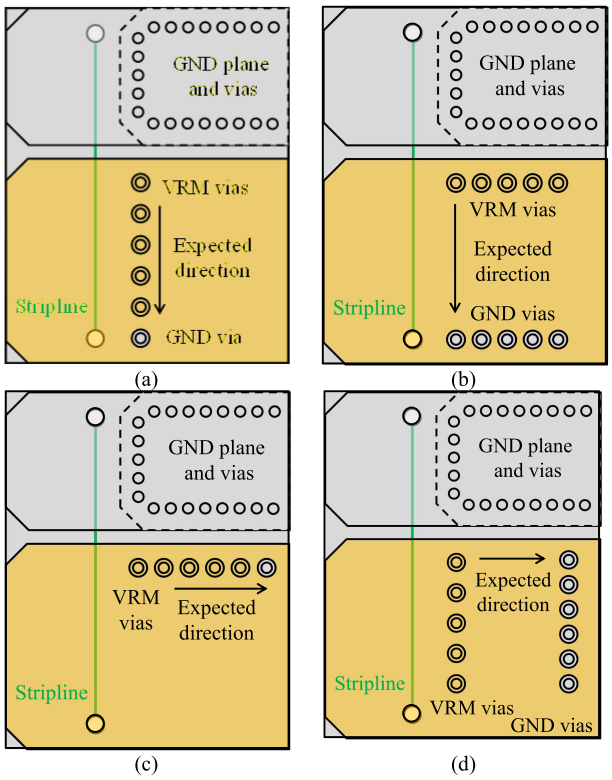

Fig. 9. PCB designs used to simulate the expected return current direction. (a) Jy dominant design #1. (b) Jy dominant design #2. (c) Jx dominant design #1. (d) Jx dominant design #2.

A. Directionality of Return Current

To analyze the directionality of the return current, the conduction path of the current must be clarified. Since the victim trace in Fig. 8 is a straight line, a surface current in the same direction can inject the noise. The simple PCB design to simulate the directionality of return current depends on the VRM and GND via designs, are shown in Fig. 9. In these designs, a victim trace, VRM vias, and GND vias are modeled under the VRM plane. Placing the GND vias under the VRM plane is not realistic, but this is applied solely to evaluate the effect of directionality. For the excitation, the group voltage ports are assigned on the antipads of the VRM vias. Through this design, the surface current is forced to flow in only the x- or y-direction. To evaluate the via designs in terms of directionality, four different PCB designs are simulated. For each direction, VRM vias are arranged in a single row or column with the returning GND vias. Thus, the return current on the GND planes will be formed differently.

The surface return current distribution of each design is shown in Fig. 10. Victim traces that are strongly affected by the VRM current are confirmed in two cases [Fig. 10(a) and (b)]. Even though the VRM vias are arranged along with the trace, if the return current path is formed in a different direction, the VRM noise coupling can be minimized.

To simulate the time-domain noise coupling, the S-parameters of the simple PCB designs are extracted. In this extraction, the victim trace is routed 100 mils away from the noisy VRM vias. The transient analysis results with the simulation setup shown

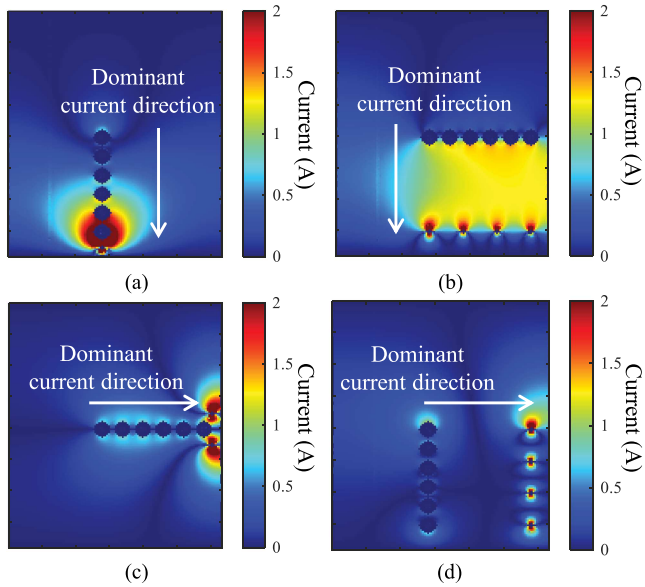

Fig. 10. Jy current distribution on the return plane. (a) Jy dominant design #1. (b) Jy dominant design #2. (c) Jx dominant design #1. (d) Jx dominant design #2.

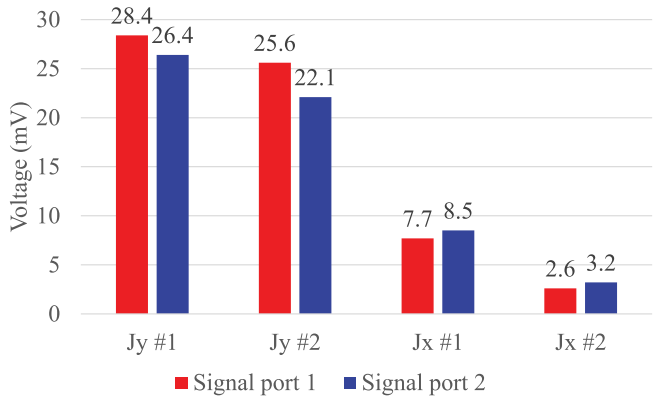

Fig. 11. Time-domain simulation results for directionality.

in Fig. 4 are shown in Fig. 11. As shown in the surface current distributions in Fig. 10, the coupled VRM noise on the trace can be minimized by forming an appropriate return current path on the return plane.

In addition, this analysis evaluated the conventional "rules of thumb" in VRM via design. Typically, it is recommended to avoid the VRM via array along with the victim traces. However, the coupled noise voltage can be reduced by applying the return path nonrelevant with the direction of inductive coupling.

On the basis of this analysis, the directionality of return current must be considered carefully during the early stage of board design.

B. Radius of Antipad for VRM via

In high-speed signal via design, a large shared antipad for negative and positive channels is traditionally used [19]. This is because the reduction of discontinuity is the most important engineering factor in high-speed signaling. To maintain a consistent characteristic impedance of 100 Ω for differential traces, it

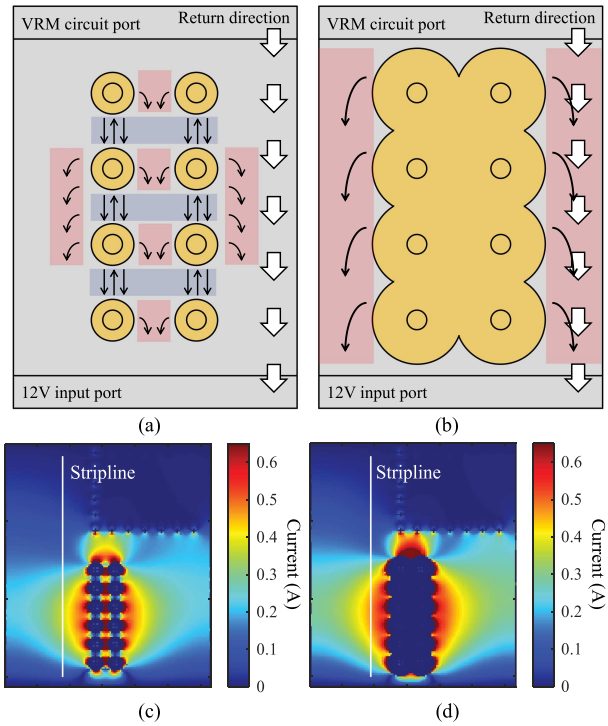

Fig. 12. Top view of antipad design and current. (a) Expected surface current canceled and accumulated area. (b) Expected surface current accumulated area. (c) Jy distribution with separated antipads. (d) Jy distribution with shared antipads.

is necessary to minimize the capacitance of the differential vias. This is because any impedance mismatch between the vias and the traces can lead to signal reflections and degradation of signal quality. Therefore, a fine-tuning of the via capacitance ensures that the impedance of the via is as close as that of the traces, resulting in smooth signal transmission without any reflections or losses. In the power VRM via design, the same shared-antipad structure is applied, resulting in a large void on the GND planes. However, the use of a shared antipad for power vias can lead to significant signal integrity (SI) issues.

The top view of the simplified PCB design illustrated in Fig. 12 demonstrates that the leakage current emanates from the antipad sprinkles in all directions and can accumulate or reduce, depending on the current direction, due to constructive and destructive interference. The regions where current accumulates or reduces are shown in red and blue, respectively, in Fig. 12(a). Although most of the leakage current is canceled out in the VRM coupling region, as shown in Fig. 12(c), the use of a large shared antipad creates a stronger VRM noise coupling region, as shown in Fig. 12(d). With the design of a shared antipad, most of the return current is leaked to the adjacent victim trace without cancellation. The existence of a large void on the ground plane impels the conduction path to approach even closer to the victim trace by accumulating the leakage current of each separated antipad, resulting in a larger and more robust coupling region. It is apparent that the magnitude of VRM coupling noise with the shared antipad design is much greater than that for the separated antipad design.

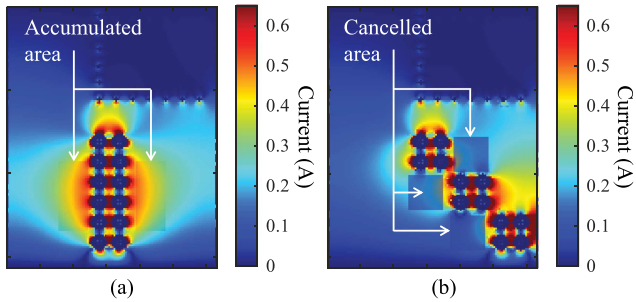

Fig. 13. Different surface current distributions dependent on via array designs. (a) Straight VRM via column design. (b) Patterned VRM via design.

C. Via Array Design

The previous analysis shows that the separated antipad design for VRM power vias can cancel the leakage current. However, the VRM noise coupling is not only solely determined by the antipad design but also by the power VRM via array design. Fig. 13 shows the surface current distributions for different VRM via designs. In Fig. 13(b), a smaller and weaker coupling current region is formed directly below the strong VRM coupling region by the antipads of the second power via array. This region is created because the leakage current dissipates out from the second power via array and cancels out the strong return current in the y-direction. In addition, the optimized via pattern can reduce the leaked current by providing a solid vertical return path in proximity to the power vias; also known as power-ground interleaved via array. Therefore, by using appropriate power via patterns, the leakage current can be canceled out effectively.

D. Via Transition Due to Decoupling Capacitors

In the previous section, it was emphasized that via transitions must be avoided in VRM via design. However, in the case of a complex server PCB, a significant number of decoupling capacitors are placed on the bottom of the PCB for the VRM input plane, while the VRM switches are mounted on the top layer. Such a design can cause an interlayer transition in the conduction path of the return current, leading to significant noise coupling to the victim trace. A conduction path comparison for different decoupling capacitor locations is depicted in Fig. 14. Since a large number of decoupling capacitors are used in a server platform, a high transient current due to the sudden activation of VRM switches is supplied by the decoupling capacitor bank. As a result, the majority of noise generated by switching events will be generated by the decoupling capacitors with via the transition in Fig. 14(a). Conversely, when the decoupling capacitors are mounted on the same layer as the VRM switches, the majority current loop will still be created on the top layer, resulting in low noise coupling. Therefore, the location of decoupling capacitors plays a crucial role in VRM noise coupling to traces.

Fig. 15 illustrates the surface current distribution on the GND plane, which varies with the location of the capacitors. The simulation results demonstrate a strong return current when via transition is forced due to the capacitors in Fig. 15(b). However, a weak surface current is simulated in Fig. 15(a), where there is no via transition due to the decoupling capacitors. Thus, based

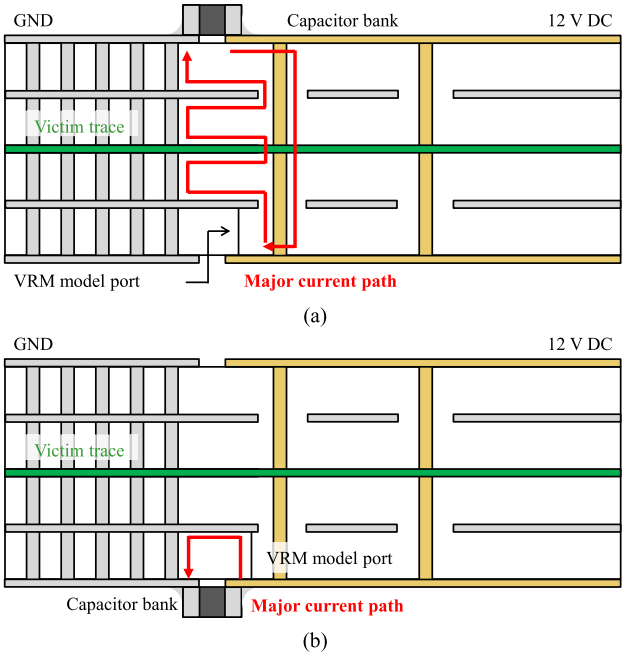

Fig. 14. Conduction path comparison depending on the decoupling capacitors. (a) Via transition due to the capacitors. (b) Minimized current loop.

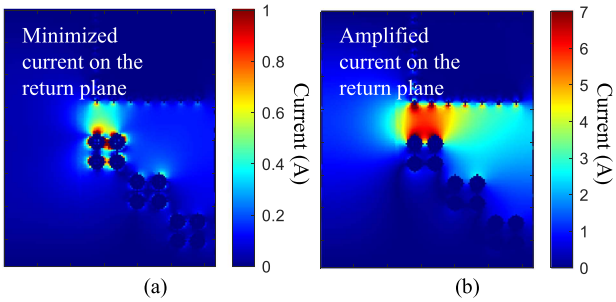

Fig. 15. Surface current on the return plane depends on the decoupling capacitors. (a) Minimized current with the capacitors on the same layer as the VRM switch. (b) Amplified current due to the via transition.

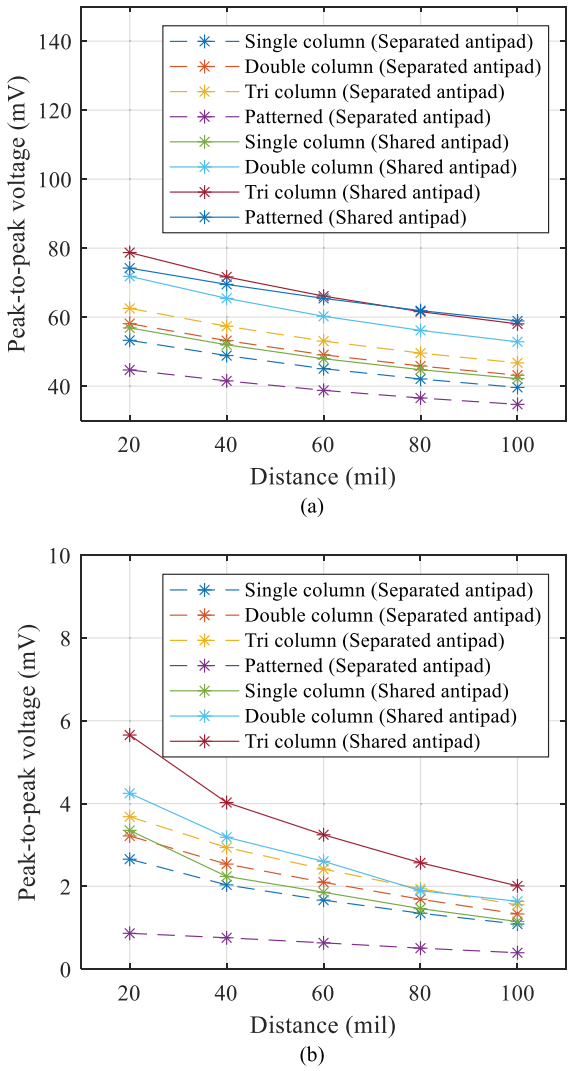

Fig. 16. Peak-to-peak coupled voltages on the victim trace. (a) Single-ended transmission line case. (b) Differential line case.

on these findings, the VRM noise coupling to nearby victim traces can be minimized by carefully selecting the location of the decoupling capacitors.

In this study, four design factors have been investigated to evaluate their effect on VRM noise coupling: 1) directionality of return current, 2) radius of antipad for VRM via, 3) via array design, and 4) via transition due to decoupling capacitors. However, VRM via arrays designed without considering the return current directionality and that have large shared antipad are still used in conventional VRM via configurations.

To evaluate the effectiveness of VRM via designs, a transient simulation is performed. For the transient simulation, the equivalent VRM model in [18] is combined with the S-parameters of 3-D models analyzed in Section III-A and III-D. Both single-ended and differential transmission lines are simulated as the victim traces. It has already been reported [18] that the number of power via columns has an impact on the VRM via noise coupling as well. In this analysis, the number of via columns is increased from one to three. For all the designed factors for VRM vias, the peak-to-peak voltage of VRM noise coupled on the victim trace was analyzed, and the simulation results are presented in Fig. 16.

Conventional VRM via configurations typically employ a large number of straight vias with a large shared antipad, running parallel to the transmission lines. As illustrated in Fig. 16, the coupled noise voltage associated with this conventional design is characterized by the tri column (shared antipad), resulting in the most pronounced VRM noise coupling. Counterintuitively for via designs, VRM via configurations with separated antipads and patterned via arrays exhibit superior performance in terms of coupled noise voltage.

For the differential transmission line cases, the coupling mechanism is still identical to the single-ended cases. The coupled voltages shown in Fig. 16(b) are in the millivolt or submillivolt range, indicating low noise coupling. However, as the speed of communication increases, the voltage margin becomes tighter, as summarized in Table I, and appropriate VRM via design strategies must be carefully taken to minimize noise

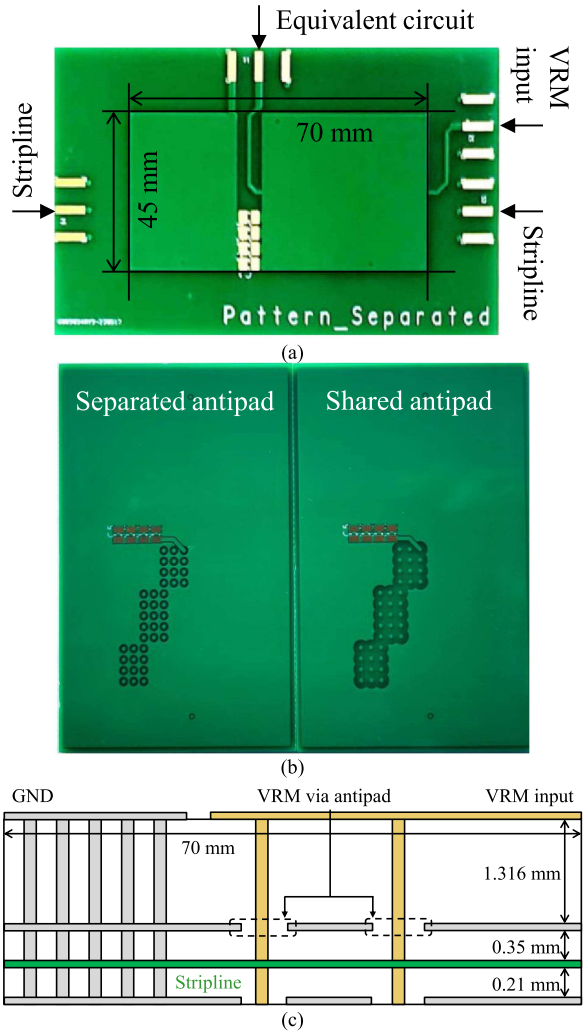

Fig. 17. Fabricated PCB used for validation in this study. (a) Top view of the PCB. (b) Bottom view of the PCB. (c) Side-view and dimensions of the PCB.

coupling. This analysis confirms the effectiveness of counterintuitive via designs as compared to conventional approaches.

IV. Measurement Validation

To further validate the design factors addressed in the previous section, PCBs based on the 3-D simulation structure are fabricated. The mock-up designs for the VRM noise coupling experiments are shown in Fig. 17. Each PCB has a different antipad radius and via array designs for validation of the design factors. As shown in Fig. 17(b), the mentioned patterned via array designs are fabricated with different antipad radii. For the various measurement validation, a single- and three-columns via array with different antipad radii are fabricated as well. The radius of the antipads varied from 30 to 60 mils and the via drill hole size is fixed at 15 mils. FR-4 with different thicknesses is used as the dielectric material. From the top VRM plane to the GND layer, the thickness is designed to be 1.244 mm to minimize the capacitance between them. For the excitation of VRM radiation, two SMA connectors are designed for the top surface of the PCBs. Each SMA connector is connected to the

TABLE II
Difference in Coupled VRM Noise as Affected by via Design in Measurement and Simulation

Via designs	Antipad radius	Measurement	Difference
Multi column	60 mils	77.8 mV	88.6 %
	30 mils	8.8 mV	
Single column	60 mils	67.3 mV	91.5 %
	30 mils	5.7 mV	
Patterned column	60 mils	45.1 mV	91.9 %
	30 mils	3.7 mV	

Via designs	Antipad radius	Simulation	Difference
Multi column	60 mils	85.8 mV	87.2 %
	30 mils	10.9 mV	
Single column	60 mils	76.8 mV	94.6 %
	30 mils	4.9 mV	
Patterned column	60 mils	47.3 mV	94.3 %
	30 mils	2.7 mV	

top VRM plane to create a current loop on the top layer. In the third layer, a 50-Ω transmission line is routed 1-mm away from the antipad of the VRM via. The PCBs are designed with unrealistic dimensions, solely to investigate the effects of via design factors. With the fabricated PCBs, the S-parameters of all four ports from 100 to 500 MHz are measured and applied to the advanced design system (ADS) for circuit simulation. The same VRM macro model shown in Fig. 4 is applied, and the peak-to-peak coupled voltages on the transmission lines are simulated. The transient simulation results with the measured S-parameters are summarized in Table II.

The simulation results confirmed that both design factors have an effect on VRM noise coupling. The larger radius antipads with a large shared antipad always show a higher coupled voltage. In the previous section, the effect of via array designs, such as single to multiple columns and patterned via arrays are validated by simulation. The decreasing trends of peak-to-peak coupled voltages depend on the via array designs validated by measurement as well. The highest coupled voltage is measured for the multiple columns case, and the patterned via array shows the lowest coupled voltages. To double check the decreasing trends in the measurements, the same 3-D PCB models are simulated in high-frequency structure simulator (HFSS). The simulated S-parameters are then applied to the ADS circuit simulation setup to simulate the coupled voltages. The simulation results show the same decreasing trends with similar decrease percentages. Based on the measurements and simulation, the effects of via array designs discussed in the previous sections are validated.

V. Combined High-Frequency and DC Analysis

Based on the simulation and measurement, a smaller number of VRM vias reduces the noise coupling to nearby traces. However, the number of power vias can have tremendous effects on the IR drop of a PCB. Typically, the IR drop is calculated from

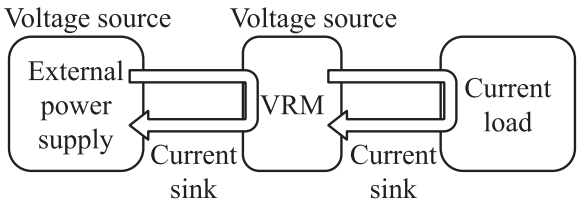

Fig. 18. Current sink and voltage source relationship in black box.

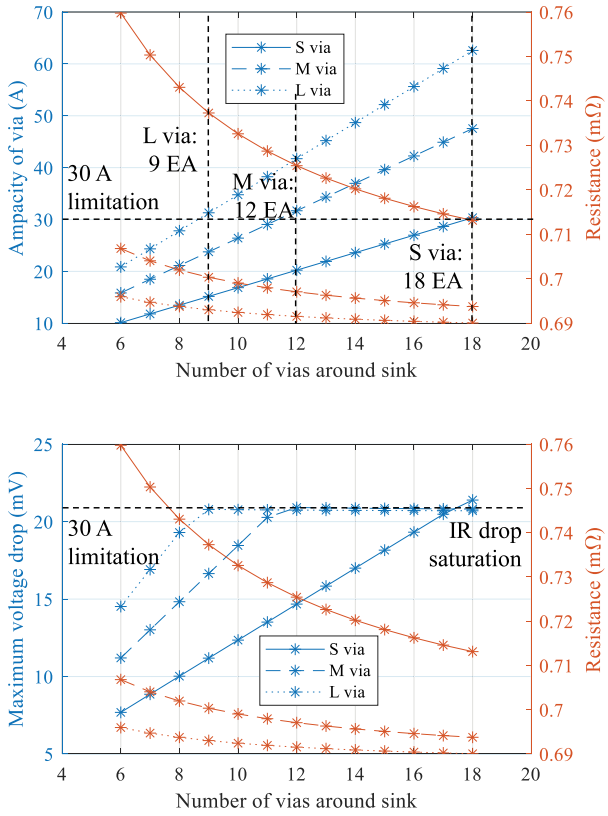

Fig. 19. (a) Calculation of resistance and ampacity. (b) IR drop saturation.

the voltage source to the current sink, which is VRM and current load, respectively. From the perspective of PCB resistance, it is typically recommended to apply power vias around the current sink as much as possible. This rule directly contrasts against the VRM noise coupling because the VRM switches consume the power provided by an external outlet, so could be considered as a current sink, as shown in Fig. 18. As a result, high-speed traces routed in the inner layer could be easily deteriorated by the power VRM vias. Thus, an appropriate design to mitigate both VRM noise coupling and dc IR drop must be performed.

A. DC Resistances for IR Drop and Ampacity Calculation

For the IR drop analysis, the resistance of the vias and PCB plane are calculated. The dc and ac resistances of a via are as follows [20], [21]:

$$R_{\mathrm{DC}} = \frac{1}{\sigma_{\mathrm{copper}}} \frac{L}{\pi R^2} \tag{1}$$

where σ_{copper}, L, and R are the conductivity of copper, length, and radius of copper plating, respectively. From the above equation,

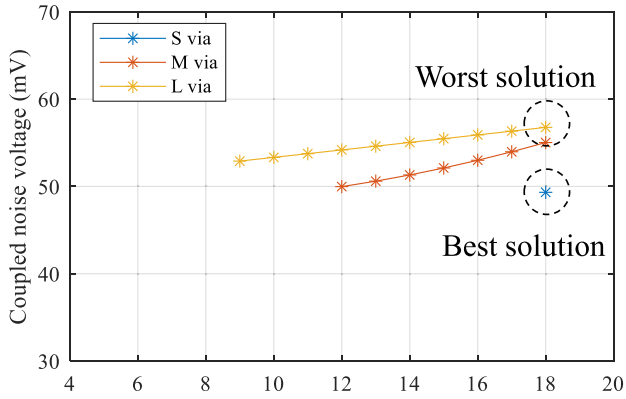

Fig. 20. Best and worst solution of VRM via design with IR drop consideration.

0.15-mΩ resistance of a typical copper through a via with a length of 0.4 mm, radius of 0.15 mm, and plating ratio of 40% can be calculated. The plane resistance of the PCB can be simply calculated by considering the width and thickness of the board as

$$R_{\mathrm{PCB}} = \frac{\rho}{w_{\mathrm{PCB}} t_{\mathrm{PCB}}} \quad [\Omega/m] \tag{2}$$

where ρ, w_{PCB}, and t_{PCB} are the resistivity of copper, width, and thickness of the plane, respectively. Finally, the total resistance of the plane can be calculated as follows:

$$R_{\mathrm{total}} = \frac{\mathrm{LR_{PCB}}\left(\mathrm{LR_{PCB}} + R_{\mathrm{via}}/N\right)}{2\mathrm{LR_{PCB}} + R_{\mathrm{via}}/N} \tag{3}$$

where L and N are the length of the plane and the number of vias around the current sink, respectively. Based on (3), it is apparent that the total resistance will be saturated to half of R_{PCB} when the number of vias is large enough. As a result, it cannot be compared with the high-frequency VRM noise coupling since the resistance and coupled voltage will show the opposite trends against the number of vias. Thus, the ampacity of VRM vias to limit the maximum allowable current is also considered for IR drop estimation.

To calculate the ampacity of a via, the IPC-2221A standard is used. The maximum allowable current per via can be calculated as

$$I_{\mathrm{max}} = k\Delta T^b A^c \tag{4}$$

where k, b, and c are the constants 0.048, 0.44, and 0.725 from IPC-2221A standards and A is the cross-sectional area of a via, respectively. In this analysis, the dc resistance of the simplified PCB shown in Fig. 8 is calculated. The PCB thickness, width, and lengths are assumed to be 0.089, 12.5, and 10.5 mm, respectively, for dc resistance analysis. Three power via designs are considered for ampacity comparison, with diameters of 18, 12, and 6 mils denoted as large, medium, and small vias, respectively, and ampacity values of 3.47, 2.64, and 1.68 A per via, respectively. As discussed in the previous section, the separated antipad design is applied. For simplicity of calculation, VRM vias in a straight column without any pattern are considered. The calculation results for resistance and ampacity are presented

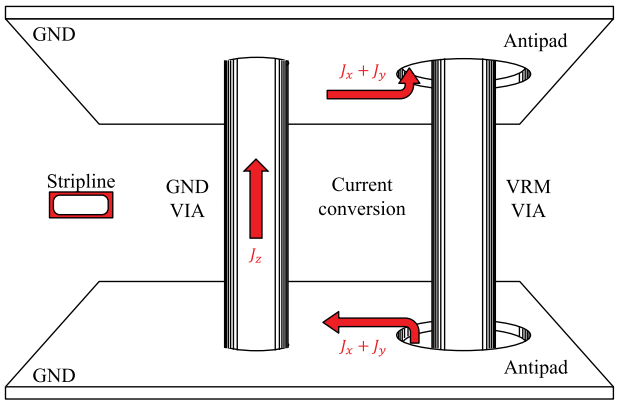

Fig. 21. Inner signal layer with a GND via.

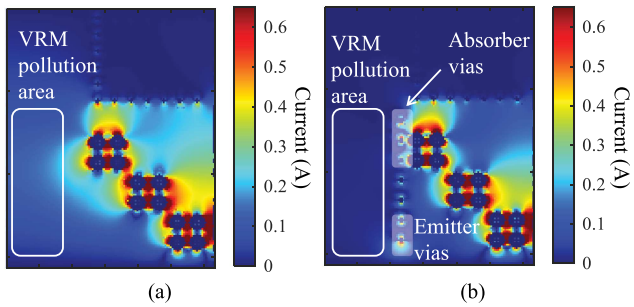

Fig. 22. Current distribution with GND via. (a) Without shielding GND vias. (b) With GND shielding vias.

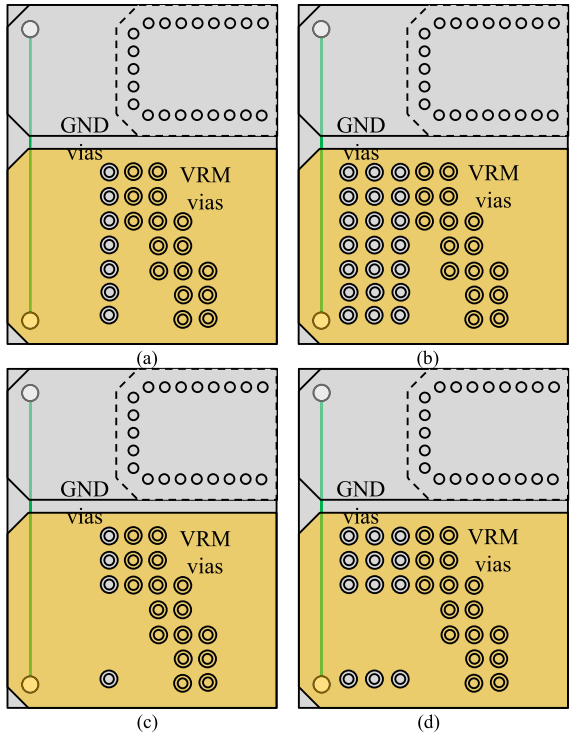

Fig. 23. Shielding test cases. (a) Single shielding via column. (b) Three shielding via columns. (c) Optimized number of vias with single column. (d) Optimized number of vias with three columns.

in Fig. 19(a), with a maximum load current of 30 A assumed for comparison purposes. The analysis reveals that, based on the current limit, at least 18, 12, and 9 vias are required for the small, medium, and large vias, respectively, to carry the maximum current. Moreover, the study shows that the IR drop which is caused by the resistance of the PCB including vias saturates once the maximum current is reached, as illustrated in Fig. 19(b). Thus, the dc IR drop analysis suggests that a large number of vias are unnecessary if the current is bounded, and the optimal number and design of VRM vias can be determined through a comparison with the VRM noise coupling analysis.

B. Comparison Between the VRM Noise Coupling and IR Drop

In this section, the number of VRM vias is optimized by integrating the results from the previous section on dc IR drop analysis into VRM noise coupling analysis. For VRM noise coupling analysis, a single-ended stripline is routed in the inner layer, 100-mils away from the VRM via antipad. VRM via arrays with different numbers of vias and shared/separated antipad designs are used as noise sources, and the required numbers of vias from the previous analysis are applied. Simulation results for coupled voltage with different numbers of vias and designs considering the IR drop analysis are shown in Fig. 20. The separated antipad design consistently yields lower noise coupling than the shared-antipad design. By considering the IR drop results, the optimal design for a 30-A current requirement is 18 small vias with a separated antipad design, while the optimal design for a 25-A current requirement is ten medium-sized vias with a separated antipad design. The analysis results confirm that a smaller number of vias does not necessarily lead to reduced VRM noise coupling to victim traces. The proposed method enables optimization of the power VRM via design to reduce both the dc IR drop and high-frequency noise coupling in the early stage of the development cycle.

VI. Noise Mitigation Method

Even though the VRM noise coupling to victim trace is minimized by following the proposed design factors of VRM vias, the threat of noise is not perfectly eliminated. To meet the noise voltage/timing margins summarized in Table I, additional noise mitigation methods must be performed. In this section, the noise mitigation methods achieved by constructing GND vias around the VRM pollution area are investigated. As an example of shielding GND vias, a typical via wall in PCBs is shown in Fig. 21. In this method, the array of shielding GND vias acts like an electric wall that blocks the radiation from the noisy structures. However, the densely placed shielding vias are not required in VRM noise coupling since the impact of the surface return current is much stronger than the radiated field, as simulated in the section. Instead, providing the alternative conduction path using GND vias for the leakage current is more suitable for this issue.

The use of additional GND vias near the VRM via can help mitigate noise coupling in two ways. First, the GND via converts

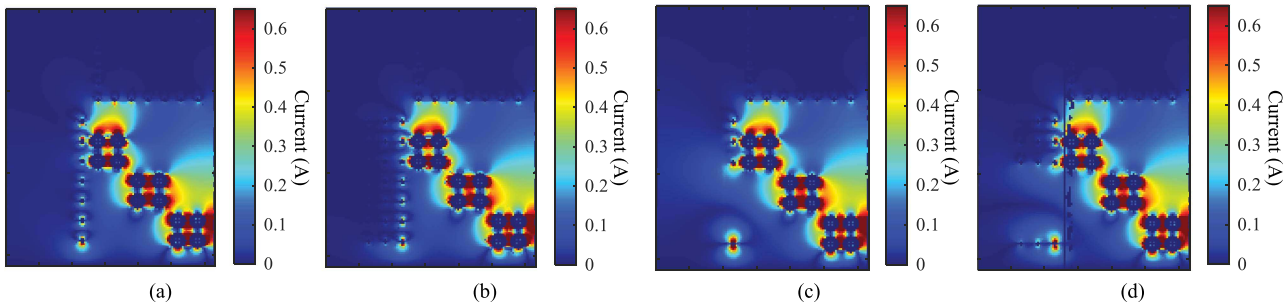

Fig. 24. Surface return current in the y-direction. (a) Single shielding via column. (b) Three shielding via columns. (c) Optimized number of vias with single column. (d) Optimized number of vias with three columns.

tangential current on the return plane to vertical current by absorbing leaked current from the antipad and rerouting it to other layers. This reduces noise coupling as the circular fields from the vertical current are not as strong as the tangential current. Second, the GND via serves as a path for conduction current to the return plane, allowing the rerouted leakage current to return through the GND via, which is positioned in close proximity to the VRM circuit. To track the conduction path of the return current, a simulation setup with the shielding GND via array is designed by applying an additional GND via array between the victim trace and VRM vias. The layer stackup is identical to the design proposed in Fig. 8. For the shielding vias, the gap between each via is 2 mm and the victim shielding, which surrounds the stripline, is applied. As discussed in the previous section, a patterned VRM via with a separated antipad is designed for the PCB. The victim stripline is placed 100 mils away from the noisy VRM antipad. The simulated current distribution on the return plane is shown in Fig. 22. For the field distribution simulation, 120 MHz of noise frequency which is regenerated in [16] is selected. Since some GND vias are placed close to the noisy antipads, the leaked current is rerouted to the other layers through the absorber GND vias. After absorption, the rerouted leaked current is returned through the emitter GND via as expected. Based on the simulation results, it is confirmed that the GND via greatly reduces the leaked current on the return plane compared with the PCB without shielding GND vias.

To quantify the shielding method, various designs for shielding vias are investigated, and a new figure of merit (FOM) is proposed. The designs for shielding vias are presented in Fig. 23, and the number of GND via arrays and nonrelevant vias are taken into consideration for quantification purposes. Shielding vias are applied in single-to-three columns, with a fixed distance between the stripline and VRM antipad. To optimize the number of vias, nonrelevant shielding vias are removed from the PCB. GND vias located on each edge of the column were found to mainly absorb and emit the conduction current, whereas those in the middle could be removed, leaving only absorber and emitter vias. The surface return current distribution, which depends on the design, is shown in Fig. 24. Additional shielding via columns are found to reduce the surface current around the victim trace by 20% by providing a further possibility to absorb the surface return current. However, the optimized shielding via arrays is unable to block the surface current, as the emitter vias could possibly emit the current into empty space.

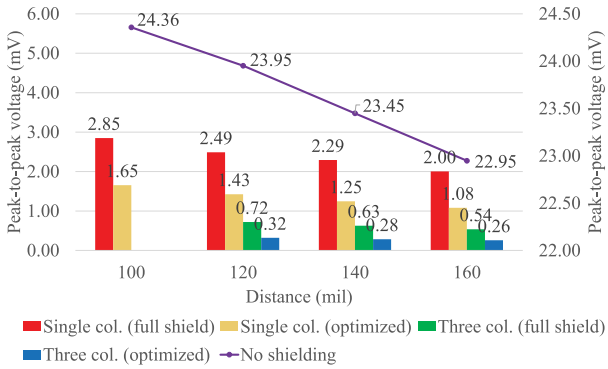

Fig. 25. Coupled voltage comparisons depending on the shielding methods.

To complete the investigation, a transient simulation using the setup shown in Fig. 4 is performed. The new S-parameters, which depend on the shielding via designs, are extracted and applied as a black box. The simulation results, shown in Fig. 25, demonstrate that most of the shielding methods reduce VRM noise coupling by at least 90% compared to designs without shielding. According to the transient analysis, it is always preferable to use as many shielding vias as possible. However, the large number of shielding vias required to achieve this goal can occupy a significant amount of space on the PCB's top and bottom layers, making the shielding methods less attractive. To evaluate the shielding structures proposed in this section, an FOM is proposed as follows:

$$\text{FOM} = \frac{V_{\text{reduced}}}{V_{\text{coupled}}} / (NS) \tag{5}$$

where V_{reduced}, V_{coupled}, N, and S are the reduced noise due to the shielding vias, coupled noise without shielding structure, number of shielding vias, and distance from the trace to the antipad of the VRM vias, respectively. The numerator and denominator of the proposed FOM represent the percentage of noise reduction and the area occupied by shielding vias, respectively. Therefore, the effectiveness of a shielding method is evaluated by its ability to provide higher noise reduction with a lower occupied area. The evaluation results for different shielding methods are presented in Fig. 26. Interestingly, the FOM of a single column with removed nonrelevant shielding vias is found to be higher than that of the fully shielded three columns of shielding vias, even though both methods achieve

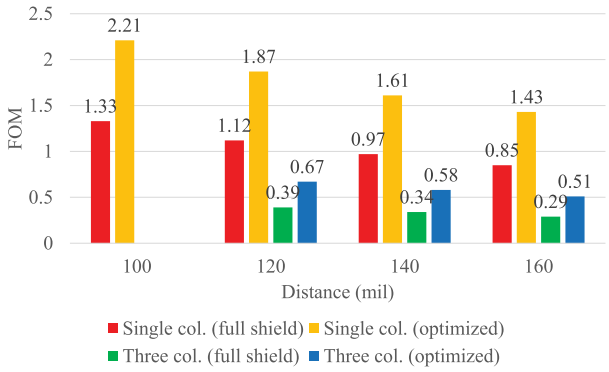

Fig. 26. Proposed FOM comparison.

around 90% reduction in noise. This is because the efficiency of shielding is evaluated based on the area occupied by the vias.

On the basis of the shielding methods investigation, it is confirmed that VRM noise coupling can be reduced with the sparsely placed GND shielding vias. Furthermore, the proposed FOM evaluates the shielding methods numerically with a given percentage of noise reduction and occupied PCB area.

VII. Conclusion

In this article, a comprehensive analysis of the VRM noise coupling to victim trace in highly integrated server platforms is presented. Design factors that have a significant impact on the VRM noise coupling are analyzed. Simulation results using the proposed design factors are compared, and the effectiveness of each design factor is validated through measurements using a simplified PCB. In addition, IR drop analysis using the resistance of the PCB and via is also carried out for the optimization of the via design. By calculating and comparing the resistance and ampacity of PCB and VRM group vias, the minimum required number of vias is calculated. From the calculated results, the optimal number and design of VRM vias that ensure minimum noise coupling are determined and validated using a numerical simulation. For the mitigation of existing VRM noise coupling, shielding through GND vias is analyzed. Based on the proposed analysis results, it is expected that optimal design can be achieved for a noisy VRM via against high-frequency noise coupling and dc IR drop in the early stage of the development cycle.

However, the proposed VRM via design factors must be carefully applied to the PDN design. In this work, the impact of decoupling capacitors to the time-domain peak-to-peak voltages is not simulated. Because the decoupling capacitors supply the charge when the sudden load current is required, the return current path discussed in this article could be changed. This changed return path can also have an impact on the IR drop. Furthermore, the selection of simulation frequencies and shielding GND vias must be carefully selected. The simulated frequency in this work is 120 MHz which the wavelength is electrically larger than the physical dimensions of the board. However, the higher noise frequencies may inject higher harmonics, leading to resonance. Therefore, the noise frequencies must be considered for the selection of the shielding structure, which can be future work.

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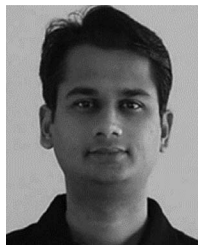

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