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Behavior Model of a Multiphase Voltage Regulator Module with Rapid Voltage Drop Protection

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***Abstract*— In this paper, a modeling method of voltage regulator module (VRM) with rapid voltage drop protection is introduced. The proposed VRM model captures a pulse-width modulation scheme developed to counteract substantial load currents with high di/dt, resulting in a large voltage drop across the power delivery network (PDN). The equations to describe the non-linear behavior associated with the multiphase VRM behavior are proposed and successfully validated for both light and heavy loads, the latter being particularly crucial to trigger the voltage drop protection measures.**

Keywords— voltage regulator module; rapid voltage drop protection; power distribution network; multiphase

I. INTRODUCTION

Accurate models of power distribution networks (PDNs) are fundamental to designing reliable and efficient systems and provide valuable insights for engineers to make informed decisions [1]. The PDN is comprised of several parts such as PCB, package, on-die, and voltage regulator module (VRM), and has been commonly modeled by using passive equivalent circuits. However, modern VRMs (usually multiphase) have adopted many non-linear features to improve power regulation, making it hard for passive-only equivalent circuits to represent the behavior. Thus, accurate non-linear models of multiphase VRMs are required for accurate end-to-end power integrity simulation.

Recent studies have employed SPICE-based circuits to replicate the VRM behavior. In [2, 3], modeling methods for single-phase VRMs are proposed, employing a simple combination of RL components for damping and active inductance in VRMs. Although these methods successfully capture the steady-state behavior of VRMs, passive components limit the representation of non-linear characteristics exhibited by actual VRMs.

Recently, there have been efforts to accurately represent the non-linear characteristics of VRMs using behavioral models. In [4, 5], methods for modeling non-linear single-phase VRMs have been proposed, with a focus on the adaptive voltage positioning (AVP) presented in [5], which has been validated through measurement. Despite these advancements, there remains an ongoing need for the development of complex multiphase VRM models to improve the end-to-end PDN transient simulations. To address this need, multiphase VRM modeling methods have been proposed [6-9]. The constant-on time (CoT) of modern VRMs is proposed in [7] using analytical equations. In [8], both discontinuous and continuous conduction modes (DCM and CCM) are proposed to simulate light and heavy loading conditions. Building upon [8], the phase activation control and pulse frequency and width modulation schemes (PFM and PWM) features are modeled in [9]. However, a crucial multiphase feature known as rapid voltage drop protection, widely adopted for quickly recovering the voltage in response to a high di/dt current load, has not been previously modeled.

In this paper, the rapid voltage drop protection feature of multiphase VRM is modeled and validated. To model the erratic behavior caused by high di/dt load currents, the phase activation that could be observed in practical VRMs is implemented. The proposed VRM model employs the analytic equations of a single voltage and multiple current loops to simulate general PWM-based multiphase VRM behavior. Utilizing a voltage sensing network with a predefined dv/dt threshold, the model determines the extended duty cycle on auxiliary phases when phase activation control is triggered. The proposed model is successfully benchmarked against measurements using an evaluation board (EVB).

II. MULTIPHASE VRM MODELING

For the completeness of the paper, the multiphase VRM modeling method is reiterated briefly. Fig. 1 shows the SPICE-based VRM model proposed in [9]. This model generates continuous-time operation, unlike other switching-based behavioral model. The time-averaged waveforms of VRM can be described as

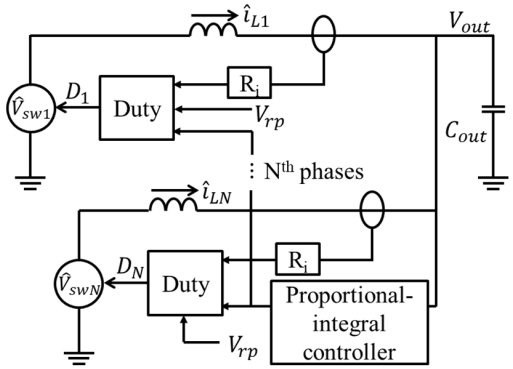


Fig. 1. Proposed continuous-time multiphase VRM model.

$$\hat{V}_{sw1} = D_1\left(V_{in} - r_{on,H}\hat{i}_{L1}\right) - (1 - D_1)r_{on,L}\hat{i}_{L1}. \quad (1)$$

$$\hat{V}_{swN} = (D_N(V_{in} - r_{on,H}\hat{\imath}_{LN}) - (1 - D_N)r_{on,L}\hat{\imath}_{LN})V_{APD} + V_{out}(1 - V_{APD}) \quad (2)$$

where V_{in}, $r_{on,L}$, $r_{on,H}$, and $\hat{\imath}_L$ are input voltage, on resistance of high and low side switches, and averaged inductor current. Then the pre-calculated duty cycles, denoted as D_1 and D_N, determine the averaged switching node voltages $\hat{V}_{sw1}$ and $\hat{V}_{swN}$. The turn-on signal of auxiliary phases, V_{APD}, is activated when the load current surpasses the threshold of phase adding current level. However, it is important to note that this model only provides the multiphase operation and requires the manipulated D_1 and D_N for enhanced accuracy in PDN simulation. The following section introduces a modeling method for the rapid voltage drop protection.

III. Rapid Voltage Drop Protection

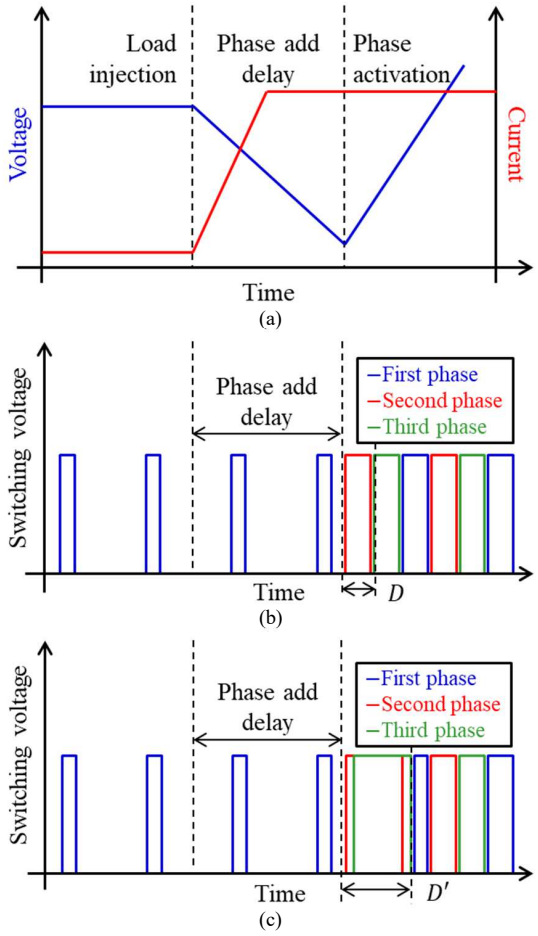


Fig. 2. Voltage and current of multiphase VRM and corresponding switching behavior. (a) Output voltage and load current. (b) Switching signals without rapid voltage drop protection. (c) Switching signals with rapid voltage drop protection.

In this section, the rapid voltage drop protection in 3-phase VRM is introduced. Fig. 2 shows the output voltage, load current, and corresponding switching operation of 3-phase VRM. The output voltage of VRM experiences a voltage drop when the load current is injected. Since the VRM cannot react to the sudden load injection immediately, the duty cycle of the switching signal is not extended. After phase add delay, the 2nd and 3rd phases are successively added to VRM without overlapped switching behavior as shown in Fig. 2(b). In this case, more recovery time is required to compensate for the voltage drop until it rises to the nominal level. To address this, the rapid voltage drop protection could be triggered in some VRMs. The switching operation with the rapid voltage drop protection are shown in Fig. 2(c). The same phase add delay is still required to activate the auxiliary phases. However, the auxiliary phases are simultaneously activated with the enlarged duty cycle *D'*. Compared with the duty cycle shown in Fig. 2(b), the enlarged duty cycle ensures fast voltage compensation against the large voltage drop.

A. Voltage Drop Detection

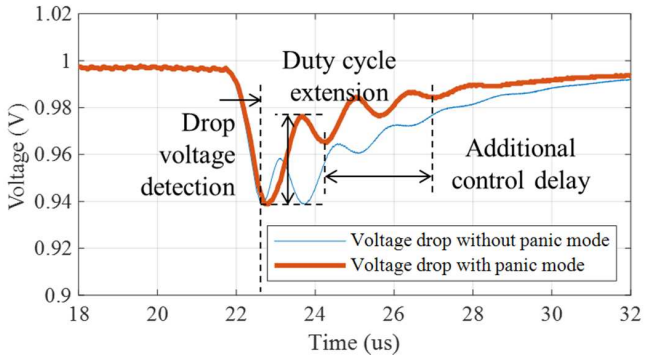


Fig. 3. VRM output voltages depending on rapid voltage drop protection.

The target voltage behavior with the rapid voltage drop protection is shown in Fig. 3. In this work, the EVB of multiphase VRM without load application is used. Instead, the embedded load current slammer is used to inject current. The EVB in this work is designed for power supply experiments. The generic modeling method in this paper is applicable to the various VRMs in the market with similar rapid voltage drop protection behavior. In this board, the rapid voltage drop protection is not always activated when the load current is injected. To trigger the rapid voltage drop protection, the real-time voltage drop must be detected. The threshold of rapid voltage drop protection is determined by a predefined voltage level of dv/dt. Because the initial voltage drop slope shown in Fig. 3 is determined by the capacitor, the threshold can be described as

$$dv = \frac{di}{C_{out}}dt \quad (3)$$

where *dv* and *di* are the change of voltage and current, *dt* is the given time window, and C_{out} is the output capacitance. The output capacitance can be usually found in the datasheet which is provided along with the EVB from the VRM manufacturers. The remaining variables are characterized by the measurement. In Fig. 3, the known load current is injected to observe the voltage behavior. With the known phase add delay after load injection [9], *dt* in (3) must be smaller than the phase add delay. After extraction of *dt*, *di* can be estimated from the known load current. For example, if the slew-rate of load current is 3A/µs, *di* would be 1.5 A when *dt* is defined as 0.5 µs.

After determining the threshold of rapid voltage drop protection, the manipulation of the duty cycle can be calculated by sensing the voltage drop. By applying the time delay of *dt* on the simulation model, *dv* in (3) can be calculated by subtracting V_{out} from V_{out_delay} as depicted in Fig. 4. When the subtracted voltage *dv* exceeds the threshold in (3), the duty cycle D_n of the voltage source in (2) has to be extended to quickly recover the voltage drop.

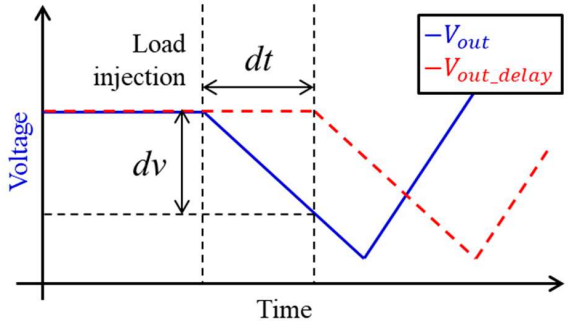


Fig. 4. Output voltages of VRM depending on the time delay *dt*.

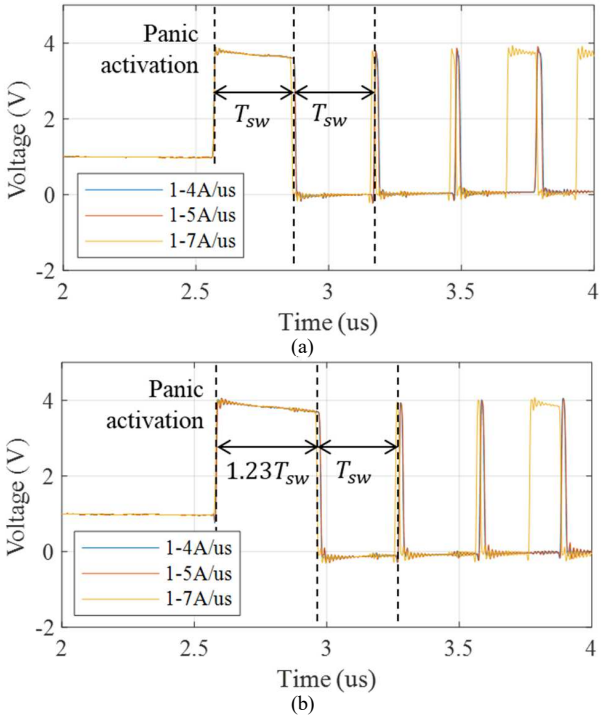


Fig. 5. Switching node voltages. (a) Second phase. (b) Third phase.

B. Duty Cycle Extension

To investigate the duty cycle extension of VRM, the switching voltage operations are measured and depicted in Fig. 5. For the various case studies, three different load current: 1-4A, 1-5A, and 1-7A/μs are applied. The nominal single switching time of VRM is 300 ns. Before the phase activation, the predefined output voltage of 1V is measured because the 2nd and 3rd phases are disconnected from MOSFET switches. After rapid voltage drop protection is activated, regardless of loading conditions, the increased duty cycles of 100% and 123% are measured for each 2nd and 3rd phase switching node. Thus, the duty cycle D_2 and D_3 for each 2nd and 3rd phases must be updated accordingly. The equations for updated 2nd and 3rd phases' duty cycles can be described below:

$$D_2 = \frac{1}{2} + \frac{V_{rp}}{T_{SW}\Delta SR_i} + \left(D_{\max\_2nd} - D_2\right)V_{APD} - \sqrt{\left(\frac{1}{2} + \frac{V_{rp}}{T_{SW}\Delta SR_i}\right)^2 - \frac{2}{T_{SW}\Delta S}\left(\frac{V_C}{R_i} - \hat{\imath}_{L2}\right)} \quad (4)$$

$$D_3 = \frac{1}{2} + \frac{V_{rp}}{T_{SW}\Delta SR_i} + \left(D_{\max\_3rd} - D_3\right)V_{APD} - \sqrt{\left(\frac{1}{2} + \frac{V_{rp}}{T_{SW}\Delta SR_i}\right)^2 - \frac{2}{T_{SW}\Delta S}\left(\frac{V_C}{R_i} - \hat{\imath}_{L3}\right)} \quad (5)$$

where $D_{\max\_2nd}$ and $D_{\max\_3rd}$ are the maximum duty cycles of 2nd and 3rd phases when rapid voltage drop protection is triggered. However, the continuous-time switching node voltages for the auxiliary phases in (2) can exceed input voltage V_{in} with enlarged duty cycles D_{max}. Thus, the switching node voltage must be limited by

$$V_{limit} = V_{in} - (r_{on,H} + r_L)\hat{\imath}_L. \quad (6)$$

In (6), r_L is DC resistance of external inductor. By applying a hard limit of input voltage, the accurate simulation of VRM with rapid voltage drop protection is achieved.

C. Additional Control Delay

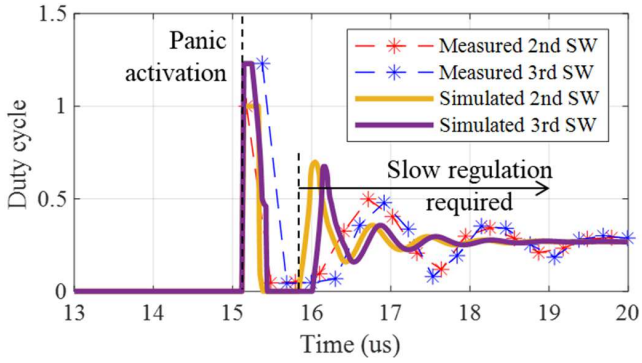


Fig. 6. Duty cycle comparison.

For the final step of rapid voltage drop protection modeling, the additional control delay shown in Fig. 3 is required. Before applying the control delay, the measured and simulated duty cycles are compared in Fig. 6. After rapid voltage drop protection is activated, both simulation and measurement show the extended duty cycles up to 100% and 123 % for each 2nd and 3rd phases. However, the simulations tend to be stabilized earlier than measurements. This is because, when the additional phases are activated, (4) and (5) are continuously updated in the VRM model proposed in [9], while the switching VRM keeps the duty of the PWM signal during the single switching cycle. Thus, the additional control delay is required only when rapid voltage drop protection is triggered. In this work, additional 200 and 400 ns for each 2nd and 3rd phases are applied.

IV. Measurement-based Validation

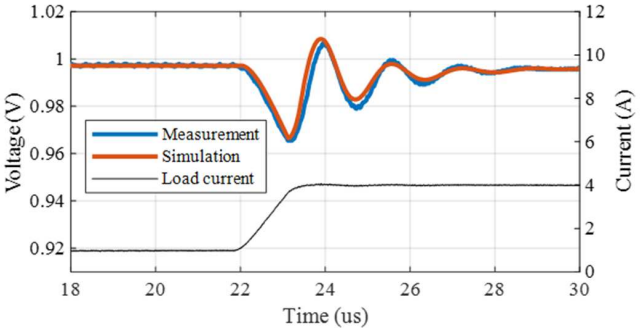
For the validation of rapid voltage drop protection, the output voltage behavior depending on the load current is measured and compared with the simulation. The required and new design parameters are introduced in [7, 9, 10] and for rapid voltage drop protection are summarized in Tables I and II. In the EVB, the embedded load slammer is used to test the high current loads seen as application processors. It is controlled by the external signal generator and the voltage-to-current conversion ratio is 1A/10mV which can be monitored through the current sense output. In this measurement, to trigger the rapid voltage drop protection and validate the VRM model, the various step load current is applied, and corresponding voltage and current waveforms are measured and compared to the simulation. In the simulation, an ideal current source is applied to the output of VRM.

TABLE I.
Design Parameters of Multiphase VRM Model

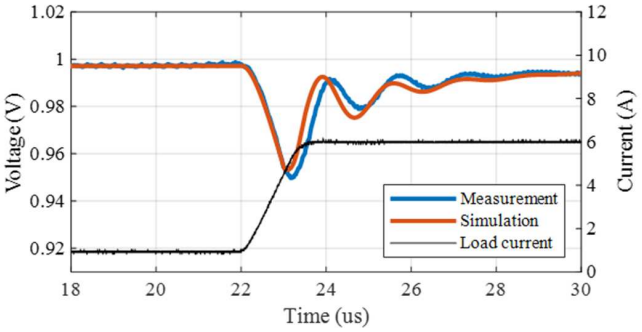
Type	Parameters	Description
Known parameters	L	External inductor
	C_{out}	Output capacitor
	$r_{on,H}, r_{on,L}$	Turn-on resistance
	r_L	DC resistance of inductor
	V_{ref}	Reference voltage
	V_{in}	Input voltage
	T_{sw}	Switching cycle
	T_{add}	Phase add delay
	T_{drop}	Phase drop delay
	I_{add}	Phase add threshold
	I_{drop}	Phase drop threshold
Extracted and tuned parameters	R_i	Current sensing gain
	V_{rp}	Ramp voltage
	$K_{P.S}, K_{I.S}, K_{DC.S}$	Single-phase voltage controller
	$K_{P.M}, K_{I.M}, K_{DC.M}$	Multiphase voltage controller

TABLE II.
Additional Design Parameters for Rapid Voltage Drop Protection

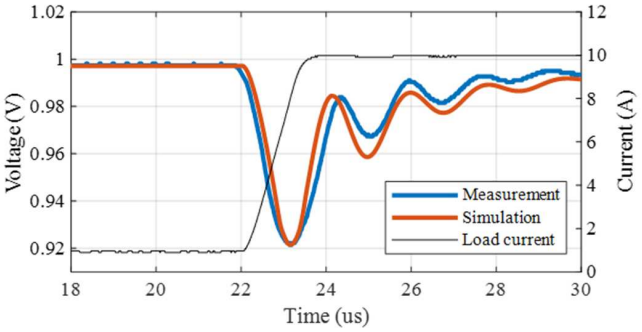
Type	Parameters	Description
Known parameters	$D_{\max\_2nd}$	Maximum duty cycle of 2nd phase
	$D_{\max\_3rd}$	Maximum duty cycle of 3rd phase
	T_{add_2nd}	Additional control delay of 2nd phase
	T_{add_3rd}	Additional control delay of 3rd phase



(a)



(b)



(c)

Fig. 7. Validation of proposed multiphase VRM with rapid voltage drop protection with various load of: (a) 1-4A/µs. (b) 1-6A/µs. (c) 1-10A/µs.

The comparisons between measurements and simulations is shown in Fig. 7. From the measurement, the VRM shows a large voltage drop when the load current is injected, and an irregular high voltage peak follows. This is caused by the extended duty cycle to compensate for the rapid voltage drop due to the high di/dt of load current. Thus, the overreacting supply current leads the VRM output voltage to irregular high voltage peaks. However, it can be found that the high voltage peak after rapid voltage drop protection tends to be decreased when the amount of step load increases. When the rapid voltage drop protection is triggered, the duty cycle is always fixed to 100% and 123%, resulting in the same supply current from VRM. Thus, the voltage peak becomes lower when the step load goes higher. In this validation, the target voltage behavior is maximum voltage drop and peak before and after rapid voltage drop protections. The largest error in the voltage drop is 5.5 mV when 1-8A/µs is

applied to the simulation. Overall, the proposed simulation model shows a good correlation with measurements.

V. Conclusion

This paper introduces the modeling method of a multiphase VRM with rapid voltage drop protection for accurate end-to-end PDN simulations. The SPICE-based VRM model employs equation-based voltage control sources to emulate the rapid voltage drop protection. The correlation between measurement and simulation results validates the effectiveness of the VRM model under various loading conditions. On the basis of this result, the proposed modeling method is expected to provide an accurate end-to-end transient simulation in PDN design.

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