2024 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI) | 979-8-3503-6039-4/24/$31.00 ©2024 IEEE | DOI: 10.1109/EMCSIPI49824.2024.10705593

Vertical Interconnect Technology in Silicon, Package, and Printed Circuit Board (PCB) with Coaxial Structure

Junyong Park
Electrical and Computer Engineering
Missouri University of Science and Technology
Rolla, MO, USA
junyongpark@mst.edu

Chaofeng Li
Electrical and Computer Engineering
Missouri University of Science and Technology
Rolla, MO, USA
clf83@mst.edu

Eddie Mok
Wus Printed Circuit (Kunshan) Co., Ltd
Kunshan, China
eddie_mok@wustec.com

Joe Dickson
Wus Printed Circuit (Kunshan) Co., Ltd
Kunshan, China
1144@joedwuspcbintl.com

Joan Tourné
NextGin Technology
Netherlands
j.tourne@nextgin-tech.com

Donghyun (Bill) Kim
Electrical and Computer Engineering
Missouri University of Science and Technology
Rolla, MO, USA
dkim@mst.edu

***Abstract*—This paper introduces vertical interconnect technology in silicon, package, and printed circuit board (PCB) levels with a coaxial structure, respectively. The coaxial structure has been known to be advantageous in terms of signal integrity (SI) compared to the non-coaxial structure. The coaxial structure is easy to control the characteristic impedance Z_0 and robust to crosstalk. The silicon-level interconnect includes the wire bonding (WB) and through-silicon via (TSV) technology, the package-level interconnect includes an elastomer package test socket. The PCB-level interconnect includes the vias, and vertical conductive structure (VeCS). For each level, the non-coaxial and coaxial interconnects are compared with the measurement results in the frequency domain. In conclusion, this paper successfully shows the improvement of the coaxial structure at silicon, package, and PCB levels.**

Keywords—3D integrated circuit, coaxial structure, package, PCB, signal integrity, TSV, vertical interconnect.

I. Introduction

A three-dimensional (3D) vertical structure has advantages compared to a two-dimensional (2D) planar structure in terms of signal integrity (SI) [1]. Manhattan distance is the distance between two routing points. The Manhattan distance can be substantially decreased when the 3D structure is applied [2, 3]. The Manhattan distance can be regarded as the amount of parasitic resistance and inductance between two routing points [4]. The decreased resistance mitigates an RC delay which attenuates and widens a signal over a high-speed channel [5]. Also, the decreased inductance mitigates crosstalk. The crosstalk is caused by the capacitive and magnetic coupling [6]. Therefore, the 3D structure is desirable in terms of SI.

As the data rate increases, SI issues like the above have been addressed [7]. The SI issues are different depending on the levels: silicon, package, and PCB as shown in Fig. 1. Because they have different fabrication processes, they have totally different structures and parasitic values. However, all levels have to be considered to achieve the signal integrity. For this, the SI analysis has been introduced for the silicon level [8]–[10], and the PCB level [11]. Vertical interconnections include a through-silicon via (TSV), elastomer package socket, and printed circuit board (PDB) via depending on levels. The interconnections always have references, which determines a characteristic impedance Z_0. The Z_0 is the ratio between electric (E) and magnetic (H) -fields at the cross-section of a transmission line, thus, it is determined by a signal and a reference [12]. The coaxial structure has the signal and reference placed on the same axis, thus it has the well-confined E- and H-fields. A coplanar waveguide as an example of a non-coaxial structure has a concentrated E-field distribution between the signal and reference, which leads to being sensitive to the characteristic impedance depending on the change in the dimensions. The above characteristic of the coaxial structure makes the impedance control easy. The signal is shielded by the

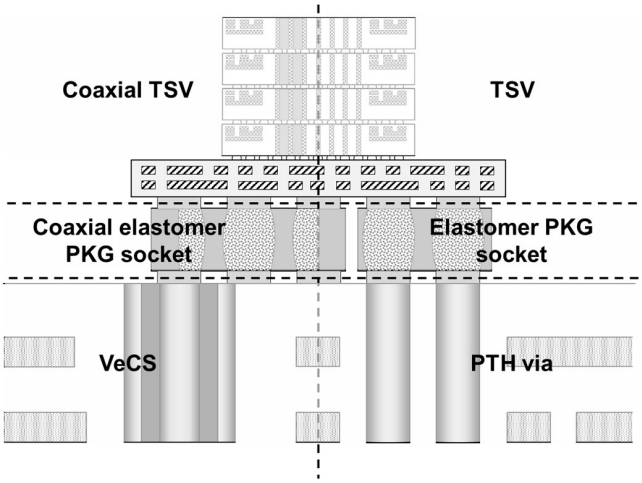


Fig. 1. Vertical interconnects depending on silicon, package, and PCB.

Authorized licensed use limited to: Missouri University of Science and Technology. Downloaded on January 16,2025 at 18:36:03 UTC from IEEE Xplore. Restrictions apply.

reference, which leads to being robust to crosstalk noise. Also, the impedance discontinuity is avoidable in the coaxial configuration. Because the signal is surrounded by the ground, the return path only exists in the ground shield. Thus, the microwave system uses the coaxial configuration such as SubMiniature version A (SMA).

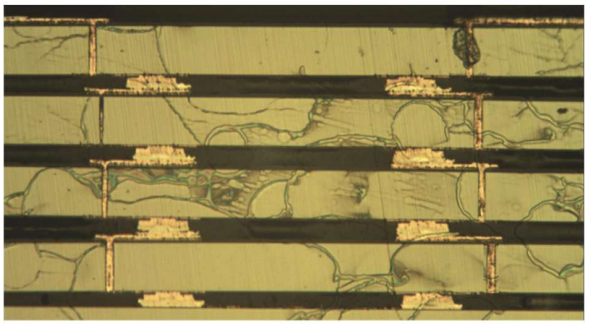
This paper introduces the vertical interconnects at silicon, package, and PCB levels. Also, this paper introduces how a coaxial configuration is applied at each level. This paper is organized as follows. The vertical interconnects at the silicon, package, and PCB levels are introduced, respectively. Each section compares the non-coaxial and coaxial interconnects in terms of SI.

II. Vertical Interconnects at Silicon Level

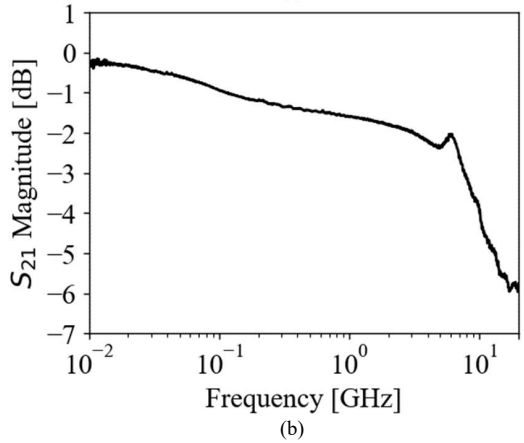
Silicon-level vertical interconnects include the TSV and the wire bonding (WB) technologies to interconnect between silicon dies.

A. Through-Silion Via (TSV)

The TSV technology achieves a shorter physical distance and a lower parasitic inductance compared to the WB technology [13] for stacked multi-silicon dies such as a high-bandwidth memory (HBM). The WB technology provides a vertical interconnection, however, a gold wire introduces a substantial amount of parasitic inductance. The WB technology cannot also provide a direct connection because the silicon dies are flipped and interconnected by the WB technology. The property of the TSV is advantageous in terms of SI. The TSV technology drills a silicon die and filled by the copper to interconnect the silicon dies, as shown in Fig. 2 (a).



(a)



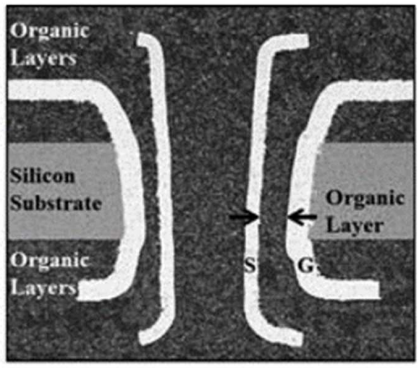
(b)

Fig. 2. (a) Cross-section of the fabricated TSVs (Fig. 4 in [14]). The silicon is drilled and filled by copper. (b) The measured insertion loss of the fabricated TSV chain (Fig. 5 in [14]).

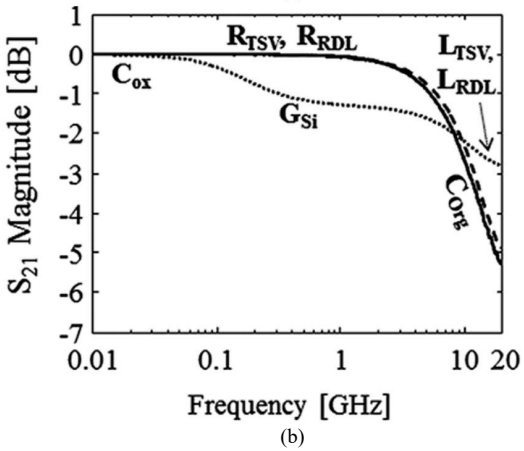
Fig. 2 (b) shows the measured insertion loss of the fabricated TSVs. The test vehicle included 8 stacked TSVs and redistribution layers (RDLs) [14]. The insertion loss was measured up to 20 GHz in the frequency domain. The test vehicle had a gradual insertion loss in MHz range and a steep insertion loss in GHz range. When the signal propagates along with the TSV, the reference is typically the closest conductive thing nearby. The above introduces the coaxial structure of the TSV to mitigate the impedance mismatches in the high-speed channel including the TSV.

B. Coaxial TSV

The TSV can be fabricated with a coaxial configuration. As shown in Fig. 3 (a), additional copper is fabricated around the TSV [15]. The fabricated coaxial TSV consists of a center conductor and a shield. The thin-film and organic lamination technique was used to fabricate the low-cost coaxial TSV. The fabrication includes laser drilling and copper metallization. The shield makes impedance control easier than the non-coaxial TSV. Also, the reference shield in the coaxial TSV mitigates the near- and far-end crosstalk. In conclusion, the TSV even improves the SI at the silicon level compared to the WB technology, the coaxial TSV improves further the SI.



(a)



(b)

Fig. 3. (a) A scanning electrode microscope (SEM) image of the cross-section for the coaxial through-silicon via (TSV) (Fig. 1. (b) in [15]). (b) Measured insertion loss (black solid line) of the fabricated coaxial TSV. (Fig. 4 in [15]).

Identify applicable funding agency here. If none, delete this text box.

Authorized licensed use limited to: Missouri University of Science and Technology. Downloaded on January 16,2025 at 18:36:03 UTC from IEEE Xplore. Restrictions apply.

Fig. 3 (b) (Fig. 4 in [15]) shows the measured insertion loss of the fabricated coaxial TSVs. The test vehicle included 4 coaxial TSVs and RDLs. The insertion loss of the test vehicle was measured up to 20 GHz. Unlike the measurement result of the non-coaxial TSV, the resonances were not identified up to 20 GHz. As discussed earlier, the impedance mismatch was suppressed by introducing the coaxial structure. That is, the coaxial structure is advantageous in terms of the SI. Also, the crosstalk performance can be improved by the shield conductor in the coaxial TSV. However, the coaxial structure may increase the fabrication cost due to additional processes.

III. Vertical Interconnect at Package Level

Package test sockets are required to provide a temporary connection for SI. A temporary connection is achieved by compression with a force. Thus, test sockets with a compressible interconnect are introduced in this section.

A. Elastomer package test socket

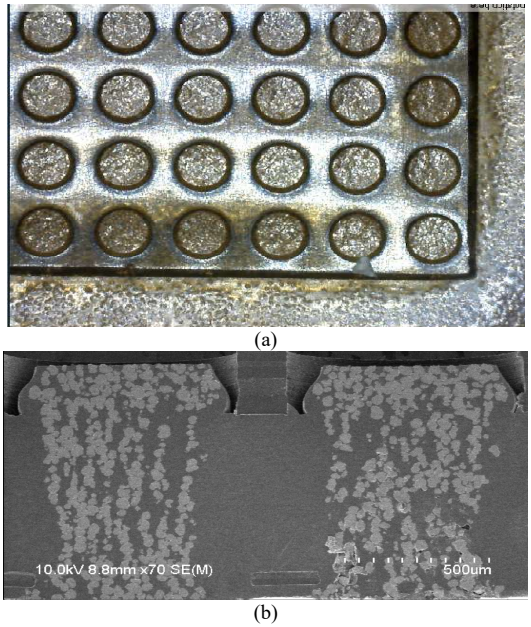
A pogo pin is conductive when being compressed, because it includes a metal spring [16]. However, the metal spring introduces a substantial parasitic inductance due to its structure. Hence, the pogo pin is limited to use for high-frequency package tests. An elastomer package socket is also conductive when a vertical force is applied. As shown in Fig. 4 (a), the elastomer socket includes conductive powders in an elastomer material [17]. The powders are contacted with one another when the elastomer material is compressed [18]. In terms of the temporary connection, the pogo pin and elastomer socket are the same. However, the absence of the metal spring improves the elastomer socket in terms of the electrical performance in the high-frequency range.

B. Coaxial elastomer package test socket

The coaxial approach was also applied to the pogo pin [19]. The coaxial pogo pin improved the crosstalk performance, however the principal limitation which is the significant amount of parasitic inductance was still inevitable. The elastomer socket without the metal spring is also fabricable in the coaxial structure. The coaxial elastomer socket was fabricated by injecting conductive powders in a coaxial direction inside the elastomer material [20]. The conductive powders are then placed in the coaxial form after the fabrication process. The inner set of the powders is for signal and the outer set of the powders is for reference as shown in Fig. 5. Both of the non-coaxial and coaxial elastomer sockets have the same pitch of 1.0 mm.

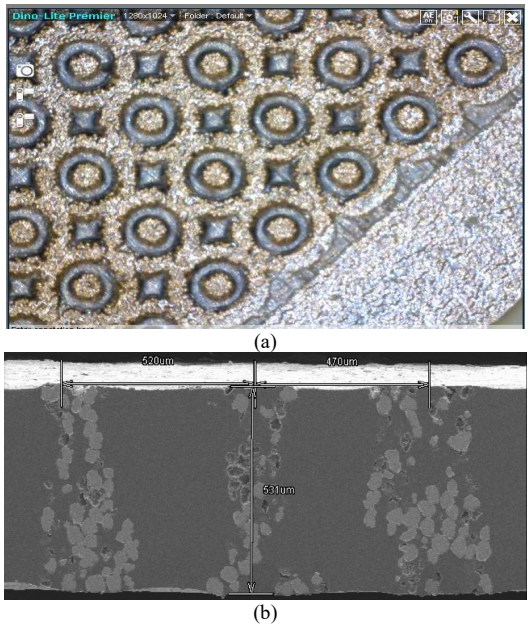
Fig. 6 compares the measured insertion loss and the far-end crosstalk (FEXT) in the frequency domain. According to the comparison, the advantage of the coaxial structure is clearly shown again as discussed in this paper. The non-coaxial socket had a resonance near 20 GHz, while the coaxial socket did not. The non-coaxial socket has a reference column next to the signal column, which causes the E-field to be distributed in between. While, the coaxial socket has a larger reference column to surround the signal column. The E-field is equally distributed along with the circumference of the signal column. The difference in the field distribution makes the different resonance frequencies.

Another advantage of the coaxial structure was identified in the measured crosstalk: 20 dB/dec [21]. The slope difference in the crosstalk resulted from an asymmetry in the signaling [22]. The non-coaxial structure only supports the ground-signal (GS) signaling, hence, asymmetry is inevitable. However, the coaxial structure supports the ground-signal-ground (GSG) signaling which is desirable in terms of the asymmetry. Therefore, another advantage of the coaxial structure is identified in the crosstalk measurement herein. The cost for the coaxial case is nearly the same as that of the non-coaxial case. Because they have the same amount of conductive powders. They only have different configurations of the applied E-field to align the conductive powders in an elastoemer material.



(a) (b)

Fig. 4. (a) Top view image and (b) cross-sectional SEM image of the non-coaxial elastomer socket.



(a) (b)

Fig. 5. (a) Top view image and (b) cross-sectional SEM image of the coaxial elastomer socket.

Authorized licensed use limited to: Missouri University of Science and Technology. Downloaded on January 16,2025 at 18:36:03 UTC from IEEE Xplore. Restrictions apply.

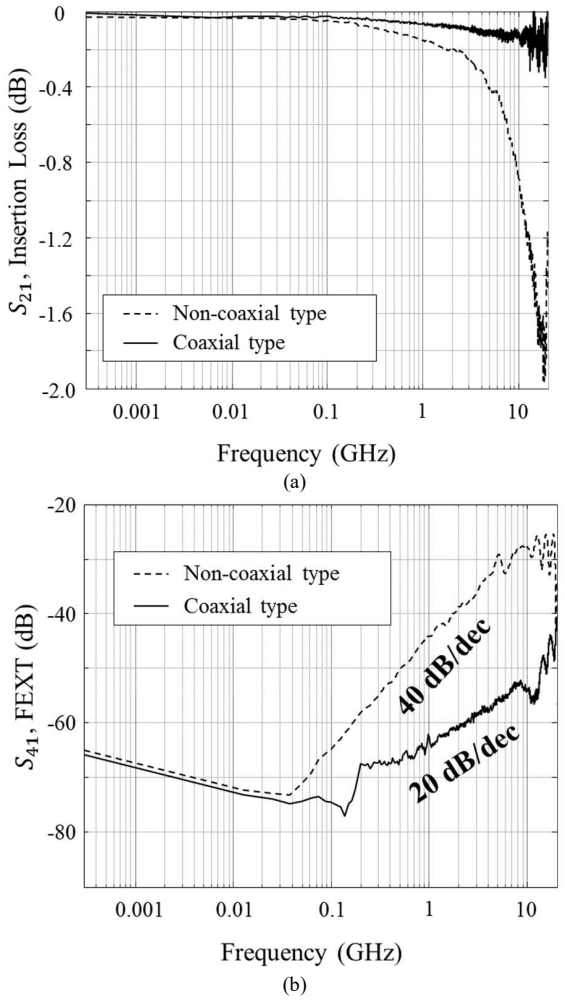


Fig. 6. Measured insertion losses and FEXT of non-coaxial and coaxial elastomer sockets.

IV. Vertical Interconnect at PCB Level

The PCB provides interconnections between the packages and discrete components such as capacitors, switches, connectors, filters, and resistors [23]–[24]. The PCB is required to be designed as small as possible due to the form factor of a system. To satisfy the above, the PCB had to be designed and fabricated with a multi-layer structure, which leads to vertical interconnects in the PCB.

A. Plated Through Hole (PTH) Via

The vertical interconnections in the multi-layer PCB include blind, stacked, staggered, buried, and PTH vias depending on which layers are connected [25]. As can be seen from Fig. 7, the PTH via provides a connection from the top to bottom layers [26]. Thus, the PTH via is the longest type among the fabricable vias in the PCB technology. In the SI, the longest channel typically implies the worst channel. Because the corresponding insertion loss and FEXT are usually proportional to the length [27]–[28]. Furthermore, the non-coaxial structure may have resonance depending on the channel. Therefore, the multi-layer PCB generally has limited electrical performances due to the PTH vias. For this reason, most signal integrity analyses on the

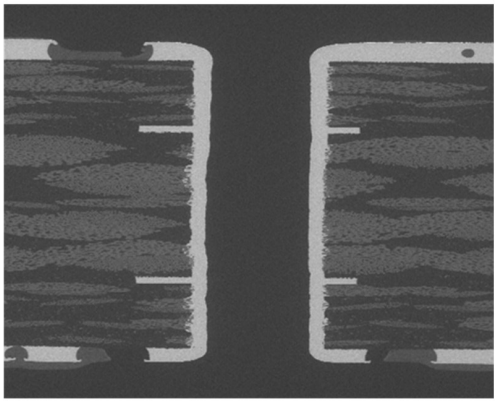


Fig. 7. The PTH via provides a connection between the top and bottom layers [26].

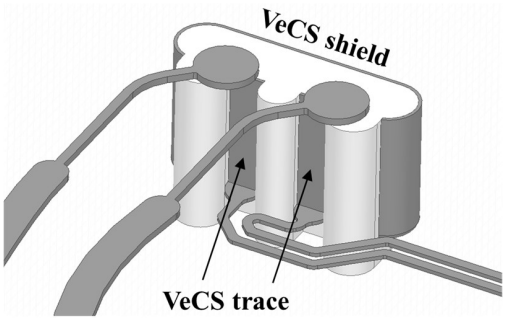
via have focused on a modeling-based approach [29–31]. The PCB via also has multiple reflections due to impedance mismatches [32].

B. Vertical Conductive Struture (VeCS)

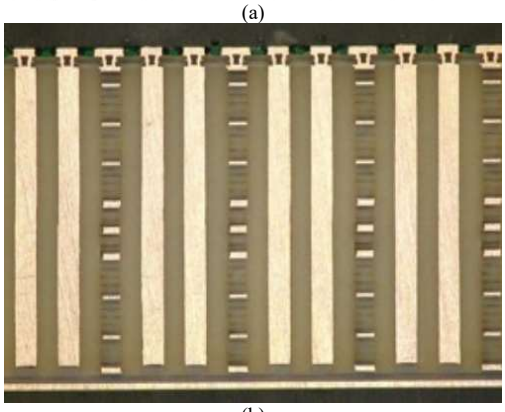
The VeCS was introduced to improve the electrical performances of the multi-layer PCB [33]–[35]. The VeCS consists of a VeCS trace and metal jacket to shield the VeCS trace as can be seen from Fig. 8. (a). The VeCS is a semi-coaxial structure, because most of the electric (E)- and magnetic (H)-fields are distributed between the VeCS trace and metal jacket. Thus, the VeCS also has the advantage of the coaxial structure. When the signal propagates over the VeCS trace (Fig. 8 (b)), the return current for the signal is induced over the metal shield (Fig. 8 (c)). That is, the characteristic impedance is constant during the signal propagation on the VeCS. In contrast, the PTH via has no vertical reference such as the metal jacket in the VeCS. Thus, the PTH via typically has a substantial amount of signal reflection during the signal propagation. This signal reflection may cause resonances on the insertion loss.

Fig. 9 shows the simulated time-domain reflectometer (TDR) in the time domain, and the measured insertion loss up to 70 GHz in the frequency domain. The simulated models include only either the PTH via or the VeCS, and the HFSS from ANSYS was used. The TDR shows how much the voltage is reflected along with the signal propagation, which can be used to show how much the characteristic impedance varies. The simulated TDR shows that the VeCS has less amount of signal reflection along with the signal propagation. The measured test vehicles included the fabricable ranges for the PTH vias and the VeCS with the same pitch. Thus, each set shows the practical insertion losses for the PTH vias and the VeCS, respectively. According to the measurement result, while some PTH vias had resonances around 35 GHz, the VeCS did not. The undesired resonances are resulted from the poor return path [36]. Because the PTH vias have the reference changes along with the signal propagation. Also, the slope of the measured insertion loss is less steep in the case of the VeCS. Therefore, the VeCS improved the electrical performances with the semi-coaxial structure. The VeCS shows better electrical performances, however the cost for the VeCS is comparable to that of the PTH via.

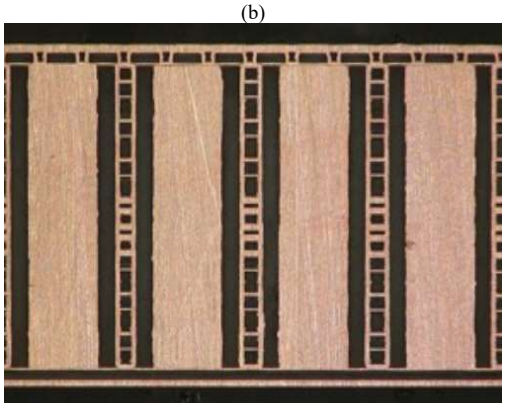
Authorized licensed use limited to: Missouri University of Science and Technology. Downloaded on January 16,2025 at 18:36:03 UTC from IEEE Xplore. Restrictions apply.



(a)



(b)

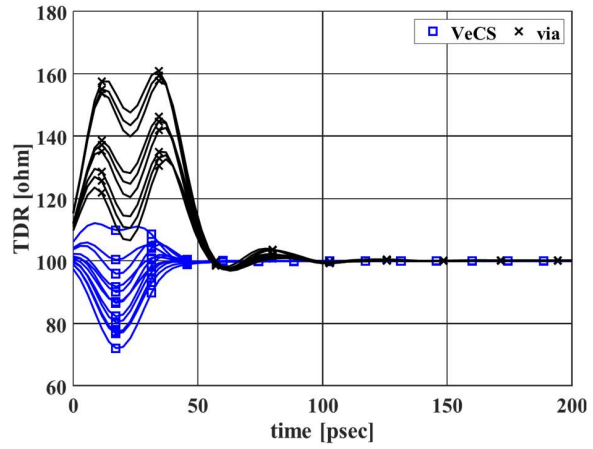


(c)

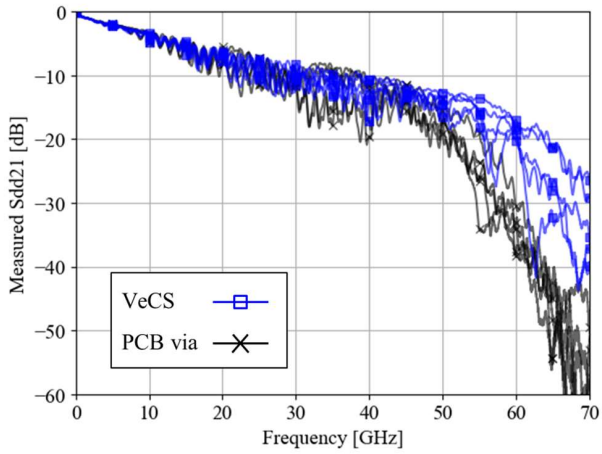
Fig. 8. (a) The VeCS consists of the VeCS trace and metal jacket. The VeCS also provides a connection from the top to the bottom layers with (b) the VeCS trace and (c) metal shield.

V. Conclusion

This paper introduces the vertical technology with the coaxial structure in silicon, package, and PCB levels, respectively. The coaxial structure has advantages in the SI due to its geometrical characteristics. The charge distribution is determined by the signal and reference, thus, the coaxial structure has equally distributed charges over a circumference. While, the non-coaxial structure has a biased charge distribution depending on the reference. The vertical interconnect in the laminated multi-layer may be sensitive to signal reflection by the mismatched characteristic impedance. The laminated structure may have different characteristic impedance, the non-coaxial structure may be sensitive correspondingly. Also, the crosstalk noise is suppressed by a surrounding reference in the coaxial structure. The measurement and simulation results herein successfully show the above advantages of the coaxial



(a)



(b)

Fig. 9. (a) The simulated TDR results and (b) measured differential insertion loss for the VeCS (blue solid lines) and the PTH vias (black solid lines).

structure for the TSV, the elastomer package socket, and the PCB via.

Acknowledgment

This article is based upon work supported partially by the National Science Foundation under Grant No. IIP-1916535 and equipment loaned by Rohde & Schwarz.

References

[1] W. R. Davis et al., "Demystifying 3D ICs: the pros and cons of going vertical," in IEEE Design & Test of Computers, vol. 22, no. 6, pp. 498-510, Nov.-Dec. 2005, doi: 10.1109/MDT.2005.136.

[2] S. William, "Semiconductive wafer and method of making the same," U.S. Patent US3044909A, Jul. 17, 1962.

[3] J. U. Knickerbocker et al., "Three-dimensional silicon integration," in IBM Journal of Research and Development, vol. 52, no. 6, pp. 553-569, Nov. 2008, doi: 10.1147/JRD.2008.5388564.

[4] C. A. Balanis, Advanced Engineering Electromagnetics. Hoboken, NJ: John Wiley & Sons, 2012.

[5] M. N. O. Sadiku and L. C. Agba, "A simple introduction to the transmission-line modeling," in IEEE Transactions on Circuits and Systems, vol. 37, no. 8, pp. 991-999, Aug. 1990, doi: 10.1109/31.56072.

[6] N. Kim, D. Wu, J. Carrel, J. -H. Kim and P. Wu, "Channel design methodology for 28Gb/s SerDes FPGA applications with stacked silicon interconnect technology," 2012 IEEE 62nd Electronic Components and

Authorized licensed use limited to: Missouri University of Science and Technology. Downloaded on January 16,2025 at 18:36:03 UTC from IEEE Xplore. Restrictions apply.

Technology Conference, San Diego, CA, USA, 2012, pp. 1786-1793, doi: 10.1109/ECTC.2012.6249080.

[7] L. Green, "Understanding the importance of signal integrity," in IEEE Circuits and Devices Magazine, vol. 15, no. 6, pp. 7-10, Nov. 1999, doi: 10.1109/101.808850.

[8] P. Nordholz, D. Treytnar, J. Otterstedt, H. Grabinski, D. Niggemeyer and T. W. Williams, "Signal integrity problems in deep submicron arising from interconnects between cores," Proceedings. 16th IEEE VLSI Test Symposium (Cat. No.98TB100231), Monterey, CA, USA, 1998, pp. 28-33, doi: 10.1109/VTEST.1998.670845.

[9] D. Sylvester, Chenming Hu, O. S. Nakagawa and Soo-Young Oh, "Interconnect scaling: signal integrity and performance in future high-speed CMOS designs," 1998 Symposium on VLSI Technology Digest of Technical Papers (Cat. No.98CH36216), Honolulu, HI, USA, 1998, pp. 42-43, doi: 10.1109/VLSIT.1998.689191.

[10] J. Fan, X. Ye, J. Kim, B. Archambeault and A. Orlandi, "Signal Integrity Design for High-Speed Digital Circuits: Progress and Directions," in IEEE Transactions on Electromagnetic Compatibility, vol. 52, no. 2, pp. 392-400, May 2010, doi: 10.1109/TEMC.2010.2045381.

[11] T. -L. Wu, F. Buesink and F. Canavero, "Overview of Signal Integrity and EMC Design Technologies on PCB: Fundamentals and Latest Progress," in IEEE Transactions on Electromagnetic Compatibility, vol. 55, no. 4, pp. 624-638, Aug. 2013, doi: 10.1109/TEMC.2013.2257796.

[12] D. Pozar, *Microwave Engineering*. John Wiley & Sons, 2021.

[13] M. Motoyoshi, "Through-Silicon Via (TSV)," in Proceedings of the IEEE, vol. 97, no. 1, pp. 43-48, Jan. 2009, doi: 10.1109/JPROC.2008.2007462.

[14] J. Park et al., "A Novel Eye-Diagram Estimation Method for Pulse Amplitude Modulation With N-Level (PAM-N) on Stacked Through-Silicon Vias," in IEEE Transactions on Electromagnetic Compatibility, vol. 61, no. 4, pp. 1198-1206, Aug. 2019, doi: 10.1109/TEMC.2018.2843813.

[15] D. H. Jung et al., "30 Gbps High-Speed Characterization and Channel Performance of Coaxial Through Silicon Via," in IEEE Microwave and Wireless Components Letters, vol. 24, no. 11, pp. 814-816, Nov. 2014, doi: 10.1109/LMWC.2014.2348502.

[16] H. Barnes, J. Moreira, H. Ossoinig, M. Wollitzer, T. Schmid and Ming Tsai, "Development of a pogo pin assembly and via design for multi-gigabit interfaces on automated test equipment," 2006 Asia-Pacific Microwave Conference, Yokohama, Japan, 2006, pp. 381-384, doi: 10.1109/APMC.2006.4429444.

[17] H. Kim et al., "High-Frequency Modeling and Signal Integrity Analysis of a Silicone Rubber Socket for High-Performance Package," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 7, no. 8, pp. 1356-1368, Aug. 2017, doi: 10.1109/TCPMT.2017.2712362.

[18] J. Park et al., "Analysis of external force dependent lumped RLGC model of high-bandwidth and high-density silicone rubber socket," 2015 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), Seoul, Korea (South), 2015, pp. 54-57, doi: 10.1109/EDAPS.2015.7383666.

[19] R. -B. Sun, C. -Y. Wen and R. -B. Wu, "A New Isolation Structure of Pogo Pins for Crosstalk Reduction in a Test Socket," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 1, no. 4, pp. 586-594, April 2011, doi: 10.1109/TCPMT.2010.2102491.

[20] J. Park et al., "High-Frequency Electrical Characterization of a New Coaxial Silicone Rubber Socket for High-Bandwidth and High-Density Package Test," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 8, no. 12, pp. 2152-2162, Dec. 2018, doi: 10.1109/TCPMT.2018.2828223.

[21] J. Park et al., "Electrical Performance Comparison between Coaxial and Non-coaxial Silicone Rubber Socket," 2019 Joint International Symposium on Electromagnetic Compatibility, Sapporo and Asia-Pacific International Symposium on Electromagnetic Compatibility (EMC Sapporo/APEMC), Sapporo, Japan, 2019, pp. 293-296, doi: 10.23919/EMCTokyo.2019.8893841.

[22] R. Brind., "Understanding the dual-slope effect in corsstalk (EL-FEXT)" [Online] Available: https://www.joepeesoft.com/Public/DSL_Corner/Docs/Presentations/PUB_2016_06_29_UFBB_Seminar_RobBrink.pdf

[23] "What is a printed circuit board? make circuits by connecting components," Altium, https://resources.altium.com/p/what-is-a-pcb (accessed Jan. 14, 2024).

[24] F. Gisin and Z. Pantic-Tanner, "Design advances in PCB/backplane interconnects for the propagation of high speed Gb/s digital signals," 6th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Service, 2003. TELSIKS 2003., Nis, Yugoslavia, 2003, pp. 184-191 vol.1, doi: 10.1109/TELSKS.2003.1246211.

[25] G. Shemesh, "PCB vias: An in-depth guide," An In-Depth Guide to PCB Vias and PCB Design, https://www.epiccolo.com/articles/pcb-vias-guide (accessed August 10, 2023).

[26] Riemer, E. (2017, August 27). *Plated thru hole*. SEM Lab Inc. https://www.semlab.com/example26/

[27] Y. Liu et al., "Far-End Crosstalk Modeling and Prediction for Stripline With Inhomogeneous Dielectric Layers (IDLs)," in IEEE Transactions on Signal and Power Integrity, vol. 1, pp. 93-103, 2022, doi: 10.1109/TSIPI.2022.3203031.

[28] Y. Liu et al., "An Empirical Modeling of Far-End Crosstalk and Insertion Loss in Microstrip Lines," in IEEE Transactions on Signal and Power Integrity, vol. 1, pp. 130-139, 2022, doi: 10.1109/TSIPI.2022.3214172.

[29] C. Li et al., "High-Speed Differential Via Optimization using a High-Accuracy and High-Bandwidth Via Model," 2023 IEEE Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMC+SIPI), Grand Rapids, MI, USA, 2023, pp. 280-285, doi: 10.1109/EMCSIPI50001.2023.10241408.

[30] C. Li et al., "Mode-decomposition-based Equivalent Via (MEV) Model and MEV Model Application Range Analysis," 2023 Joint Asia-Pacific International Symposium on Electromagnetic Compatibility and International Conference on ElectroMagnetic Interference & Compatibility (APEMC/INCEMIC), Bengaluru, India, 2023, pp. 1-4, doi: 10.1109/APEMC57782.2023.10217672.

[31] C. Li, K. Cai, M. Ouyang, Q. Gao, B. Sen and D. Kim, "Mode-Decomposition-Based Equivalent Model of High-Speed Vias up to 100 GHz," in IEEE Transactions on Signal and Power Integrity, vol. 2, pp. 74-83, 2023, doi: 10.1109/TSIPI.2023.3268255.

[32] M. Ouyang et al., "Novel Formulations of Multireflections and Their Applications to High-Speed Channel Design," in IEEE Transactions on Signal and Power Integrity, vol. 1, pp. 43-54, 2022, doi: 10.1109/TSIPI.2022.3176592.

[33] J. Tourné, "PCB007 MAGAZINE," Vertical Conductive Structures, Part1: Rethinking Sequential Lamination, pp. 88–93, Apr. 2019.

[34] J. Tourné, "PCB007 MAGAZINE," Vertical Conductive Structures, Part2: VeCS and Micro-machining, pp. 72–78, Jun. 2019.

[35] E. Hickey, J. Joan, and M. Catrambone, "PCB007 MAGAZINE," *Vertical Conductive Structures, Part3: Design Tool Techniques*, pp. 90–99, Aug. 2019.

[36] C. Li et al., "Undesired-resonance Analysis and Modeling of Differential Signals Due to Narrow Ground Lines Without Stitching Vias," 2023 IEEE Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMC+SIPI), Grand Rapids, MI, USA, 2023, pp. 688-692, doi: 10.1109/EMCSIPI50001.2023.10241719.

Authorized licensed use limited to: Missouri University of Science and Technology. Downloaded on January 16,2025 at 18:36:03 UTC from IEEE Xplore. Restrictions apply.