

Modeling of Power Distribution Network (PDN) Noise Coupling Induced Clock Phase Noise

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Abstract—Phase noise analysis is important to clock design. Noise sources of spurs shown on the phase noise result are challenging to find out due to the unknown source locations and coupling mechanisms. Noise from power distribution network (PDN) is one of the most troublesome sources. A behavioral modeling methodology is proposed to simulate the clock phase noise induced by PDN noise coupling for two different mechanisms: PDN-to-clock additive coupling and PDN-to-PDN up-conversion modulation. The thermal noise and 1/f flicker noise are simplified to provide a straightforward view of spur level. The model can be applied to both single-ended clock and differential clock. The result of the model can be used to compare the power spectral density of the potential noise sources and provides hypothesis on the potential noise source together with layout change simulation. The potential root cause of the spurs is analyzed. The mitigation methodologies of the phase noise are proposed and evaluated in the specific case, presenting a 34 dB suppression to the spurs shown on a differential clock phase noise.

Keywords—power distribution network, phase noise, source reconstruction, behavioral model, noise coupling mitigation

I. INTRODUCTION

Clock is one of the most important factors for radio frequency (RF) system. A clock synthesizer provides reference clock with different frequencies for various uses of other modules. Any spurious noise induced or coupled through power distribution network (PDN) can cause instability to the clock, which is called phase noise. Phase noise is well known to cause lots of problems in radar systems and communication systems [1]. The root cause investigation and modeling of phase noise are always popular but challenging topics.

Many aspects of noises are involved in phase noise analysis. The general noises occur in electronic devices are the thermal noise and the 1/f flicker noise [2, 3], forming the background noise. Thermal noise is the white noise associated with temperature and bandwidth, and 1/f flicker noise is a modulation noise in electronic devices [4]. The observation of the phase noise at the clock signal part are the phase fluctuation (or jitter) and magnitude instability in time domain [5].

Although suppressing the background noise improves the performance of the clock, engineers are more likely to be

plagued with spurious noise from unknown aggressors and coupling paths. Phase noise induced by the spurious noise is relatively high compared to background noise, resulting in much worse total jitter [6]. Several filter designs have been raised up to reduce phase noise [7, 8], while the prevention is limited when facing the noise coupling that bypass the filter.

The spurious noise sources vary in different scenarios. Power supply, heatsink and the crystal performance were investigated as the sources of phase noise at different frequency offsets from the clock frequency [5]. Among these factors, noise from power supply is of the most variation and hardest to distinguish. The noise carried by the power rails can be the lack of ability to handle sudden load changes for low-dropout (LDO) regulators [9], the fast-switching induced noise from voltage regulator module (VRM) [10] and PDN-to-PDN noise coupling [11]. Noise induced by PDN noise coupling can either be additively coupled or up-conversion modulation to the carrier frequency. Additionally, there could be multiple power rails existing in the whole system. All these possible reasons contribute to the complexity of finding out the intrinsic noise source.

Several approaches have been proposed for modeling the phase noise. The mathematical expression modeling of thermal noise with 1/f flicker noise varies with different designs of oscillators [3, 12, 13, 14]. Several measurement-based behavioral models are also proved to work well in different applications [15, 16]. These models, however, only provide the basic analysis of the background noise but lack the capability to deal with spurs analysis. Such specific spurs can be modeled by the close-loop response of the phase-locked loop (PLL) to the known phase noise seen on the crystal, oscillator and converter [17, 18]. The phase noise spectrum can also be simulated by Floquet theory through the known noise spectrum [19]. Nevertheless, the noise spectrum is often implicit to engineers. The knowns are only the profile of phase noise measurement and the system design.

Generally, the investigation of potential noise sources starts by some hypotheses on the aggressors. Phase noise modeling can be simplified by applying the noise source and the coupling ratio to find out the jitter spectrum [20, 21]. The methodology of noise source reconstruction can be the reversion of the methodology with the help of PDN simulation. With the analysis of different reconstructed potential noise sources, engineers can evaluate on the possible methods to improve the layout designs to enhance the clock

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performance. The behavioral model can also be applied to the layout improvements for validation.

This paper analyzes the coupling mechanism of PDN-to-clock additive coupling and PDN-PDN up-conversion coupling scenarios. A behavioral model is proposed to apply phase noise source reconstruction for background noise and spurious noise. The novelty of the model is the compatibility of evaluating all the potential sources of spurious noise with respect to the noise power spectral density. An example of differential clock phase noise, which is observed to be PDN noise coupled induced, is shown and modeled. A new hypothesis on the cause of spurious phase noise in differential signal is proposed based on the proposed model. The potential root causes are analyzed through the coupling mechanism. Several layout improvements for mitigating the PDN noise coupling induced clock phase noise are highlighted.

II. BEHAVIORAL MODEL FOR PDN NOISE COUPLING INDUCED CLOCK PHASE NOISE

The phase noise consists of background noise modeling and PDN coupled noise modeling. PDN noise coupling can either happen through PDN-to-clock or PDN-to-PDN coupling, which corresponds to different intrinsic noise frequencies due to the coupling mechanism. For PDN-to-clock direct coupling, the phase noises shown in single-ended clock and differential clock are caused by different reasons.

A. Background Noise

The mathematical calculation of thermal noise and 1/f flicker noise changes as oscillator design changes. However, as a behavioral model for PDN spurious noise coupling simulation, the background noise serves as the reference to the minimum measurable spurs. The requirement for modeling the background noise is to match the measurement result, with less restriction on the root cause of the background noise source. Therefore, the measurement-based behavioral model in [16] was applied to simulate the background noise.

For the single sideband phase noise simulation, each segment at different frequency offsets has different slopes, noise levels and corner frequencies. The target background noise is similar to Fig. 1 [22] with multiple segments representing phase noise caused by different modulations of white noise and flicker noise.

The trend of phase noise versus the frequency is similar to the bode magnitude plot. Therefore, the single sideband phase noise levels L_n in decibel can be expressed as:

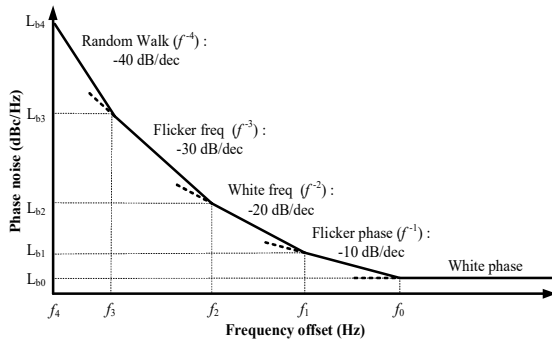


Fig. 1. Target background noise trends.

$$L_n = \begin{cases} L_{b0} & , \text{when } n = 0 \\ L_{bn} + k_n \cdot \log\left(\frac{f_n}{f - f_c}\right) & , \text{when } n = 1, 2, 3, 4 \end{cases} \quad (1)$$

where L_{b0} is the white phase level (noise trend is flat), L_{bn} is the starting phase noise for each segment, k_n is the slope in dB per decade for each segment, f_n is the start frequency of each segment, f_c is the carrier frequency (clock frequency) and f is the offset frequency from the carrier frequency.

Commercial simulation tool requires the corresponding noise voltage magnitude to excite the noise source. The conversion from the single sideband phase noise to noise voltage magnitude can be calculated mathematically. The relationship between power and voltage in both decimal and decibel are described as:

$$\frac{P_{SSB}}{P_{carrier}} = \left(\frac{V_{SSB}}{V_{carrier}}\right)^2 \quad (2)$$

$$\left(\frac{P_{SSB}}{P_{carrier}}\right)_{dB} = \left(\frac{V_{SSB}}{V_{carrier}}\right)_{dB} \quad (3)$$

where P_{SSB} and V_{SSB} denote the single sideband noise power and voltage magnitude, $P_{carrier}$ and $V_{carrier}$ denote the power and voltage magnitude at clock signal's carrier frequency.

Assume the carrier signal's voltage magnitude to be 1 V and set the noise simulation bandwidth to be 1 Hz. Single sideband phase noise L_n equals to half of the total noise power spectrum density. Combined with (2) and (3), the noise source voltage magnitude can be expressed as:

$$V_{SSB} = \sqrt{10^{\frac{L_n}{10}}} \quad (V/\sqrt{\text{Hz}}) \quad (4)$$

The background noise works as a noise floor to the spurs induced by PDN noise coupling. Although this paper is not aimed at finding the intrinsic reason for the background noise, the correct level of background noise from measurement provides a straightforward view of spurs' level and how the mitigation methodologies work at improvement stage.

B. PDN-to-clock Noise Coupling

PDN-to-clock directly coupling indicates an additive coupling. The coupling generally only occurs at one sideband.

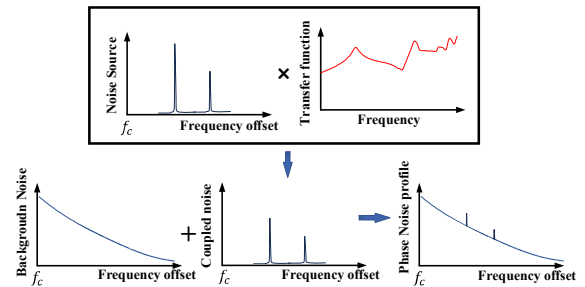


Fig. 2. PDN-to-clock noise coupling mechanism. Noise source couples to the clock signal additively through PDN, forming the phase noise profile with the background noise.

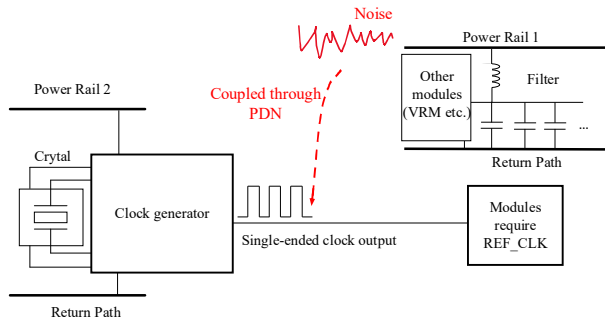


Fig. 3. Noise coupling on single-ended clock output through PDN.

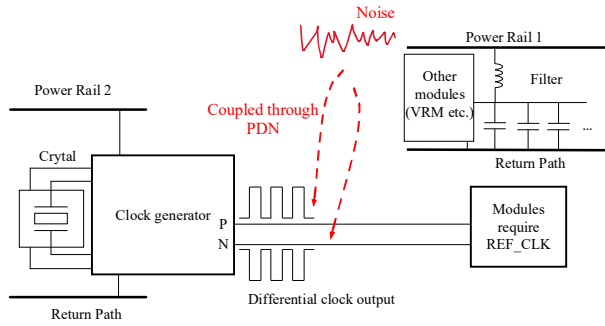


Fig. 4. Noise coupling on differential clock output through PDN. Ideally noise is canceled at REF_CLK end after being converted to unbalanced signal.

The noise induced on the power rail couples the noise through the PDN directly to clock through the coupling mechanism shown in Fig. 2. Same noise source can induce different phase noise result on the single-ended clock and differential clock.

1) Single-ended Clock

Single-ended clock signals has weaker robustness to the phase noise, as the coupling from the power rail directly happens on the clock channel. The coupling diagram is depicted in Fig. 3. The noise sources can be unintentional antennas, switching regulators, and high-speed digital integrated circuits (ICs). Layout design should take the potential noise sources or radiators into consideration. Enough noise shielding structure is required to avoid having the clock signal exposed to the noise source.

2) Differential Clock

Ideally, PDN noise coupled to the differential clock signals can be considered as a common mode noise. The coupling diagram for differential clock is depicted in Fig. 4. The noise on both positive (P) and negative (N) can be canceled out when converting the balanced clock signal to unbalanced clock signal.

However, there are some potential issues that can degrade the capability of the noise cancellation. If the noise source is close enough to the differential traces, the coupling to P and N can no longer be considered as identical. Consequently, the noise cannot be totally canceled out. Therefore, the power plane has to be well isolated from the clock generators and the differential clock traces. Another scenario is the improper design difference between P and N clock traces, such as skew and impedance difference. Unaware of the design differences can cause significant phase noise problems.

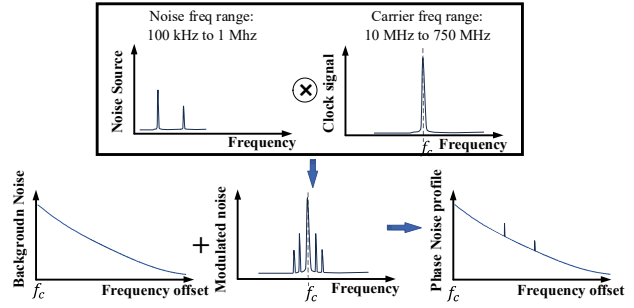


Fig. 5. PDN-to-PDN noise coupling mechanism. Noise couples from one power rail to another power rail, causing up-conversion modulation with the clock frequency and forming the phase noise profile with the background noise.

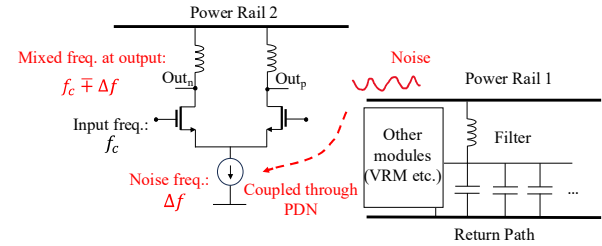


Fig. 6. An example of PDN-to-PDN noise coupling. Low frequency noise couples to another power rail through PDN shows up at current source and up-converts with the high frequency input signal to generate the mixed signal at the output.

C. PDN-to-PDN Noise Coupling

PDN-to-PDN noise coupling mechanism falls into the unintentional modulation process. Low frequency spurious noise can be coupled to the VDD rail of the clock differential output and up-convert to the phase noise frequency with the clock signal [23, 24]. The coupling mechanism is shown in Fig. 5. This coupling happens through devices such as field effect transistors (FET), bipolar junction transistors (BJT) and diodes. An example of noise coupling scenario is shown in Fig. 6. The MOSFET differential pair acts as a mixer. The low frequency noise from power rail 1 couples to power rail 2 through PDN. The physical mechanisms that cause the coupling could be the back-drilling caused holes on GND layers, not well isolated power rails and improper layout such as trenches or big non-plated holes. The victim power rail provides the power to the current source (through e.g. current mirror) and makes the noise appear in the current source. The noise from the FET source will then be mixed up with the gate input signal and the mixed signal is generated at both positive and negative output. Ground-bounce noise (GBN) [25] can also contribute to the noise shown at FET source. It's expected that the noise shows up on both P and N outputs as common mode noise, which can be reduced a lot after converting to unbalanced clock.

III. PHASE NOISE MEASUREMENT AND NOISE SOURCE RECONSTRUCTION

Phase noise measurement was performed on a differential clock output in Low-voltage Differential Signaling (LVDS) on a self-designed evaluation board for a commercial clock generator. The measurement setup followed the same setup as

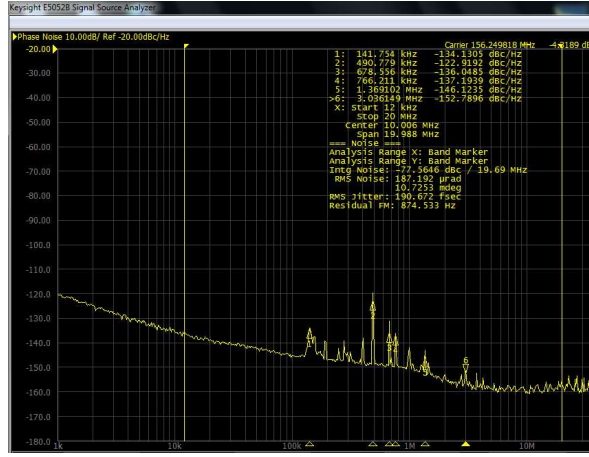


Fig. 7. Phase noise measurement result on a LVDS clock output on a self-designed evaluation board for a commercial clock generator.

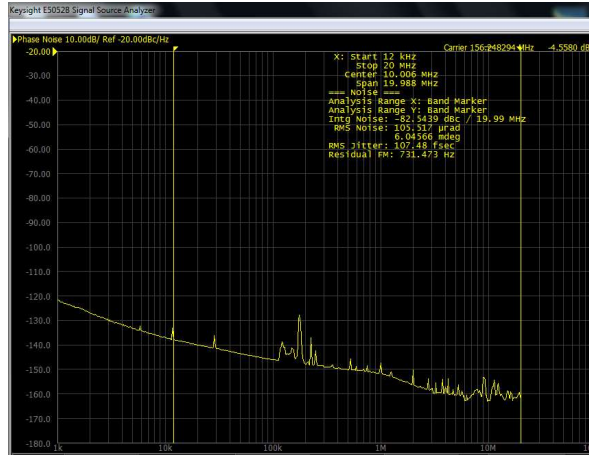


Fig. 8. Phase noise measurement result of the same clock on a new evaluation board with improved layout discussed in Section IV.

the differential phase noise measurement in [6] using a balun to convert balanced differential signal to unbalanced signal. The measurement was performed on Keysight E5052B Signal Source Analyzer. As shown in Fig. 7, the spurious phase noise is observed in the range of frequency offset from the carrier frequency (156.25 MHz) from 100 kHz to 5 MHz. Through the location and noise frequency analysis, 12 V power rail becomes the most suspicious noise source. With the great adjustment on the layout of shielding structure, the phase noise profile was greatly improved as shown in Fig. 8. It is confirmed that the noise comes from the power rails and coupled through PDN.

Among all the possibilities listed in Section II, PDN-to-clock directly coupling best explains why for differential signals the spurs show in Fig. 7 but disappear in Fig. 8. An example of using the behavioral model to provide an estimation on the noise source magnitude is shown below. The behavioral model is based on the coupling diagram shown in Fig. 4. Simulation and noise source reconstruction is performed in Advanced Design System.

The whole schematic of simulating phase noise on the differential trace is shown in Fig. 9. A noise source acts as the spurious noise source on the power rail side and perform PDN coupling through S-parameter simulation. The S-parameter is obtained by printed circuit board (PCB) simulation using

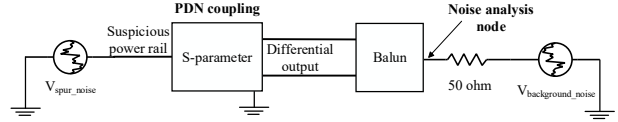


Fig. 9. Schematic of behavioral model for PDN noise induced differential clock phase noise simulation.

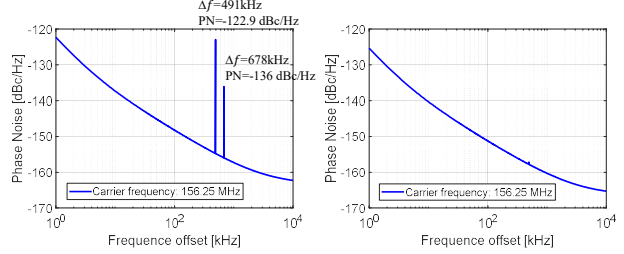


Fig. 10. Modeled background noise and spurs at $\Delta f=491$ kHz and $\Delta f=678$ kHz on the old PCB (left) and the modeled noise is applied to the new PCB (right). Noise sources are reconstructed to match the spurs shown in the measurement.

Ansys SIwave. A balun is connected to the differential clock output, with the other side terminated with a 50-ohm load (Signal Source Analyzer's input terminal) and the background noise source. Noise shown at the noise analysis node is an add-up result through superposition theorem. The reconstructed noise represents the equivalent noise shown on the power rail, which means no port impedance required for the noise source.

The background noise parameters (L_{bn} , f_n) are adjusted to match the same level as the measurement. The noise voltage magnitude of the spurious noise source can then be optimized to match the measured spurs. Here the spurs at $\Delta f=491$ kHz and $\Delta f=678$ kHz are selected. Modeled results are shown in Fig. 10. The optimized spur noise source voltage magnitudes are:

$$V_{\Delta f=491 \text{ kHz}} = 14.1 \text{ mV}/\sqrt{\text{Hz}} \quad (5)$$

$$V_{\Delta f=678 \text{ kHz}} = 3.1 \text{ mV}/\sqrt{\text{Hz}} \quad (6)$$

The reconstructed noise source follows the unit of the noise voltage magnitude. Noise level is related to the bandwidth. The background noise, such as thermal noise, are wide band, showing a pretty low level in $\text{nV}/\sqrt{\text{Hz}}$, while the spurs are more likely to be the narrowband interference. Therefore, the reconstruction result is an equivalent result from the behavioral model, which does not show the real noise signal magnitude. It can only be compared internally to find the most possible aggressors and used as a metric for validation of how the layout change improves the coupling issue.

The hypothesis of PDN-to-clock coupling to differential traces shows plausible results of having 12V power rail as the aggressor with noise at $f = 156.74 \text{ MHz}$ and $f = 156.93 \text{ MHz}$. The same model can be applied to PDN-to-clock on single-ended clock without balun and PDN-to-PDN coupling with a replacement of mixer to the balun used in the model. However, the PDN-to-PDN coupling with modulation is considered to be a more general interpretation of the measurement result, while it cannot provide a good explanation on the spurs for differential clock phase noise. The behavioral model requires further studies on simulating PDN-to-PDN coupling caused phase noise.

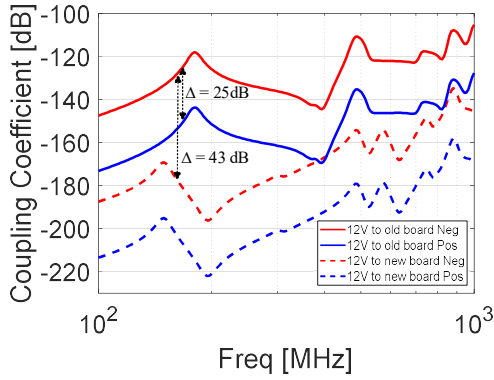


Fig. 11. Simulated coupling coefficient (S21 magnitude) from 12V power rail to the differential clock's positive output and negative output. Results for both old board and new board are presented.

IV. ANALYSIS ON POTENTIAL ROOT CAUSE AND MITIGATION METHODOLOGY BASED ON LAYOUT CHANGE

As introduced in Section II, improper layout designs can lead to the noise appearing on the differential output. The analysis can be performed on the detailed coupling ratio through S-parameter, as shown in Fig. 11. There is a large difference between the coupling to P and N on the old board. A variation of 25 dB shows up. The large variation indicates a large difference between the noise coupled to both positive and negative, resulting in the large degradation of noise cancellation.

There are two general methods to improve the noise rejection ratio to the phase noise:

- Adjust layout to make coupling to positive equals to coupling to negative.
- Improve shielding to bring down the whole levels of both coupling to positive and negative.

The variation of coupling between the old and the new board are also compared in Fig. 11. The difference of 43 dB at around 156.74 MHz and 156.93 MHz shows that the whole levels for coupling to both positive and negative drop and accounts for the mitigated phase noise.

In practice, engineers prefer to avoid excessive layout change which may involves more unknowns to other system characteristics and performances. The detailed layout change is shown in Fig. 12. Here all the mitigation methodologies are listed out and compared through reversion simulation to evaluate the efficiency of the mitigation technologies under this specific case.

A. Cutout of 12V Power Plane under the Clock Generator Region.

The external power rails are generally the noisiest sources. When a power plane is needed, generally it's placed at inner layers and isolated from signal layers with ground return planes. However, the regulator modules have to be somewhere on the top or bottom layer, so the coupling from the power parts is inevitable. Besides, holes, apertures and trenches on the PCB make the interference coupling and radiation to be worse. The void region on the ground return plane reduces the shielding performance. Anti-pad for the vias could also be a potential reason for noise coupling at high frequency.

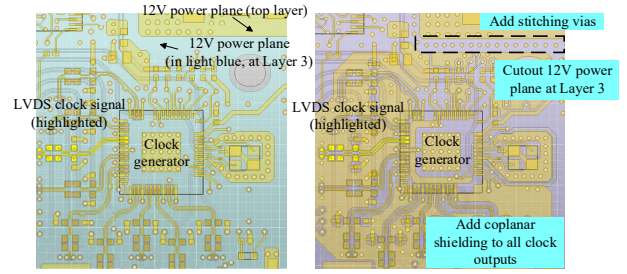


Fig. 12. Layout comparison between old PCB (left) and new PCB (right).

Engineer should avoid unnecessary dig-through and good arrangement of sensitive modules away from holes.

A rough but effective way is to cut out the power plane region underneath the vulnerable modules. The method moves the potential noise source far from the victim, while it may increase the layout difficulties and affect PDN impedance.

B. Adding Stitching Vias between the 12 V Power Plane on Top Layer and Clock Generator

Stitching via provides a lower impedance return path, shielding between the aggressor and victim and mitigation to the radiation electromagnetic interference (EMI) [26]. The placement of stitching vias is important in high-speed application to ensure a good shielding while maintaining the impedance of signal traces and vias at proper distance. The stitching vias used in this application around several hundreds of MHz are not of that excessive concerns as long as the vias do not occupy too much space and not too close to the signal traces. In this application, stitching vias are placed between the top layer 12 V power area and the clock generator area.

C. Provide coplanar shielding structure

The coplanar shielding provides good isolation to the coupling between the interconnects and additional heat sinking [27]. The coplanar pouring all over the outer layers (i.e. top and bottom layers) generally performs a good impact to the noise mitigation. The main concerns are the influence to the signal trace impedance and small island which acts as a patch antenna to radiate.

To evaluate the mitigation methodologies in this application, reversion simulations are done by reverting layout changes back to old version separately (i.e. revert one layout change but keep the other two the same as new version) and compare the coupling ratio through SIwave simulations. The result is shown in Fig. 13. Since every reversion is done separately, the influence of mitigation methodologies is straightforward to be analyzed without interaction between each other. According to the result, the stitching vias show the most impact to the magnitude coupling. The power plane cutout shows more impact to the trends shape of coupling ratio regarding the frequency, which is most likely due to the PDN impedance change. The coplanar shielding does not show large impact at this stage. The result only indicates the impact in the specific case. Impact varies in different scenarios because the noise source location, frequency band and coupling mechanism are different.

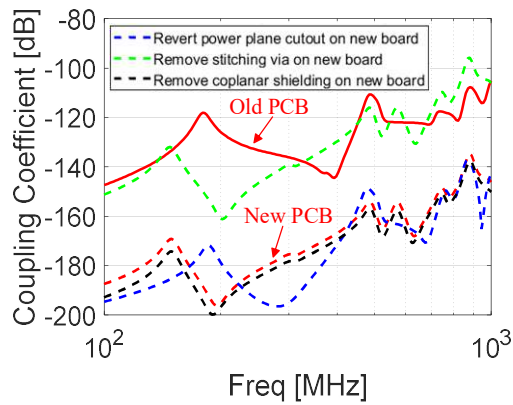


Fig. 13. Reversion simulation result of coupling coefficient (S21 magnitude) from 12 V power plane to the negative of the differential clock output.

V. CONCLUSION

PDN noise coupling induced phase noise was analyzed in two different coupling mechanism. PDN-to-clock coupling shows an additive coupling to the clock. Scenario of both single-ended and differential clock signals were analyzed. PDN-to-PDN coupling shows an up-conversion modulation to the clock signal. A behavioral model of PDN noise coupling induced phase noise with background noise was proposed to evaluate the potential noise source location and the noise power spectral density. An example of analyzing spur noise source of differential clock outputs was provided to show the performance of reconstructing noise source power spectral density due to PDN-to-clock coupling. The potential root cause was analyzed, and mitigation methodologies based on the layout change were listed out and ranked for the specific case. The behavioral model provides an internal comparison methodology to find out the potential noise source among different power rails and evaluate on the performance of noise mitigation by layout change.

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