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Double Sided Conduction in N:1 Transformers

Alyssa Brown, Michael Solomentsev, Champers Fu, Odinaka Okeke, Alex J. Hanson
University of Texas at Austin
2501 Speedway, Austin, TX 78712, USA
{rileyalyssa3, mys432, champers.fu, odinaka, ajhanson}@utexas.edu

***Abstract*—In the high-frequency regime (HF, 3-30 MHz), the proximity effect in transformers can lead to large losses due to undesired current crowding and circulation. Litz wire's efficacy does not scale well past a few and interleaving solid conductors leaves much conduction area underutilized. Field-shaping techniques have recently been proposed to achieve double-sided conduction, resulting in twice as much conduction area in interleaved solid-conductor layers compared to normal interleaving. While double-sided conduction has been demonstrated in 1:1 transformers, we explore in this paper the application of the double sided conduction design methodology to non-unity turns ratio transformers. We validate our conclusions with a 4:1 double sided conduction foil-wound transformer optimized for operation at 13.56 MHz, and compare it to a standard-interleaved foil-wound transformer, a magnet wire-wound transformer and a litz-wound transformer. We find that it is possible to achieve double sided conduction in non-unity turns ratio transformers and that they can achieve better performance than standard interleaving, magnet wire and litz wire in the MHz regime.**

***Index Terms*—High Frequency (HF), Magnetics, Performance Factor, Core Loss, Copper Loss, Power Conversion, Transformers**

I. Introduction

Motivated by the desire for lower volume, higher power density, and higher efficiency, power converters have been designed to operate at higher switching frequencies. Recently, the development of wide-bandgap devices has caused magnetic components to become the bottleneck on high-performance, high frequency power converter design [1]. Magnetic components (inductors and transformers) are subject to a variety of magnetic effects which cause their losses to scale nonlinearly with frequency, making their design difficult and limiting miniaturization.

At high frequencies, electrical current tends to crowd toward regions of high H-fields - this phenomenon is often known as the skin and proximity effect. At best, this reduces the available conduction area significantly and at worst, causes large circulating currents and loss. It is thus important to design to mitigate these effects.

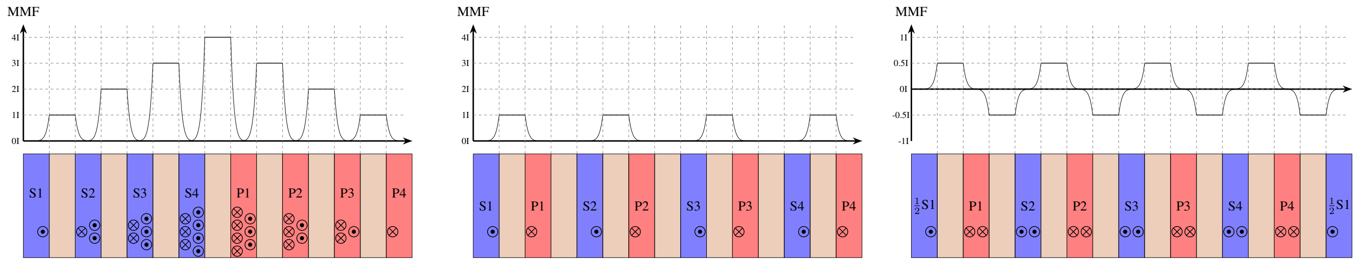
One common approach is to use litz wire, but this does not always work at high frequencies: Even 48 gauge litz wire strands, among the thinnest that are commercially available and already too expensive for many cost-constrained applications, have a diameter of 32 microns which equals a skin depth at approximately 4 MHz. Above this point, litz may not mitigate, and potentially can even increase copper losses [2]–[5]. Therefore, litz wire is not a practical solution as frequencies push into the multi-MHz regime.

Another often-used approach is to interleave primary and secondary layers to minimize build-up of H-fields between conductors [6]. In the best case state-of-the-art approach ("full interleaving") at the high-frequency limit, such interleaving results in non-zero H field in every other inter-layer gap, causing current to conduct in one skin depth on one side of each conducting layer (single sided conduction), potentially leaving large sections of the winding window underutilized. Moreover, it is often not clear how to practically achieve interleaving, especially in cases where the turns ratio is non-unity, leading to the use of partial interleaving schemes. It is even more difficult to practically implement such winding patterns at high frequencies, where terminations and interconnects can lead to significant additional, unmodeled losses [7].

The concept of "double sided conduction" (DSC) has been developed in both inductors [8] and 1:1 transformers [9] wherein the H field on each side of a layer is designed to be equal and in opposite directions, causing current to flow in a skin-depth layer on both sides of the layer, reducing copper loss by as much as 50%. It may be of particular interest to extend this methodology to N:1 transformers, which are commonly used in high step-down or step-up converters, such as wall chargers for portable devices [10], or for high-current applications. We present a methodology for achieving DSC in such transformers. We validate our theoretical findings with FEA simulations and through high-frequency AC resistance tests [11] at 13.56 MHz of a 4:1 double sided conduction transformer, a 4:1 transformer with a simply-paralleled secondary, and two conventionally wound 4:1 transformers made from litz and magnet wire respectively. We demonstrate that litz wire indeed proves untenable at 13.56 MHz, while double sided conduction can achieve high performance. We perform a similar test at a higher rms current and take thermal measurements to further validate our findings.

II. Double Sided Conduction

Transformers often consist of layers of conductors or groups of conductors arranged in layers (i.e. stacks of concentrically wound wires). The H field between layers can be found from Ampere's law applied in a loop around all of the layers to the left or right of the space in question. In Fig. 1, cross-sections of transformer windings with unity turns ratios are paired with their MMF diagrams (where $MMF \propto H$), assuming high frequency operation. All conductors in a specific winding (except for the DSC case's first and last turns) are connected in series.



(a) Non-Interleaved (b) Standard Interleaving (c) Double Sided Conduction

Fig. 1: MMF distribution diagrams of unity turns ratio transformers with various winding configurations, showing how DSC results in MMF fields on both sides of each conductor, leading to more even current distribution and lower loss.

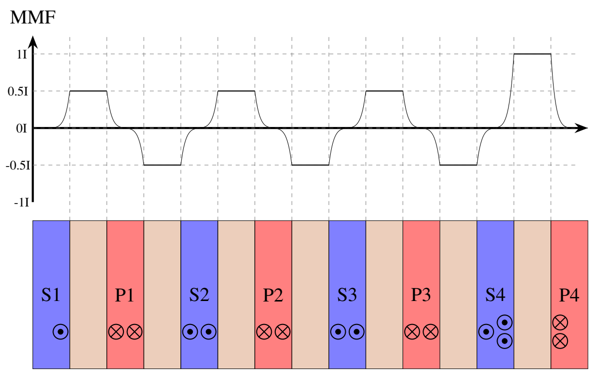


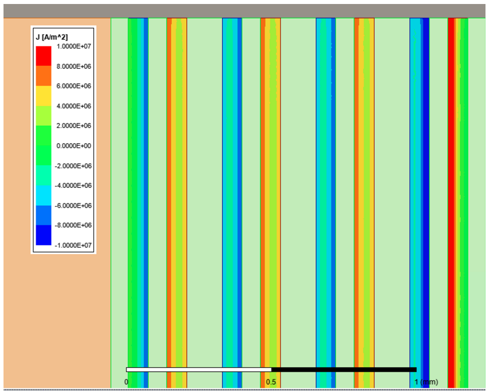
Fig. 2: MMF distribution diagram from a 4:1 turns ratio transformer, with an interleaved series-connected primary and parallel-connected secondary, exhibiting double sided conduction on many of its conductors.

In Fig. 1a, MMF rapidly builds up between layers carrying net current in the same direction. H-fields of the same polarity on both sides of a layer cause current to flow in opposite directions, leading to significant circulating current within the layer and thus loss. One mitigation strategy is to interleave or alternate primary and secondary layers to prevent the build up of loss inducing H-fields as shown in Fig. 1b, which has no circulating currents in any conductor. However, even fully-interleaved structures such as the one shown only have H-fields on only one side of each copper layer, and therefore have current on only one side of each conductor. The double sided conduction technique (Fig. 1c) arranges the conductors in a way that enforces equal-magnitude and opposite-direction H fields on either side of each conducting layer, resulting in two skin depths of same-direction current in each layer. This technique can reduce copper losses by as much as 50% relative to standard interleaving (note that the first and last layer in Fig. 1c are in parallel and experience one skin depth of conduction each; taken together, they constitute a single layer with double sided conduction).

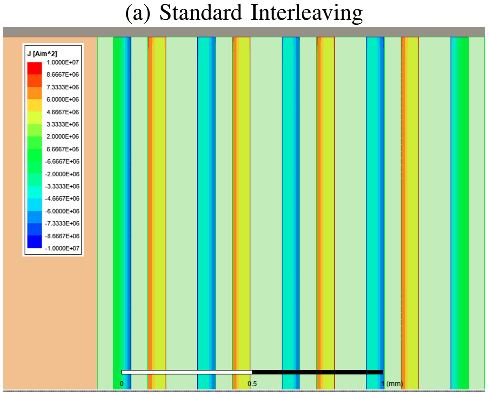
The MMF diagrams in Fig. 1 assume that the net current in each layer is one unit (or half of one unit for the paralleled inner/outer layers in the DSC case), which is true for 1:1 transformers. For non-unity turns ratio transformers to achieve interleaving or double-sided conduction, some layers must necessarily be in parallel and may or may not share net current equally [12], [13]. Consider the case of a transformer with a 4:1 turns ratio, implemented by interleaving 4 turns of a series-connected primary with 4 turns of a parallel connected secondary, as shown in Fig. 2. Analysis indicates that in an ideal case (with zero net ampere-turns in the core), this interleaved case (Fig. 2) actually has equal current distribution (i.e. double sided conduction) on both sides of five of its eight conductors, which is validated by the FEA simulations shown in Fig. 3b. This occurs because the outermost paralleled conductor (S4) carries 1.5 units of current, while the innermost paralleled conductor carries 0.5 units of current. This results in significantly less loss than in a unity turns ratio, traditionally interleaved transformer, despite no special care having been taken to achieve double-sided conduction. A 4:1 double sided conduction transformer could be constructed by simply adding an additional parallel connected secondary turn to the outside of the interleaved version (after P4), and would result in an equal MMF diagram to Fig. 1c. For the 4:1 case, we predict a 20% difference in loss between the simply paralleled and the double sided conduction designs, based on the ideal current distribution analysis. This generalizes to a $1/(N+1)$ reduction in loss in an $N:1$ transformer, a more critical difference for lower turns ratios.

This phenomenon is apparent in FEA simulations of a standard 4:1 interleaved transformer and a DSC transformer, built in ANSYS Maxwell and shown in Fig. 3. FEA confirms a 20% reduction in loss from the paralleled to the DSC designs.

We note that in both structures' simulations, current does not distribute exactly as predicted between the first and last paralleled layers, leading to slightly uneven current distribution within conductors and excess loss. This is likely due to uneven interwinding reluctances (due to uneven cross-sectional area between the inner- and outer-most windings) creating unbalanced H-fields. The equivalent MMF diagrams to the FEA simulations are shown in Fig. 4. This results in slightly higher *absolute* loss, but results in as-predicted relative loss between the two structures, as both are equally effected by this phenomenon.

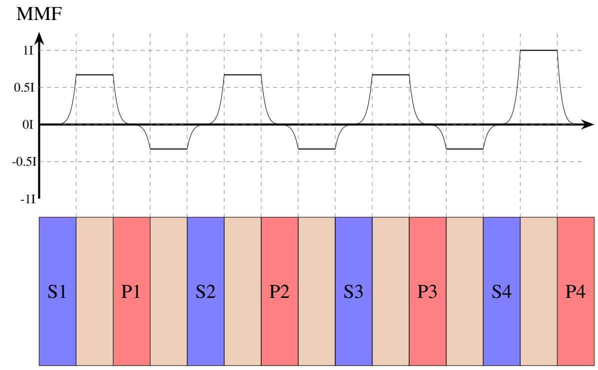


(a) Standard Interleaving

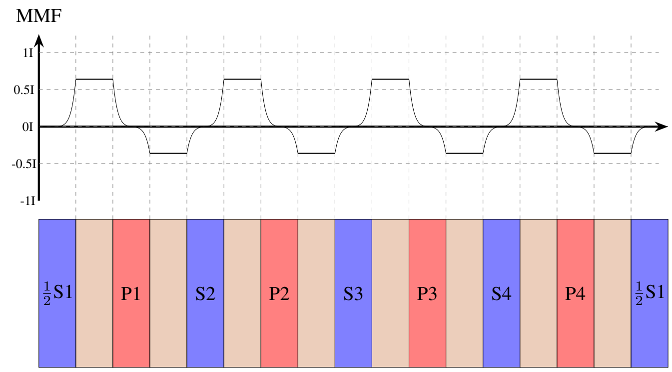


(b) DSC

Fig. 3: FEA simulations of (a) Paralleled 4:1 transformer and (b) double sided conduction 4:1 transformer. Due to the parallel connections, the paralleled transformer experiences current sharing that produces double sided conduction for the inner conductors.



(a) Standard Interleaving



(b) Double Sided Conduction

Fig. 4: MMF distribution diagrams reflecting slightly uneven current distribution due to uneven current sharing between first and last paralleled layers.

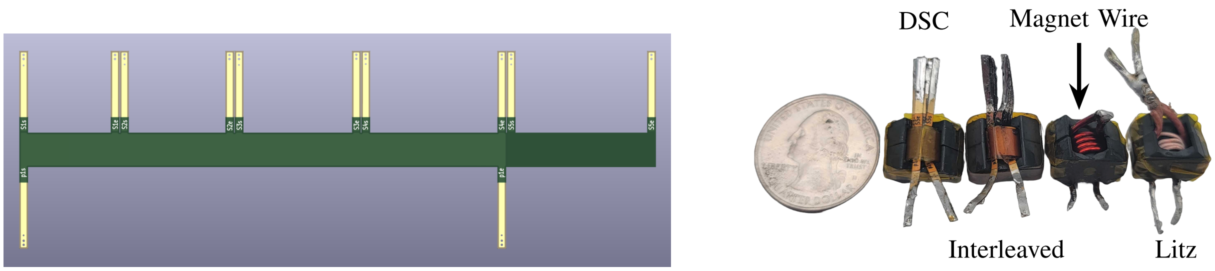
III. Experimental Validation

To verify the low loss and high power density of the proposed design, we construct four 4:1 transformers, all utilizing the same K1 material RM5 core set with no gap. We build two 'conventionally' wound transformers: one using magnet wire (19 AWG primary, 16 AWG secondary) and one using litz wire (1000/48 AWG ($\approx$ 24 AWG total) on the primary, 175/46 AWG ($\approx$ 19 AWG total) on the secondary) which were the largest litz strands available that could fit in the core. We use flexible PCB winding for the other two structures: one that uses conventional interleaving (i.e. a series connected 4-turn primary and a 4-turn simply-paralleled secondary) and another that uses the proposed double sided conduction method. The DSC and the simply-paralleled transformers are both built using 2oz copper layers within the 2-layer flexible PCB, which has a total length of 10.9 cm for the DSC winding and 8.5 cm for the simply-paralleled winding. The flexible PCB transformers can be readily assembled by wrapping the PCB winding tightly around a bobbin, sliding it onto the core, and soldering the associated tabs together. The standard interleaved and double sided conduction transformers are designed for 13.56 MHz operation in order to clearly see the difference between one versus two skin depths worth of loss with a limited copper thickness of 2 oz. The litz and wire transformers are built for comparison following standard design practice.

As shown in Fig. 5a, the DSC PCB consists of 4 turns in series on the front copper to form the primary (P) winding and 5 turns in parallel on the back copper to form the secondary (S) winding, giving an interleaved structure of 0.5S-P-S-P-S-P-S-P-0.5S as discussed previously. The simply-paralleled transformer is equivalent to removing the last turn of the secondary on the flexible PCB thus creating only 4 turns in parallel, giving an interleaved structure of S-P-S-P-S-P-S-P, as would be done with conventional interleaving. By using the front and back copper layers of the flexible PCB, interleaving is easily achieved and aligned tabs are used to create the parallel connections and terminations. The hardware prototypes are shown in Fig. 5b and their measured inductance values are shown in Table I. We note that by virtue of their extremely tight wrapping, the flexible PCB transformers (both the standard interleaved and DSC versions) have very low leakage inductances relative to their conventionally wound counterparts.

A. AC Resistance Measurements

We use the series resonant loss measurement setup described in [11] in order to characterize the ac resistances of



(a) (b)

Fig. 5: (a) Model of flexible pcb used for the DSC transformer and interleaved transformer windings. The use of front and back copper layers makes interleaving the layers very easy when wrapping the windings around the center post, even with a non-unity turns ratio. (b) Assembled prototype RM5 litz (right), magnet wire (second from the right), interleaved (second from the left) and DSC (left) transformers with a U.S. quarter for scale.

the four prototypes at 13.56 MHz. In each case, we short the secondary terminals, and resonate the primary referred leakage inductances with a series capacitor. The loss measured will be a function of the self and mutual resistances of the transformer windings, as well as whatever core loss the structure experiences at that frequency and drive level. In this particular (secondary-shorted) test, core losses are typically small and the copper loss is reflective of the losses that gapless transformers (primary current in phase with secondary current) will experience when used in typical power converter operation.

The results from the resonant loss characterization experiments are shown in Table I. We represent the loss characterization measurements as equivalent resistances, each taken at approximately 13.56 MHz with 2A driving current. Both the standard interleaved and double sided conduction transformers exhibit significantly lower loss than the litz transformer. Similarly, we see that the magnet wire transformer performs better than the litz wire but still experiences more than double the loss of the DSC and standard interleaved transformers. This experiment highlights the need to carefully examine conduction patterns in solid conductors at high frequency, as it is unlikely that litz wire can be used to suppress high-frequency effects.

The DSC transformer exhibits 25% lower loss than the standard interleaved case which agrees reasonably well with the earlier FEA simulations that suggest a 20% improvement in performance. The difference is likely due to termination and interconnect losses which can be significant in high frequency transformers, particularly with flat conductors [7].

We further verify our results through the use of a parallel resonant test. The experimental setup is described in appendix A. From this test, we can extract the equivalent R_{ac}, just as in the series resonant case, but now at a higher drive current. The 100W power amplifier used to drive these resonant circuits prefers to operate at a load of 50Ω. In the series resonant case, the combined impedance is low which can cause distortion at high gains of the power amplifier. In this test configuration, there can also be significant high frequency noise on the input waveform from the power amplifier. To filter this, there is typically some filtering capacitor attached to the input node of the series resonant test circuit. The downside of this filtering capacitor is that it takes current away from the main resonant path, thus limiting the driving abilities. In the parallel resonant test, the combined resonant tank appears as a high impedance to the power amplifier and thus suffers from less distortion at higher gains. There is also significantly more current circulating in the resonant tank therefore allowing AC resistance measurements to be measured at higher drive currents.

The results from the parallel resonant loss characterization tests are shown in Table I as well. The measurements for the double sided conduction, magnet wire, and standard interleaved transformers are taken at approximately 13.56MHz with a 4A RMS driving current. The litz wire transformer was not capable of operating at this higher current due to it overheating and sometimes melting the bounding material off thus shorting the turns. We see that there is agreement between the parallel and series resonant measurements in terms of performance. The difference in measured R_{ac} values is due to the increase of core loss in the system at higher drive currents therefore leading to higher measured values in the parallel resonant case. Nevertheless, we once again see the significant difference between the double-sided conduction transformer and its counterparts.

B. Thermal Measurements

We use the parallel resonant test configuration described in appendix A to drive the the transformer at 2A RMS and 13.56MHz while capturing the transformers' winding temperature using a thermal camera. The experimental set up also included a fan which was had the same fan speed and was placed equidistant for each case. Fig. 6 shows the temperature progression of the transformers over a 5 minute measurement period. After approximately 1 minute, each of the transformers reached their steady state temperatures. Fig. 7 depicts thermal images of the transformers at steady state operation. Although the thermal measurements are prone to some error when taken in open surroundings, these measurements and images

Transformer	Primary Referred L_{lk} (nH)	Series Resonant (SR) Measured R_{ac} (Ω) @ 2A rms	SR Measured P Loss (W)	Parallel Resonant (PR) Measured R_{ac} (Ω) @ 4A rms	PR Measured P Loss (W)
Magnet Wire	168	0.63	2.02	0.94	15.6
Litz	370	1.19	4.25	-	-
Standard Interleaved PCB Winding	80	0.39	1.59	0.42	6.16
DSC PCB Winding	52	0.21	0.70	0.21	3.95

TABLE I: Measured inductance and high-frequency ac resistance from the four experimental transformers, showing the advantageous performance of the DSC conduction design over conventional litz and wire-wound and standard interleaving PCB transformers.

Transformer	Maximum RMS Drive Current (A)	Limit
Magnet Wire	4.59	Failure
Litz	3.53	Failure
Standard Interleaved PCB Winding	6.68	Failure
DSC PCB Winding	8.44	150^{o}C

TABLE II: Measured maximum power transferable with each transformer before reaching 150^{o}C temperature or physical failure.

provide a nice visual reference for comparing the operation of the transformers. Clearly, the DSC has the lowest steady state operating temperature which once again aligns with our analysis.

C. Destructive Testing

As a final form of validation, we measured the approximate maximum power processing capability of the transformers. We increased the drive current until a thermal limit of 150^{o}C or there was physical damage from heat dissipation. Table II has the results from this experiment. The maximum drive currents indicate the power level that each transformer is capable of processing before faulting. The same trend is observed in this setting as well, with the double sided conduction transformer outperforming the rest with a maximum current of 8.44A RMS, a 20% increase from the standard interleaving case.

IV. Conclusion

High frequency magnetic effects can lead to current crowding and circulation in high frequency transformers, limiting their performance and overall converter efficiency. This work presents a design methodology for achieving extremely high utilization of available copper area in non-unity turns ratio transformers, deemed double sided conduction. The approach is easily assembled using flexible PCB windings, and is experimentally verified to have high performance in the high frequency regime, exceeding that of traditionally interleaved and wire-wound designs. This indicates promise for the DSC strategy to enable high efficiency, high thermal density HF power converters.

Appendix A
Parallel Resonant Measurement Setup

A series resonant measurement method has been frequently used in literature to measure the performance of magnetic

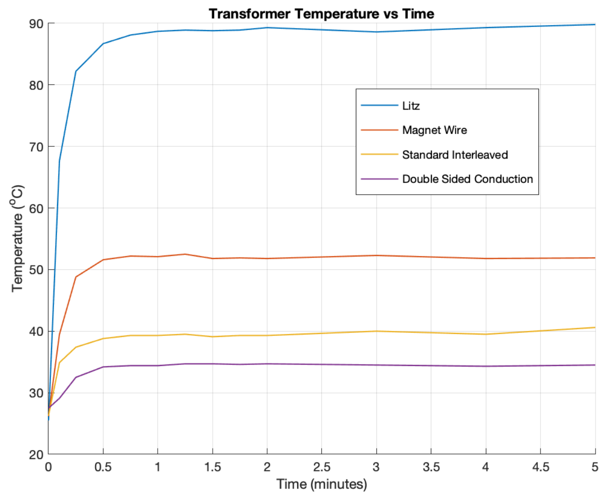
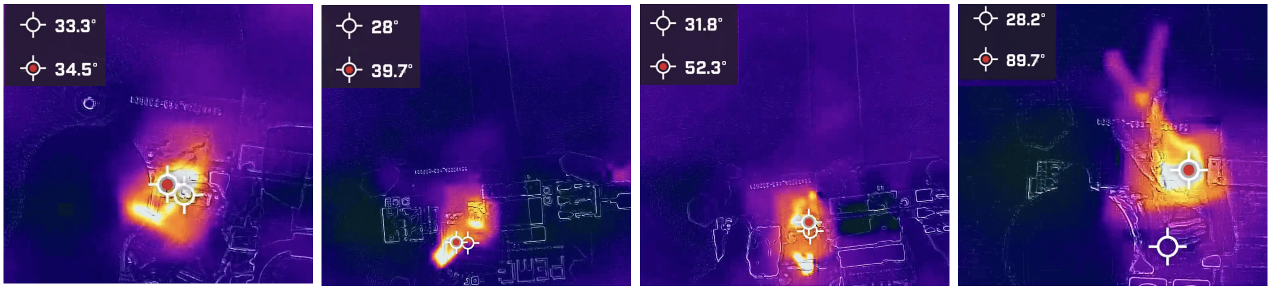


Fig. 6: Thermal curves from transformers tested at 2A and 13.56 MHz, showing the high performance of the DSC design.

materials, the quality factor of high frequency inductors, and characterize high frequency transformers [8], [11], [14]. This method places a capacitor in series with the device under test, selected to resonate at a frequency of interest. At the frequency of interest, the ratio of the capacitor voltage and the input voltage is directly proportional to the resistive impedance in the system, allowing for high accuracy, high frequency measurement. This method is advantageous for many reasons, but suffers from several drawbacks. Since an RF power amplifier is typically used to generate the HF excitation into the system, it may be difficult to produce high current measurements: When driving small impedances, RF power amplifiers typically cannot generate low distortion, high current signals, limiting measurement quality and accuracy. This is especially important for structures which need to be characterized at high current levels, like those presented in this work.

For this reason, we utilize a novel, parallel resonant measurement setup, shown in Fig. 8. A capacitor is again chosen to resonate with the DUT, but is instead placed in parallel with the device. At the resonant frequency, the power amplifier thus sees a parallel resonance with much higher impedance than the equivalent series resonance, allowing for much higher drive current.

By taking measurements of V_{block} and V_{res}, we can extract



(a) DSC. (b) Standard Interleaved. (c) Magnet Wire. (d) Litz Wire.

Fig. 7: Thermal images of the transformers at their steady state operating point with 2A RMS drive current.

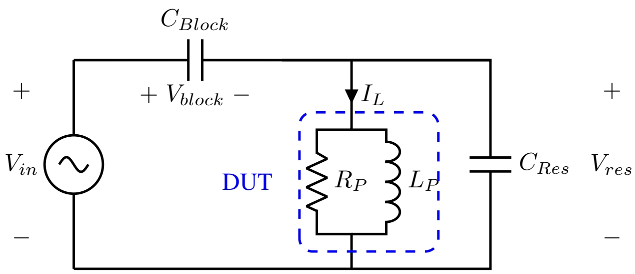


Fig. 8: Schematic of the parallel resonant measurement setup, used to make high current, high frequency loss measurements.

the properties of the DUT:

$$R_P = \frac{V_{res}}{I_{in}} = \frac{|V_{res}|}{\omega C_{block}|V_{block}|} \tag{1}$$

$$|I_L| \approx |I_{C_{res}}| = \omega C_{res}|V_{res}| \tag{2}$$

Note that the inductor current is not exactly the resonant current through the capacitor, and in fact is the difference between $I_{C_{res}}$ and the current through the blocking capacitor - however $I_{C_{block}}$ is both typically relatively small and 90° out of phase with $I_{C_{res}}$, so equation 2 is a convenient and close approximation.

Typically, magnetic structures are modeled as an inductance (L_S) in series with a resistance (R_S). This analysis utilizes the equivalent parallel version of this model, with a parallel inductance (L_P) and resistance (R_P). The models are mutually compatible with one another, and the transformations between the two can be readily calculated by equating the impedances of the two models (i.e. $j\omega L_S + R_S = j\omega L_P||R_P$). For convenience, we show the transformations from the parallel to the series equivalent circuit below, and note that for typical quality factors ($Q >> 1$), $L_P \approx L_S$.

$$L_S = \frac{L_P R_P^2}{\omega^2 L_P^2 + R_P^2} \tag{3}$$

$$R_S = \frac{\omega^2 L_P^2 R_P}{\omega^2 L_P^2 + R_P^2} \tag{4}$$

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