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NVMSurvey: Recent Advances and Comparative Analysis of Emerging Non-Volatile Memories (eNVMs)

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Abstract

Emerging non-volatile memories, specifically FeFET, PCM, RRAM, and STT-MRAM, promise significant advances in energy-efficient on-chip storage. Our research evaluates most recent (2020-2023) publications of such eNVMs against both optimistic and pessimistic projections sourced from 2016 to 2020 research using NVMExplorer, an open-source eNVMs simulator. Significant findings include FeFET's low area, PCM's improved energy efficiency and reduced read latency, and the evident advancements in STT-MRAM and RRAM. Moreover, we evaluate the potential benefits of recent eNVM solutions as memory resources for Deep Neural Network (DNN) accelerators and find that recent advances in RRAM and FeFET devices offer improved memory power and density for ResNet26 image processing. Overall, our study presents and analyzes continued research efforts on eNVM technologies as promising contenders to augment and replace conventional memory technologies.

1. Introduction

The exploration of emerging non-volatile memory technologies like FeFET, PCM, RRAM, and STT-MRAM, over the last three years offers a glimpse into the continuing evolution and innovation of memory technologies. This study dives deep into their performance and their potential to supplant conventional memories such as SRAM and DRAM by modeling and evaluating recent advances against standards from prior work based on 2016-2020 publications. Using DNN benchmarks, we also assess how these eNVMs can be optimized to improve the power efficiency of modern computing tasks.

2. Methodology

We reviewed eNVM-focused papers from ISSCC, IEDM, and VLSI (2020-2023), extracting cell configuration data. Based on the obtained data, we used NVMExplorer [10] to model array-level characteristics. We simulated eNVMs against six key optimization criteria mainly focused on energy, density, and power optimization. We then analyzed key metrics: Read Latency vs. Read Energy, Write Latency vs. Write Energy, and Area vs. Area Efficiency. Key findings on standout eNVMs are discussed in Section 3.1. We validated our simulations by comparing them against published values of fabricated test chips (see Section 3.3). Additionally, we evaluted applicability to DNN use cases using ResNet26, each storing either weights only or both weights and activations, at a 2 MB memory size; detailed results are presented in Section 3.2.

3. Results

3.1. Memory Array Characterization

We evaluated key metrics across technologies at iso-capacity (1MB) using published cell characteristics as inputs to NVMExplorer. We compared these results from 2020-2023 publications to NVMExplorer's provided optimistic and pessimistic projections per technology based on 2016-2020 publications. Our analysis highlights the top-performing technologies across several optimization criteria. Our data shows that recent examples of FeFET outperforms pre-existing pessimistic cell assumptions in area, generally achieving array characteristics close to prior optimistic assumptions, as depicted in Figure 1 (a). As per Figure 1 (b), recent advances in PCM surpass even optimistic prior characteristics, demonstrating reduced read latency and lower energy consumption. Meanwhile, Figure 1 (c) underscores the recent progress in STT-MRAM, showing examples of increased energy efficiency and quicker write times, consistently aligning with optimistic expectations.

3.2. DNN Inference Simulation

To evaluate recent eNVM configurations as potential replacements to SRAM in the deep learning accelerator architecture studied in [10], we evaluate 2MB capacity eNVM arrays under memory traffic patterns corresponding to a variety of ResNet26 image processing tasks.

Figure 2 presents the results of DNN inference simulations in which only weights are stored in eNVM array (2020-2023), leading to a read-only traffic during inference. We excluded those points that failed to meet software requirements (completing 60 frames-per-second image processing).

Table 1 compares the optimal eNVMs choices for three other DNN benchmarks based on DNN inference simulation results from 2016-2020 and 2020-2023 publications. It is noteworthy that FeFET has become the optimal choice for all benchmarks in terms of area. PCM, on the other hand, still performs the best for weights-only benchmarks, while RRAM has become the top performer for weights-and-activation benchmarks, surpassing STT.

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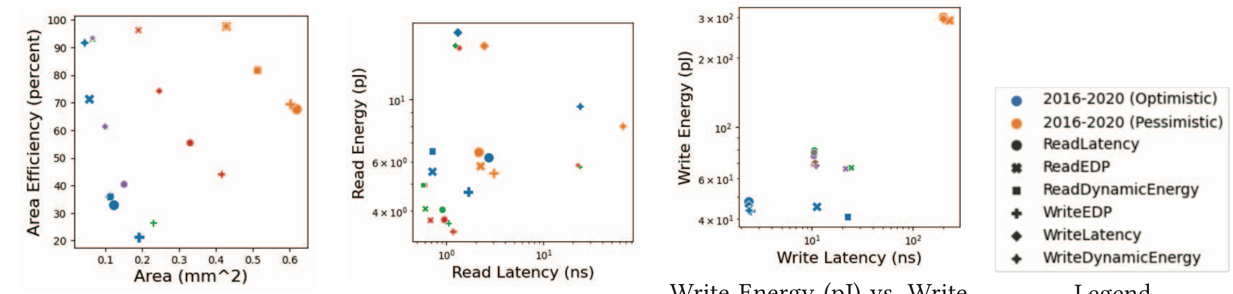

Area Efficiency (%) vs. Area (mm^2), FeFET. Green: [8], Red: [6], Purple: [9]

Read Energy (pJ) vs. Read Latency (ns), PCM. Green: [2],Red: [5]

Write Energy (pJ) vs. Write Latency (ns), STT. Green: [1], Red: [4], Purple: [3], Brown: [7], Pink: [12], Grey: [11]

Legend

Figure 1: Example Array Characteristics for 1MB eNVMs using cell characteristics derived from 2020-2023 publications compared to existing optimistic / pessimistic example configurations from [10]

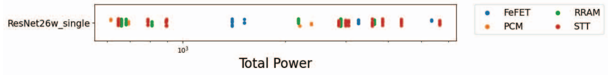

Figure 2: Total Power of eNVM-based weights memory for ResNet26 single-task image classification (2020-2023 data)

TABLE 1: Optimal eNVMs for each benchmark

Operating Mode	Priority	2016-2020	2020-2023
Single (Weights only)	Power	PCM	PCM
Single (Weights only)	Area	FeFET	FeFET
Single (Weights & Acts)	Power	PCM	**RRAM**
Single (Weights & Acts)	Area	FeFET	FeFET
Multiple (Weights only)	Power	PCM	PCM
Multiple (Weights only)	Area	STT	**FeFET**
Multiple (Weights & Acts)	Power	STT	**RRAM**
Multiple (Weights & Acts)	Area	STT	**FeFET**

4. Validation

We conducted a validation study on PCM [5] and STT-MRAM [1] memory chips, using available data from the literature at both device and array levels. We simulated array-level performance, based on provided cell parameters with NVMExplorer. The reported values consistently fell within our simulated range as depicted in Figure 3, validating that NVMExplorer's modeling capabilities effectively capture behaviors akin to those of fabricated memory arrays.

5. Conclusion

Our study advocates eNVMs as potential successors to conventional memory systems. Simulations reveal FeFET's superiority in area, power efficiency, and DNN application, while PCM, STT-MRAM, and RRAM show improved energy, latency, and reduced DNN inference power respectively.

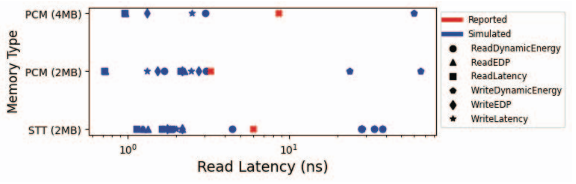

Figure 3: Simulated and Reported Results (Validation)

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