A 2.98 dB NF, 2.52 mW Low Noise Amplifier for a Brain Neuromodulation Implant

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***Abstract*—This study introduces a low noise amplifier (LNA) designed specifically for lower ultrawideband (UWB) applications. The presented LNA is based on a current-reuse common source (CS) architecture so as to achieve energy efficiency without sacrificing the noise performance. With 1.2V supply voltage, the proposed LNA consumes 2.52 mW power and achieves a 16.81 dB peak gain at 4.2 GHz frequency, with 1.28 GHz of 3-dB bandwidth. The average noise figure (NF) achieved is 2.98 dB across the 3-dB bandwidth. The design is realized using a standard 0.18 µm CMOS technology. The characteristic of the suggested amplifier makes it a proper candidate to be applied for implantable medical devices.**

***Keywords*—low noise amplifier, ultrawideband, current reuse, common source.**

I. Introduction

The Federal Communications Commission (FCC) designated the 3.1-10.6 GHz frequency spectrum for unlicensed ultra-wideband (UWB) use back in 2002 promoting commercial mass-market practices. UWB technology has sparked substantial interest in both educational and commercial enterprise because of its promise to provide high-speed short-range wireless data transmission with considerable energy efficiency.

UWB technology has demonstrated potential for various applications including Wireless Personal Area Networks (WPAN) [1][2] and Wireless Mesh Networks [3]. UWB communication uses the 3.1-10.6 GHz frequency range (lower band: 3.1-5 GHz; higher band: 6-10.6 GHz). The earliest advancement of the UWB technology takes place in the low frequency spectrum (3.1-5 GHz). When considering time to deployment, implementation cost, level of intricacy, and other factors, CMOS technology is a good choice for implementing a low band UWB system [4].

Devising an efficient low noise amplifier (LNA) is one of the challenging issues in the development of UWB circuits. In the literature, several LNA topologies have been proposed to address design issues such as broadband input and noise matching. Among these, the most popular techniques that have been implemented are common gate (CG) input matched LNA [5], cascode LNA [6], resistive feedback LNA [7], and distributed LNA [8]. However, the required wideband performance is often achieved by trading off the power consumption that doesn't meet the stringent requirement of low power biomedical applications such as a brain neuromodulation implant.

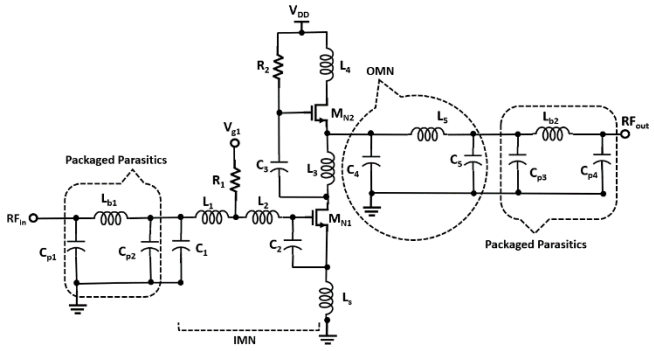

Fig. 1. Schematic of the proposed LNA

Multiple channels are exploited to capture and transfer data in high-speed biomedical fields including neural signal recording systems for brain-computer interface. The neural recording system uses a 128-channel to transfer the recorded brain signal with 90 Mbps speed while consuming only 6 mW of power [9]. Increasing the quantity of channels or the rate of sampling of the analog to digital converter (ADC) leads to a corresponding increase in the data rate. As such, the power requirement also increases. As a result, it is critical to decrease power consumption for such high data rate applications.

The originality of this work is to devise an power-efficient front-end amplifier exploiting 180 nm CMOS process which enables the receiver chain to be operated in the UWB frequency spectrum making it suitable for high data rate biomedical applications. The design architecture of the proposed LNA is discussed in section II. In section III, the simulation results are provided followed by a conclusion in section IV.

II. Proposed LNA Design

A. Circuit Description

The circuit schematic of the designed LNA is shown in Fig. 1. There are four stages, namely, input matching stage, common source first stage, current reuse stage and the output matching stage. The input matching circuit is composed of the capacitors C_1 and C_2 and the inductors L_1 and L_2. L_2 is in series resonance with the resultant capacitance coupled to the gate of active device M_{N1}. The shunt capacitor C_2 with the gate

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TABLE I
PARAMETERS OF THE ACTIVE DEVICE FOR THE LNA

Transistor	W/L (µm)	g_m/I_d
M_{N1}	150/0.18	1.68
M_{N2}	200/0.18	1.45

to source parasitic capacitance (C_{gs1}) and gate to drain parasitic capacitance (C_{gd1}) of the transistor M_{N1} forms the total capacitance that resonates with the series inductor L_2. Capacitor C_{p1}, C_{p2} and inductor L_{b1} consist of packaged parasitics [10].

The LNA is devised with the active device M_{N1} as common source (CS) structure in the first stage. Here the CS configuration is chosen due to its better gain and noise performance. Parameters for the active devices are listed in Table 1. Active device M_{N1} and M_{N2} are coupled as a cascade topology with the help of coupling capacitor C_3 such that with the identical bias current the overall transconductance is increased resulting in better noise performance with limited power consumption. The output of CS-current reuse stage taken across the parallel resonating circuit formed by inductor L_4 and the gate to drain miller capacitance of transistor M_{N2}. In the following stage, output matching circuit is devised exploiting inductor L_5 and the capacitor C_4 and C_5. Again, L_{b2}, C_{p3} and C_{p4} consist of parasitics at the output of the LNA. Table 2 presents the specific values of the components required for designing the LNA.

TABLE II
PARAMETER VALUES FOR THE DESIGNED LNA

Component	Value	Component	Value
L_1	18.5 n	C_4	65 p
L_2	2.96 n	C_5	124 f
L_3	9.3 n	C_{p1}, C_{p2}, C_{p3}, C_{p4}	250 f
L_4	4.47 n	R_1	5.02 k
L_{b1}, L_{b2}, L_{b3}, L_{b4}	1 n	R_2	0.52 k
C_1	10 f	V_{DD}	1.2 V
C_2	206.3 f	V_{g1}	0.6 V
C_3	1.2 p		

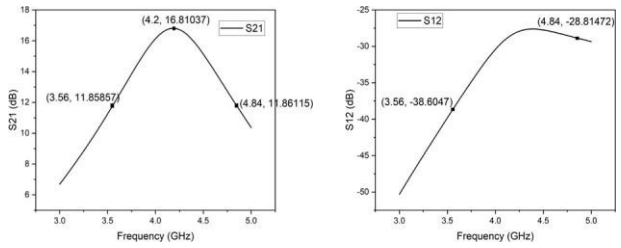
B. Input Matching Network (IMN)

In order to construct the input matching network, the input impedance of the active device, M_{N1} is evaluated at 3, 4 and 5 GHz as (30.59-68.28j), (32.64-27.32j) and (40.68+3.73j) ohm respectively. These impedances are matched with the impedance of packaged parasitics exploiting the "Impedance Matching Utility" of the Advanced Design System (ADS) platform by Keysight.

C. Output Matching Network (OMN)

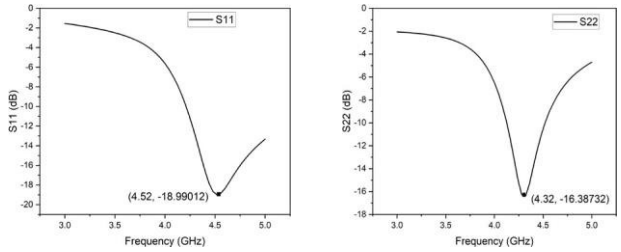
The output matching circuit is composed of L_5, C_6 and C_7. These elements are determined by initially calculating the output impedance at 3, 4 and 5 GHz as (260.15+148.77j), (252.03-256.37j) and (42.3-154.23j) ohm respectively and then these impedances are matched with the impedance of packaged parasitics in conjugate settings exploiting the Smith Chart.

III. RESULTS AND DISCUSSIONS



(a) (b)

Fig. 2. (a) S_{21} versus frequency; (b) S_{12} versus frequency of the proposed LNA



(a) (b)

Fig. 3. (a) S_{11} versus frequency; (b) S_{22} versus frequency of the proposed LNA

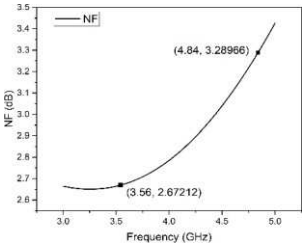


Fig. 4. Noise Figure versus frequency of the proposed LNA

The variation of S_{21} (forward gain) over the 3-5 GHz band is depicted in Fig. 2(a) where the highest gain of 16.81 dB is achieved at 4.2 GHz frequency and the 3-dB bandwidth is calculated to be 1.28 GHz. Reverse isolation, S_{12} as demonstrated in Fig. 2(b) is lower than -25 dB within the 3-dB bandwidth. Fig. 3(a) and Fig. 3(b) demonstrate the input (S_{11}) and output (S_{22}) reflection co-efficient of the proposed LNA, respectively. S_{11} of -18.99 dB is achieved at 4.52 GHz whereas S_{22} of -16.39 dB is obtained at 4.32 GHz. Noise figure (NF) is plotted in Fig. 4 where NF varies from 2.67 dB to 3.29 dB within the 3-dB bandwidth. Fig. 5 depicts the chip photo of the designed LNA from which the area footprint of the LNA is calculated to be 0.42 mm^2.

Table 3 compares the suggested LNA's performance to those of other recently reported works. It is evident from the comparison table that the power consumption of the designed LNA has been reduced by several orders while achieving comparable noise and gain performance within the ultrawideband spectrum.

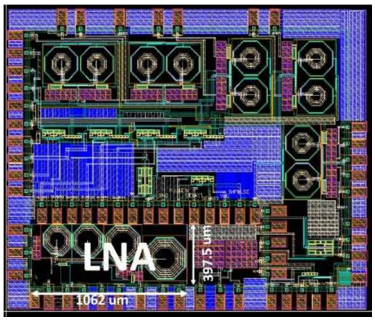


Fig. 5. Chip layout of the proposed UWB LNA

TABLE III
COMPARATIVE ANALYSIS WITH PREVIOUSLY REPORTED WORKS

	BW (GHz)	S_{21} (dB)	NF (dB)	V_{DD} (V)	P_{DC} (mW)	Tech. (µm)
This work	3-5	16.81	2.67-3.29	1.2	2.52	0.18
[11]	0.1-1.5	20	2.8-3.3	1.6	5.55	0.18
[12]	3.5-6	~13.5	~3.5	1.2	16	0.13
[13]	3-5	14.5	2.2	1.2	8.2	0.90

IV. CONCLUSION

Minimizing overall power consumption is crucial for high-speed purposes, such as a neural signal recording system, that utilizes multiple channels for data collection and transmission. When compared to existing state-of-the-art research, this study provides a low noise amplifier with optimized energy consumption while maintaining high speed transmission, making it extremely appropriate for low power biomedical sensor applications. Furthermore, by exploiting the UWB frequency band, the designed LNA is able to communicate data captured from diverse cerebral regions.

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