

Finger-Regulated Simultaneous Noise and Input Matching (FRSNIM) Guided CMOS LNA

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Abstract—The multi-finger architecture has been widely explored in submicron CMOS circuits because it caters to improved device performance compared to its mono-finger counterparts. However, setting appropriate finger variables, including finger width and number of fingers, to boost the circuit's performance is a cumbersome task. The objective of this work is to develop a finger-regulated simultaneous noise and input matching (FRSNIM) methodology for microwave front-ends. It is driven by the concept of impedance engineering of source referred noise impedances (Z_{opt}) to realize a theoretical optimization exploiting Keysight's Advanced Design System (ADS) platform and the 180 nm standard CMOS process. As part of the proposed FRSNIM approach, a protocol for setting up optimum bias points is outlined through the assessment of radio frequency benchmarks. The proposed FRSNIM mechanism takes into account the parasitics associated with the bond pad and bond wire to model the influence of the packaged parasitic on scattering port parameters. Exploiting the proposed FRSNIM scheme, a low noise amplifier (LNA) is devised, which furnishes a 16.7 dB forward gain and a 1.4 dB noise figure at 2.4 GHz while consuming only 6.6 mW of power from a 1.8 V supply voltage. The input-referred third-order intercept point (IIP3), defining the linearity of the LNA, is -7dBm . It occupies an area of $470 \times 337 \mu\text{m}^2$.

Index Terms—Finger number, aspect ratio, packaged parasitic, Smith Chart, contour plot, impedance matching, minimum noise figure.

I. INTRODUCTION

As the first active block, the low noise amplifier (LNA) has a significant impact on the overall performance of the receiver chain. The main objective of LNA is to amplify a weak radio frequency (RF) signal while minimizing the inclusion of additional noise as much as possible [1]. LNA attributes including impedance matching, noise performance, forward gain, power consumption and linearity are rigorously balanced in a highly efficient LNA [2]. The trade-off between noise figure (NF) and input matching imposes a major challenge on the design of an LNA. Various input matching networks have been proposed in prior works for narrowband LNA [3]. Ratnaparkhi et al. designed a parallel capacitor-inductor network to cancel the imaginary part of the input impedance of the source degenerated differential LNA [4]. Nguyen et al. proposed an external capacitor added in between the gate and the source of the input transistor to reduce the imaginary part of the input impedance, hence making the matching operation more straightforward [5]. Ghanbari et al. suggested a transmission line-based matching network which requires a substantial die area [6]. Padhye et al. proposed a large series

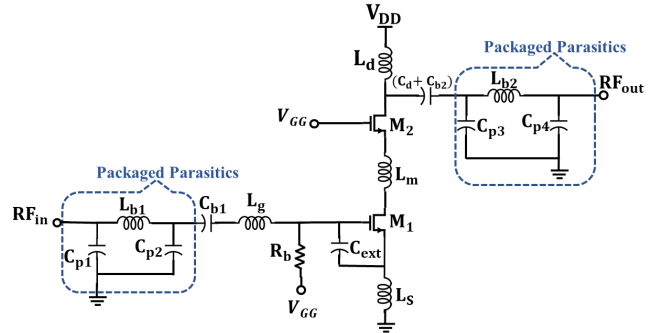


Fig. 1. Schematic of the FRSNIM-based 2.4 GHz cascode LNA.

inductor employed at the gate of the input transistor to cancel out the imaginary part of the input impedance [7]. Arshad et al. recommended transformer feedback for input matching where the transformer is connected to the input, therefore its noise is directly added to the antenna noise source and hence the NF gets degraded [8]. As a result, input matching has often been the reason for high NF, and it has negatively impacted other RF benchmarks. However, the most important aspect of LNA design is to get the lowest NF possible.

Recent advancements in CMOS technology have utilized multi-finger controlled structures to take advantage of superior layout fitting, reduced gate resistance, and enhanced reflection loss [9]–[12]. The employment of multi-finger structures can significantly downscale the diffusion area and perimeter, which results in improved RF performances. However, arbitrarily choosing finger variables will not cater to the desired specifications. Our previous work explored the impact of multi-finger technology on wideband matching [9], however; a protocol still needed to be devised to manage finger variables to establish the required benchmarks. The novelty of this work is to propose a design approach to accomplish a better trade-off between impedance matching and noise performance by modeling the influence of the finger variables on the impedance settlement of submicron amplifiers. The proposed finger-regulated simultaneous noise and input matching (FRSNIM) technique is validated by devising a CMOS LNA operating in the 2.4 GHz band through the assessment of source-referred noise impedances (Z_{opt}) modulation. As part of the impedance matching technique, a protocol is proposed to regulate finger variables while satisfying the requirements of multi-finger setups are of great interest to better optimize

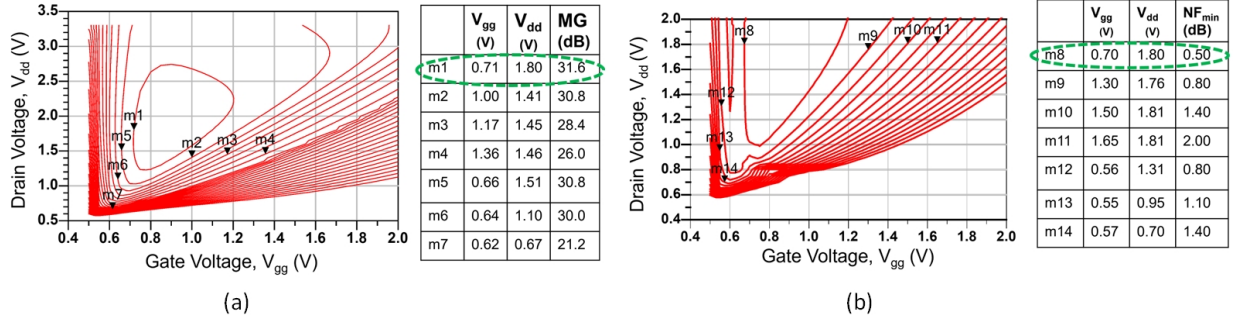


Fig. 2. Contours of (a) MG and (b) NF_{min} as a function of V_{gg} and V_{dd} .

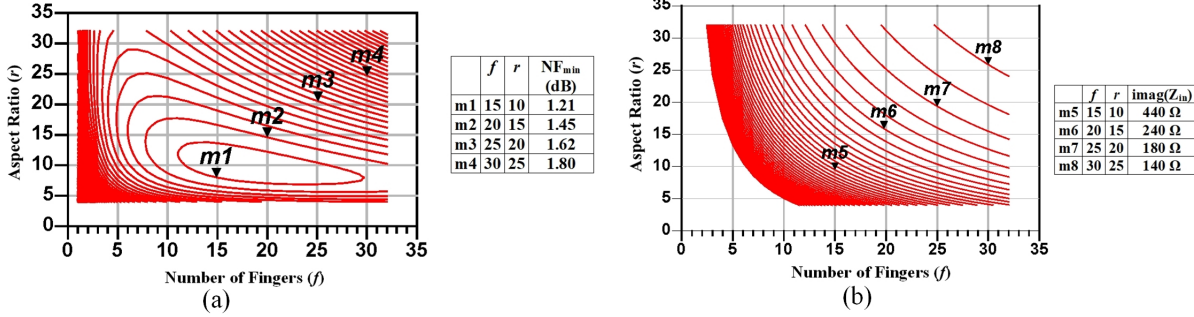


Fig. 3. Contour plots of (a) NF_{min} and (b) imaginary part of input impedance ($imag(Z_{in})$) as a function of number of fingers (f) and aspect ratio (r).

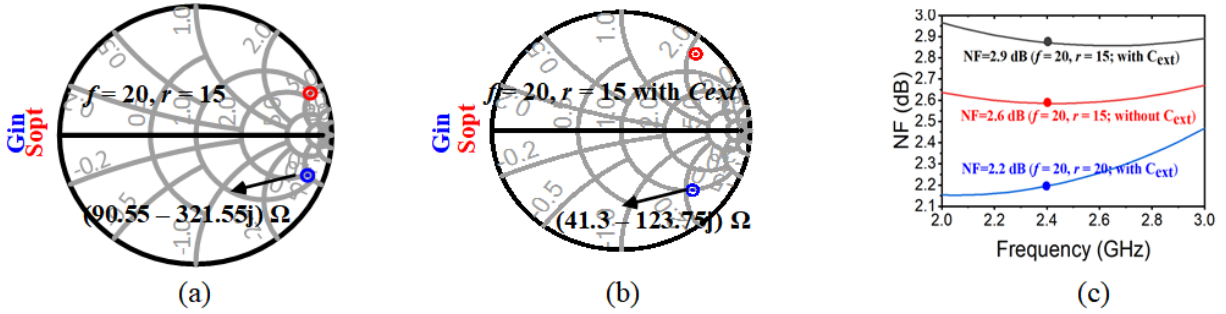


Fig. 4. Influence of finger variables (f and r) (a) without C_{ext} , (b) with C_{ext} on input impedance and (c) with and without C_{ext} on noise figure (NF).

the amplifier characteristics. Section II describes the proposed finger regulation approach in order to achieve the state-of-the-art performance metrics for the designed LNA which is then followed by a conclusion in section III.

II. FRSNIM-DRIVEN CASCODE LNA DESIGN

The architecture of the proposed FRSNIM-based CMOS LNA designed in 180 nm CMOS technology is shown in Fig. 1. The detailed design approach is explained below.

A. Assessment of Bias Points

Keysight's Advanced Design System (ADS) platform is exploited for mapping multidimensional contours to determine the optimum bias points. Simulated contours for maximum gain (MG) as a function of the drain (V_{dd}) and gate (V_{gg}) voltages are plotted in Fig. 2(a). MG indicates the theoretical highest power gain that can be achievable from a device at specific bias points and frequency. Hence, after adding the matching networks, we can't attain a power gain that is greater

than MG. Each contour furnishes a certain value of MG for different combinations of V_{gg} and V_{dd} . In this case, the highest MG of 31.6 dB is achieved through the contour marked by m_1 . It can be seen that as we go from m_7 to m_1 (along the vertical axis), V_{dd} increases, which results in an increment of MG. This is because with the increment of V_{dd} , drain current (I_d) increases, which increases the transconductance (g_m) of the device. If g_m is increased, then the voltage gain (A_v) is also increased correspondingly. On the other hand, if we go from m_1 to m_4 (along the horizontal axis), V_{gg} gets increased, which results in a decrease of MG from 31.6 dB to 26.0 dB. Similarly, as shown in Fig. 2(b), minimum noise figure (NF_{min}) contours are devised as a function of V_{gg} and V_{dd} . NF_{min} is the absolute lowest noise figure that can be achievable from a device. Hence, we can't achieve a noise figure that is lower than the NF_{min} of a device after adding matching circuitry. In this case, the best NF_{min} is tailored to the contour marked by m_8 , as demonstrated in Fig. 2(b),

where it is obvious that NF_{min} gets worsened as we increase the V_{gg} . This is because as V_{gg} increases, gate current is also increased, resulting in an increase of noise current. However, if V_{dd} gets increased, NF_{min} is also improved as g_m of the device increases with the increment of V_{dd} . To this end, the optimum bias points are set as V_{dd} and V_{gg} to 1.8V and 0.7V (marked by the dotted green line), respectively, where we have the optimum noise and gain performances.

B. Impedance Settlement with FRSNIM

The proposed FRSNIM protocol is developed to achieve an impedance settlement through the sizing of the transistors. At first, several terms including number of fingers (f), multipliers (m), and aspect ratio (r), are needed to be defined. m means the number of parallel devices. If we increase m , I_d gets increased. f is the number of polygate fingers exploited in the layout management. By extending the total f , both the source and drain experience a reduction in their area and perimeter. As a consequence, the multi-finger structure concept will substantially decrease parasitic capacitances, resulting in an improvement in noise performance. If the transistor has just one f and one m , the total width (w) becomes $r \times L$ (transistor's aspect ratio, $r = w/L$, where L is the channel length). Similarly, the total width becomes $2 \times r \times L$ for a transistor having f of 2 and m of 1. By extension, for a split device having f of 2 and m of 2, the resultant width becomes $2 \times 2 \times r \times L$. As such, the overall width of the multi-finger transistor, W_{total} , should be:

$$W_{total} = L \times r \times f \times m \quad (1)$$

Fig. 3 depicts the selection of optimal f and r within the range allowed by the process technology for achieving nearly ideal impedance matching by determining the optimum aspect ratio of the transistor. NF_{min} of the transistor is plotted in Fig. 3(a) for the various combinations of f and r values. The contour marked by $m1$ shows possible combinations of f and r for the lowest NF_{min} of 1.21 dB. Next, f and r are swept to assess the imaginary part of the input impedance ($imagZ_{in}$), as shown in Fig. 3(b). At $m5$ ($f = 15$, $r = 10$), the $imagZ_{in}$ is 440 Ω , a large off-chip inductor is thus needed to be placed in order to cancel the imaginary impedance. Various approaches have been proposed in prior works to reduce the $imagZ_{in}$. One of the approaches is to increase the size of the transistor (e.g., increase f and r), which can also be observed in Fig. 3(b). From $m5$ to $m8$, $imagZ_{in}$ is reduced from 440 Ω to 140 Ω as (f, r) is increased from (15, 10) to (30, 25).

However, for the $(f, r) = (30, 25)$, the NF_{min} increases to 1.80 dB as denoted by $m4$ in Fig. 3(a). Also, with this f and r combination, the size of the device is increased significantly, resulting in a five-fold increase in power consumption. Hence, optimum values for f and r are needed to be chosen so that NF_{min} is not greater than 1.5 dB while $imagZ_{in}$ is the lowest. Next, to further reduce the $imagZ_{in}$, $(f, r) = (20, 15)$ is chosen where NF_{min} is 1.45 dB and the $imagZ_{in}$ is 240 Ω .

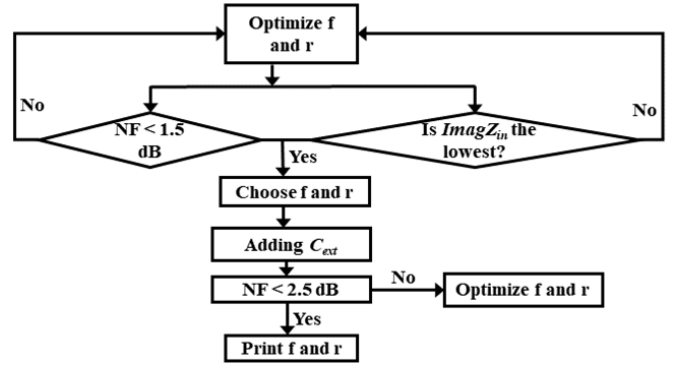


Fig. 5. Proposed FRSNIM Scheme.

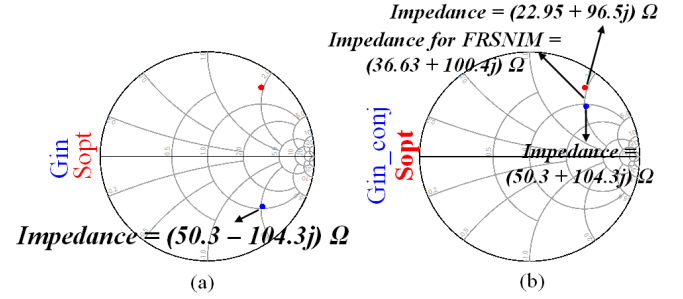


Fig. 6. Plotting of (a) G_{in} and S_{opt} and (b) G_{in_conj} and S_{opt} at the final setting of f and r for impedance matching.

Now, a trade-off between power gain and NF is furnished in Fig. 4 for this f and r combination by devising an optimum source reflection coefficient for minimum noise figure (S_{opt}) and an optimum source reflection coefficient for maximum forward gain (G_{in}) [10]. Here, the imaginary part of G_{in} is 321.55j Ω , which is indeed a high value because of the low capacitance at the input. To further explain this point, the equation of input impedance of a source degenerated common source LNA is shown below [10].

$$Z_{in} = s(L_g + L_s) + 1/(sC_{gs}) + (g_m L_s)/C_{gs} \quad (2)$$

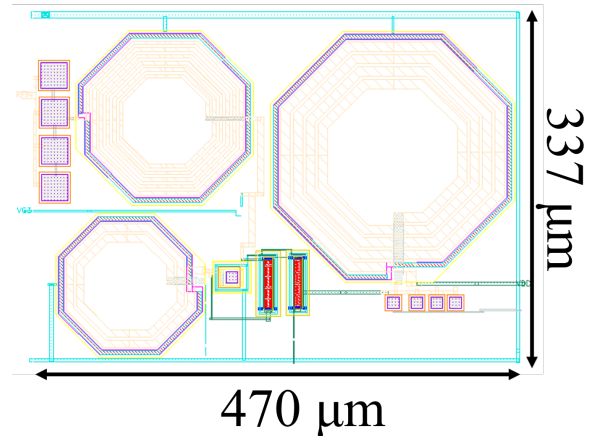


Fig. 7. Layout of the proposed FRSNIM-driven LNA.

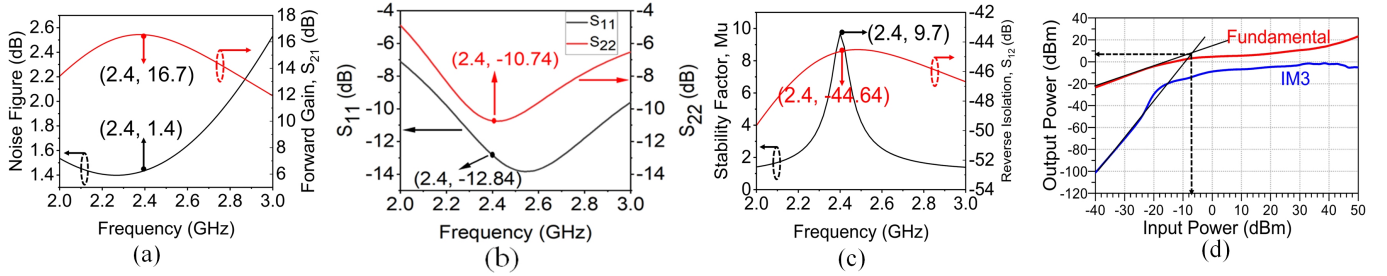


Fig. 8. Simulated (a) forward gain (S_{21}) and NF, (b) input reflection co-efficient (S_{11}) and output reflection co-efficient (S_{22}), (c) stability factor (μ) and reverse isolation (S_{12}), (d) the third-order intercept point (IIP3) of the proposed FRSNIM-based LNA.

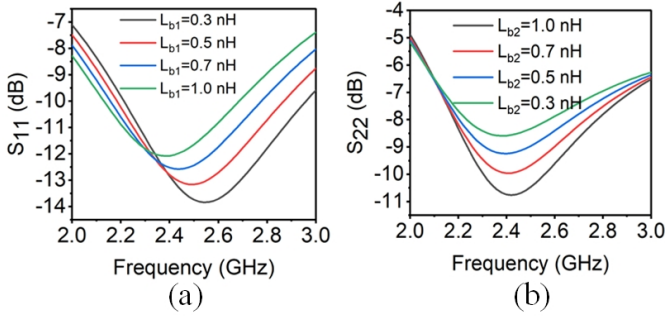


Fig. 9. Impact of packaged parasitics on (a) input and (b) output matching of the proposed FRSNIM-inspired LNA.

Where, L_g and L_s are gate and source inductor, respectively, C_{gs} is the gate-to-source capacitance of the transistor M_1 . From equation (2), it is evident that if input capacitance, C_{gs} , is very low, then the imaginary part of $Z_{in}(=1/sC_{gs})$ will be very high. Hence, an external capacitor, C_{ext} , is added between the gate and source of the M_1 to increase input capacitance, resulting in a lower $imagZ_{in}(=1/s(C_{gs}+C_{ext}))$. This approach of adding an external capacitor does not increase the power consumption, as in the case of increasing the size of the transistor. With $C_{ext} = 3$ pF and $(f, r) = (20, 15)$, the imaginary part of G_{in} is reduced to $123.75j \Omega$ as shown in Fig. 4(b).

However, adding C_{ext} increases the NF , as indicated by the blue curve in Fig. 4(c). To resolve this issue, the size of the transistor needs to be increased a little bit (increasing the transistor size results in an increase of I_d , boosting the g_m of the device, which eventually improves the NF). Based on all the steps described above, the proposed FRSNIM technique is summarized in Fig. 5. Following the proposed design approach, when $(f, r) = (20, 20)$, with C_{ext} , the NF shows the best performance of 2.2 dB, as shown in Fig. 4(c). Moreover, for this f and r combination, along with the addition of C_{ext} , the real part of G_{in} is 50.3Ω , and the imaginary part is further reduced to $104.3j \Omega$, as shown in Fig. 6(a), enabling the option to design a simpler matching network. Hence, in our proposed design, both f and r are set to be 20 for M_1 . In a similar fashion, the finger variables are optimized for M_2 .

C. Design of Input Matching Network (IMN)

For designing the IMN, $(G_{in_conj} = \text{conj}(G_{in}))$ and S_{opt} are plotted on Smith Chart as shown in Fig. 6(b). S_{opt} allows

TABLE I
COMPONENT PARTICULARS FOR THE PROPOSED LNA

Components	Values
Supply (V)	$V_{dd} = 1.8, V_{gg} = 0.7$
Resistors (Ω)	$R_b = 10k$
Capacitors (F)	$C_{p1} = C_{p2} = C_{p3} = C_{p4} = 250f$, $C_{ext} = 0.3p$, $C_d = 0.4p$, $C_{b2} = 4p$
Inductors (nH)	$L_{b1} = 1, L_g = 7, L_m = 2$, $L_s = 0.8, L_d = 8, L_{b2} = 1$
Transistors	
W/L ($\mu m/\mu m$)	$M_1 = 72/0.18, M_2 = 54/0.18$

TABLE II
CORNER ANALYSIS FOR THE PROPOSED LNA

Components	TT Corner	FF Corner	SS Corner
S_{11} (dB)	-12.84	-10.23	-16
S_{22} (dB)	-10.74	-10.38	-12
S_{21} (dB)	10.16	13.72	8.69
NF (dB)	2.82	2.13	3.76
Power (mW)	6.6	7.4	4.8
IIP3 (dBm)	-7	-8	-5.5

TABLE III
COMPARISON WITH OTHER WORKS

Parameters	[13]	[14]	[15]	This work
Process (nm)	180	GaAs	65	180
Freq. (GHz)	2.4	2.4	2.4	2.4
S_{11} (dB)	-13.8	-10.02	-19.49	-12.84
S_{22} (dB)	-12.5	-19.07	—	-10.74
S_{21} (dB)	14.6	19.85	10.6	16.7
S_{12} (dB)	-34.2	—	—	-44.64
NF (dB)	2.89	1.01	3.15	1.4
μ	4.3	—	—	9.7
IIP3 (dBm)	—	—	-8.75	-7
Power (mW)	9.15	20	11	6.6
FoM1	0.55	0.72	-2.38	3.74
FoM2	—	—	-11.14	-3.25

the minimum noise figure but not good power matching [11]. On the other hand, G_{in_conj} offers the best power matching, disregarding the minimum noise figure. Hence, the impedance $(36.63 + 100.4j) \Omega$, which is in between the two points, is chosen for the implementation of FRSNIM. This impedance point is matched to an impedance network consisting of bond pads and bond-wires in order to take into account the impact of packaged parasitics [9].

D. Complete LNA Simulation

Fig. 7 depicts the layout of the proposed LNA. The total area requirement of the LNA is $470 \times 337 \mu m^2$. Table I tabulates the component values for the proposed LNA. The quality factor (Q) of the source (L_s), gate (L_g), and drain (L_d) inductor are 5, 8, and 6, respectively. Fig. 8(a), 8(b), 8(c), and 8(d) demonstrate the post-layout simulated noise figure and forward gain (S_{21}), input and output reflection coefficients, stability factor and reverse isolation, and $IIP3$ of the proposed LNA, respectively. The LNA has a power gain of 16.7 dB and a noise figure of 1.4 dB at 2.4 GHz. It achieves good input and output matching. At 2.4 GHz, the values of S_{11} and S_{22} are -10.74 dB and -12.84 dB, respectively. The stability factor, Mu is 9.7 at 2.4 GHz, which means the LNA is unconditionally stable. The reverse isolation is -44.64 dB at 2.4 GHz. The third-order intercept point ($IIP3$) is -7 dBm as demonstrated in Fig. 8(d). The LNA draws a current of 3.6 mA from a supply voltage of 1.8V. Hence, the total power requirement of the LNA is only 6.6 mW. The LNA is simulated at different process corners and the results are demonstrated in Table II. For different values of bond wires, Fig. 9(a) and 9(b) demonstrate the influence of packaged parasitics on input and output matching, respectively. As the value of the input bond-wire (L_{b1}) increases to 1 nH, the resonant frequency shifts towards 2.4 GHz, whereas the resonant frequency is almost fixed to 2.4 GHz for different values of the output bond-wire (L_{b2}).

Table III compares the performance of the proposed LNA with other recently reported works. All the results presented in Table III are based on simulation. The proposed FRSNIM-based LNA dissipates the lowest power, yet it exhibits a comparable NF and gain. For example, although the design proposed in [14] consumes almost three times more power than our proposed LNA, our gain and noise performance are comparable. Thus, the suggested LNA fits the requirements of portable low-power high-performance receivers. Two figures of merits ($FoMs$) as described below are exploited for making a fair comparison among all the architectures. $FoM1$ is realized through frequency, power gain, noise figure, and dissipated power (P_{DC}), whereas $FoM2$ considers $IIP3$ as well. The proposed LNA is capable of attaining the best $FoMs$.

$$FoM1 = 10 \log_{10} \left(\frac{Freq_{GHz} \cdot Gain_{mag}}{(NF - 1)_{mag} \cdot P_{DC(mW)}} \right) \quad (3)$$

$$FoM2 = 10 \log_{10} \left(\frac{Freq_{GHz} \cdot Gain_{mag}}{(NF - 1)_{mag} \cdot P_{DC(mW)}} \cdot IIP3_{mw} \right) \quad (4)$$

III. CONCLUSION

A finger-regulated input impedance optimization-based design approach is proposed in this work for impedance settlement faced by submicron amplifier circuits to compensate for noise and gain impedance discrepancies with better power management which makes the designed LNA suitable for low power and short-range communication.

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REFERENCES

- [1] S. Reza and A. Roy, "Stability analysis of multifinger CMOS RF amplifiers," in *2019 2nd International Conference on Innovation in Engineering and Technology (ICIET)*, 2019, pp. 1–6.
- [2] S. Reza and I. Mahbub, "A 2.98 dB NF, 2.52 mW low noise amplifier for a brain neuromodulation implant," in *2024 IEEE 17th Dallas Circuits and Systems Conference (DCAS)*, 2024, pp. 1–3.
- [3] S. Kim and K. Kwon, "Broadband balun-LNA employing local feedback gm-boosting technique and balanced loads for low-power low-voltage applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 4631–4640, 2020.
- [4] V. V. Ratnaparkhi and K. N. Deshmukh, "Design and performance analysis of microwave amplifier using S-parameters," in *2016 International Conference on Global Trends in Signal Processing, Information Computing and Communication (ICGTSPICCC)*, 2016, pp. 631–633.
- [5] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 5, pp. 1433–1442, 2004.
- [6] M. M. Ghanbari, D. K. Piech, K. Shen, S. F. Alamouti, C. Yalcin, B. C. Johnson, J. M. Carmenta, M. M. Maharbiz, and R. Muller, "17.5 A $0.8mm^3$ ultrasonic implantable wireless neural recording system with linear AM backscattering," in *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2019, pp. 284–286.
- [7] Y.-J. Hong, S.-F. Wang, P.-T. Chen, Y.-S. Hwang, and J.-J. Chen, "A concurrent dual-band 2.4/5.2 GHz low-noise amplifier using gain enhanced techniques," in *2015 Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC)*, 2015, pp. 231–234.
- [8] S. Arshad, R. Ramzan, F. Zafar, and Q. ul Wahab, "Highly linear inductively degenerated 0.13 μm CMOS LNA using FDC technique," in *2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2014, pp. 225–228.
- [9] S. Reza and A. Roy, "3–5 GHz multifinger CMOS LNA using a simultaneous noise and impedance matching technique by a significant reduction of broadband impedance variation of metal–oxide–semiconductor field effect transistor," *IET Circuits, Devices and Systems*, vol. 14, no. 07, pp. 956–965, 2020.
- [10] B. Razavi, *RF Microelectronics*. 1st ed. New Jersey, NJ, USA: Prentice Hall, Inc., 1998.
- [11] S. Reza, *Finger-regulated simultaneous noise-and-input-matching technique with wideband impedance settlement for CMOS low noise amplifiers*. Department of Electrical and Electronic Engineering (EEE), BUET, 2021.
- [12] S. Reza and I. Mahbub, "Modeling and optimization of peaking inductors for X-band circulator in standard $0.18 \mu m$ CMOS," in *2024 IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2024.
- [13] D. Jahnavi *et al.*, "Design and analysis of 2.4 GHz low-noise, high-gain $0.18 \mu m$ CMOS cascode low-noise amplifier for IRNSS applications," *IETE Journal of Research*, vol. 68, no. 6, pp. 3960–3970, 2022.
- [14] I. E. Yilmaz *et al.*, "Low noise amplifier (LNA) design suitable for 2.4 GHz radar applications," *Journal of Millimeterwave Communication, Optimization and Modelling*, vol. 1, no. 1, pp. 17–20, 2021.
- [15] M. G. L. Kumar, S. S. Regulagadda, J. K. Das, and A. Dutta, "Design of current reuse based differential merged LNA-mixer (DMLNAM) and two-stage dual band LNA with two gain modes in 65nm technology," in *2015 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, 2015, pp. 98–103.