A 2-Bit Differential Phase Shifter in 180-nm CMOS with 1.85 dB Insertion Loss for V-band Phased Array Antenna Application

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Abstract-This paper introduces a novel phase shifter **(PS)** utilizing a standard 180-nm CMOS process, distinguished by its differential 2-bit switch-type design for V -band phased array **(PA)** application. Due to its switch-type design, this PS exhibits the advantageous characteristic of using no power. The proposed PS utilizes a differential PS unit that incorporates both high-pass and low-pass states to significantly reduce the inductor values achieving a compact dimension of 700 x 750 μm^2. The floating body terminal transistor-based 2-bit PS has been introduced resulting in the lowest average insertion loss (IL) of < 1.85 dB for the frequency range 57.18-61.92 GHz.

Index Terms-Phase shifter **(PS),** V -band, phased array antenna, 180nm CMOS, switch-type PS, differential input.

I. INTRODUCTION

Phase shifters with excellent trade-offs between low IL and precise phase resolution are essential for implementing PAs for V-band applications operating at 60 GHz [l]. Phased-array antennas designed for the V-band frequency to facilitate the 5G communication, typically leverages integration of CMOS or GaN technology within a unified microchip [2], [3]. In a system utilizing a PA, PSs are employed to change the phase of the signal in each channel, allowing for the formation of a beam directed toward a preferred direction. Practically, PSs introduce IL and phaseerrors when transitioning within states. Thus in phased-arrays, PSs are required to achieve a balanced trade-off between the low IL and the precise phase resolution.

Two categories of PSs are commonly used in the typical mm-wave PAs to achieve precise phase adjustments over an extent of 0° to 360° with an IL of approximately 12-15 dB. These PSs are known as the switched-type (STPS) and reflective-type (RTPS) [4], [5]. The RTPS has the ability to produce a continuous phase shift based on analog tuning voltages. These tuning voltages are typically sourced from digital-to-analog converters (DACs) and serve the purpose of controlling digitally. The phase resolution of an RTPS is significantly influenced by the resolution and precision of the DACs controlling the tuning voltages [6], [7]. This dependency arises from the non-linear relationship that is observed between the tuning voltages and the resulting phase shift. On the other hand, STPSs possess several advantages, including no direct current (de) power consumption, digital regulation, and bidirectional capability [8], [9]. The fundamental mechanism by which STPSs accomplish the phase shift function involves a cyclical transition between two distinct operational states: the phase shift state and the bypass state. Where the achieved phase shift is zero for the designed bypass state. The process of achieving phase shift at the central frequency involves inductor-capacitorcomponents, commonly in the configuration of a high-pass (HP) or low-pass (LP) filter circuit To minimize phase error, the researchers have employed PS units exhibiting a significant phase noise with both LP (phase delay) and HP (phase advance) states. These specialized networks are commonly denoted as HP-LP structures [11].

In this manuscript, a novel compact 2-bit differential HP-LP PS unit is proposed which achieves the lowest IL over a wide bandwidth, as far as known by the author, the proposed work achieves *a)* Enhancement of bandwidth to achieve 8.1% fractional bandwidth (4.8 GHz) by utilizing the capacitance of the switches into phase shifting elements when the switches are in OFF state, *b)* Attain a low IL of< 1.85 dB over achieved bandwidth by implementing floating body terminal based transistor in the design, and c) Significant reduction in inductor value, to reduce the overall area by incorporating LP/HP phase shifting topology for 60° and 45° phase shift by achieving ±30° and ±22.5° shift for each state. The presented 2-bit PS unit is designed to create the phased-array antenna system with our previously demonstrated antennas [12], [13]. This paper is arranged as follows: first, the designed architecture is addressed in Section II. Then, the simulation results for the **HP-LP PS** units are analyzed in Section ill, and the conclusion is presented in Section IV.

II. PROPOSED DESIGN ARCHITECTURE

Fig. 1 presents the schematic of the PS in both the high-pass and low-pass states. The HP and LP phase-shifting units alternate between their HP and LP states by adjusting the control voltage to high (2V) and low (OV) levels accordingly to accomplish the desired phase shift. Thus, a total phase shift of </> can be achieved using HP and LP state providing

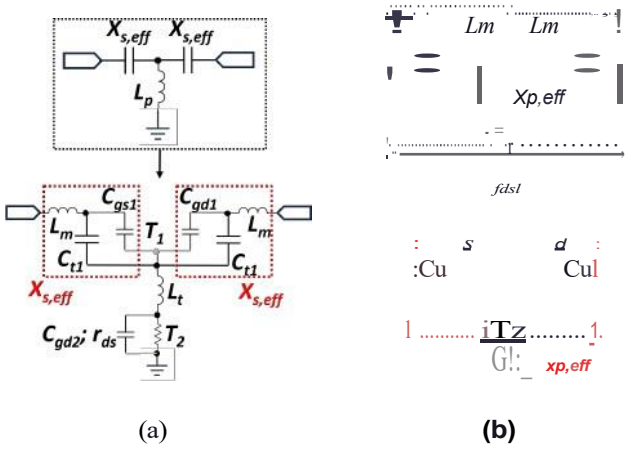
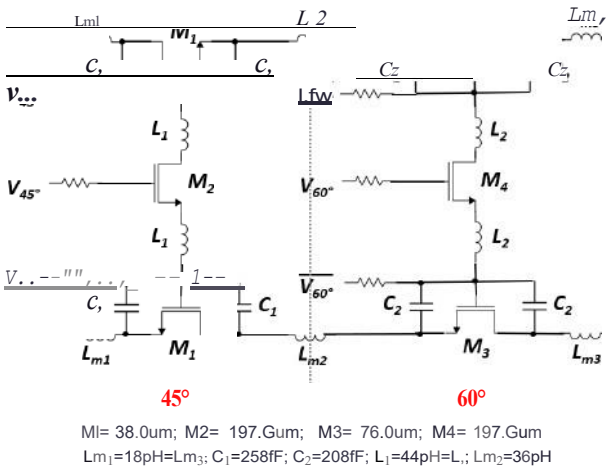


Fig. I. PS Half Circuits (a) HP state, and (b) LP state.



Ml= 38.0um; M2= 197.Gum; M3= 76.0um; M4= 197.Gum
Lm_1=18pH=Lm_3; C_1=258fF; C_2=208fF; L_1=44pH=L_1; Lm_2=36pH

Fig. 2. Equivalent circuit for the proposed 2-bit STPS

an insertion phase of positive and negative ¢/2, respectively. The HP and LP state for proposed PS is presented in Fig. 1, compared to conventional PS [14], the gate connection for T1 is connected through the drain of T_2, such that when T1 is OFF, the parasitic capacitance C_{gs1} and C_{ga1} will be considered to be connected in parallel to Cn forming $X_{s,eff}$.

This changed gate connection to the T_1, made the resulting parasitic capacitance to be accounted for the calculation of effective reactance of the *LC - netwark* while the switch is OFF for HP and LP state, improving the bandwidth of the PS. For LP state, T_1 is operating for which the corresponding tum-on resistance $(r_{asi/2})$, and for HP state T_2 is operating, its corresponding (r_{ds2}) is considered as a short circuit Thus, Fig. l(a) considering for the HP state, forms a T-type network, the series combination of equivalent reactance $X_{s,ef\ I}$ (combination of L_m and C_t) and a parallel grounded inductor L_t. To achieve a ¢/2 phase shift and thus achieve an ideal alignment in the HP state, the values of L_t and $X_{s,ef\ I}$ can be determined using the following formulas [14]:

$$L_t = \frac{Z_o}{w_o \sin\langle/J/21} \quad \text{(I)}$$

$$X_{s,eff} = \frac{1}{w_o Z_o \tan l¢/41} \quad (2)$$

Where W_o and Z_o are known as angular frequency and characteristic impedance, respectively.

Now, in the LP state, the series combination of equivalent reactance $X_{p,eff}$ (L_t, $2C_t$ and C_{9a2} connected in series) and L_m, forms a T-type network. Thus, to achieve a ¢/2 of phase shift and optimal alignment in the phase delay state, one can determine the values of L_m and $X_{p,eff}$ through the following calculations:

$$L_m = \frac{Z_o \tan l¢/41}{W_o} \quad (3)$$

$$X_{p,eff} = \frac{\sin l\langle/J/21}{W_{oo}} \quad (4)$$

From (1), (2), (3), and (4), C_t and C_{9a2} can be obtained as follows:

$$C_t = \frac{1}{2 w_o Z_o \tan l\langle/J/41} \quad (5)$$

$$C_{gd2} = \frac{\tan l¢/41}{W_o Z_o} \quad (6)$$

The above-discussed formulas (1)-(6) are used to obtain design parameters and the proposed design is optimized further in the Cadence Virtuoso **(R)** simulation platform. Furthermore, to improve the IL of the overall PS, the floating-body triple-well switch is used compared to the grounded body terminal transistor [13]. However, the width of the switch is optimized to achieve minimal loss and effective isolation within the floating body terminal transistor-based switch. Increasing the transistor width reduces loss and isolation, underscoring the importance of optimizing the transistor width. Irrespective of conventional PS [14], to achieve a wide range of phase shift, the proposed PS switches between HP and LP states achieving ±¢/2 for a low value of inductor occupying a smaller area at each state, resulting in a significant reduction of the overall area of the PS.

Ill. SIMULATION RESULTS

This work proposes an HP-LP PS unit with 45° and 60° phase shift, utilizing a 180-nm CMOS process and operating at a central frequency of 60 GHz. For the phase shift of 45° and 60°, the magnitude of the IP (¢/2) is considered to be equal to 22.5° and 30°, respectively. To achieve a low IL over a wide frequency range, the size of the transistors is optimized, where the complete schematic of the proposed **PS** is shown in Fig. 2.

The proposed PS demonstrates high-pass (HP) and low-pass (LP) frequency characteristics while in their respective HP and LP states. The PS units for 45° and 60° are operating for the frequency range 58-61.92 GHz and 57.18-61.23 GHz, respectively have return losses >25 dB as shown in Fig. 3 achieving an approximate wide bandwidth of 4.8 GHz. Whereas, Fig. 4, presents the magnitude of the IL and phases for the 45° and 60° PS stage. For the 45° phase shift unit, the

TABLE I
COMPARISON TABLE

Ref.	Process	Frequency (GHz)	Topology	No. of Bits	Insertion Loss (dB)	Return Loss
[10]	180-nm CMOS	26-30	STPS	5	15	>5.7
111J	65-nm CMOS	35-41.9	STPS	5	7.56	>7.8
[16]	65-nm CMOS	37-40	STPS	5	9.3	>10.4
[17]	65-nm CMOS	29	RTPS	-	9.5	18
10is Work	180-nm CMOS	57.18-61.92	STPS	2	<1.85	>26

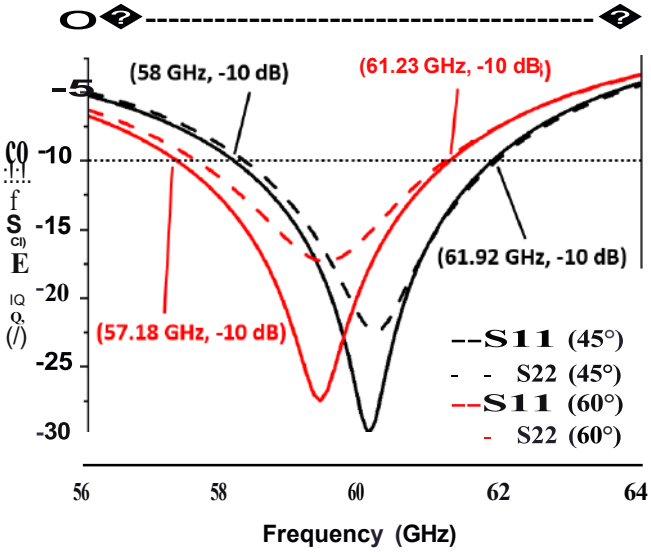


Fig. 3. Return losses for 45° and 60° phase shift unit.

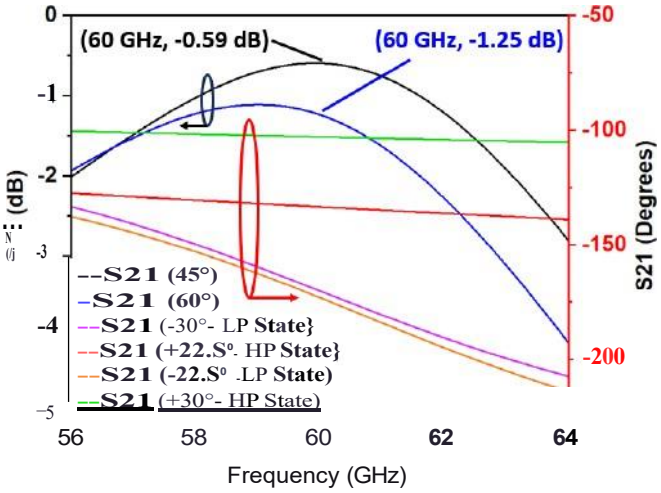


Fig. 4. Insertion losses and insertion phase for 45° and 60° phase shift unit.

achieved IL at 60 GHz is 0.59 dB, whereas for the 60° phase shift unit it is 1.25 dB at 60 GHz. Fig. 5 presents a layout of the proposed PS with a compact size of 700 x 750 μm², including the chip pads.

IV. CONCLUSION

This work presents a 2-bit differential PS designed using a 180-nm CMOS process for V-band PA antenna. The proposed novel design allows the PS to maintain the lowest average IL

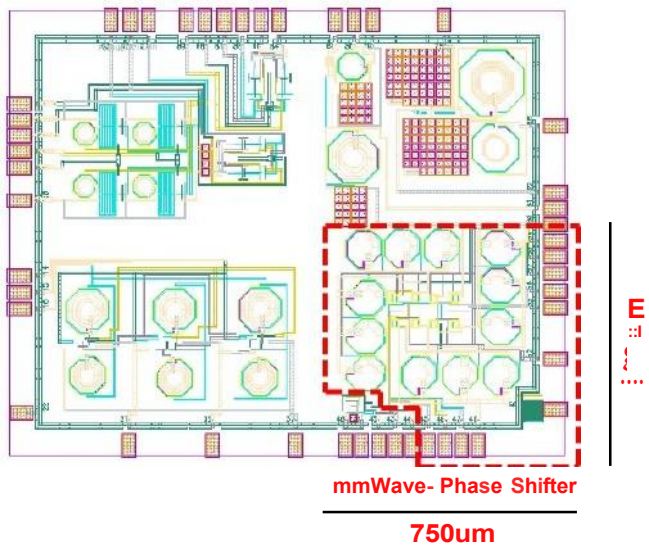


Fig. 5. Layout of proposed 2-bit STPS

of <1.85 dB for a wideband frequency range of 57.18-61.92 GHz for a compact size of 700 x 750 μm². These results indicate that the developed PS exhibits promise for utilization in V-band PA systems.

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REFERENCES

(1) S. Kutty and D. Sen, "Beamforming for Millimeter Wave Communications: An Inclusive Survey," in IEEE Communications Surveys Tutorials, vol. 18, no. 2, pp. 949-973, Secondquarter 2016, doi: 10.1109/COMST.2015.2504600.

(2) Y. -C. Liu, M. -H. Lin and C. -C. Chang, "AV-Band Nine-State CMOS-MEMS Phase Shifter MMIC," 2022 IEEE 22nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), Las Vegas, NV, USA, 2022, pp. 88-90, doi: 10.1109/SiRF53094.2022.9720045.

(3) B. Biglarbegian, M. R. Nezhad-Ahmadi, **M.** Fakharzadeh and S. Safavi-Naeini,"Millimeter-Wave Reflective-lype Phase Shifter in CMOS Technology," in IEEE Microwave and Wireless Components Letters, vol. 19, no. 9, pp. 560-562, Sept. 2009, doi: 10.1109/LMWC.2009.2027065.

(4) B. Biglarbegian, M. -R. Nezhad-Ahmadi, **M.** Fakharzadeh and *S.* Safavi-Naeini,"A Wideband 90° continuous phase shifter for 60GHz phased array transceiver in 90nm CMOS technology," 2009 European Microwave Integrated Circuits Conference (EuMIC), Rome, Italy, 2009, pp. 479-482.

(5) F. Meng, K Ma, **K.** *S.* Yeo and S. Xu, "A 57-to-64-GHz 0.094-mm2 5-bit Passive Phase Shifter in 65-nm CMOS," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. *5,* pp. 1917-1925, May 2016, doi: 10.1 t09nvLSL2015.2469158.

(6) F. Ellinger, R. Vogt, and W. Bachtold, "Compact reflective-type phase-shifter **MMIC** for C-band using a lumped-.ilement coupler,"IEEE Trans. Mierow. Theory Tech., vol. 49, pp. 913-917, 2001.

[7] B. Biglarbegian, M. R Nezhad-Ahmadi, M. Fakharzadeh, and S.Safavi-Naeini, "Millimeter-wave reflective-type phase shifter in CMOS technology," IEEE Mierow. Wireless Compon. Lett., vol. 19, pp. 560-562, 2009.

[8] M. Jung and B.-W. Min, "A compact Ka-band 4-bit phase shifter with low group delay deviation," IEEE Mierow. Wireless Compon. Lett, vol. 30, no. 4, pp. 414-416, Apr. 2020.

[9] J.-H. Tsai, Y.-L. Tung, and Y-H. Lin, "A 27-42-GHz low phase error 5-bit passive phase shifter in 65-nm CMOS technology," IEEE Mierow. Wireless Compon. Lett., vol. 30, no. 9, pp. 900-903, Sep. 2020.

[10] J.-H. Tsai, F.-M. Lin, and H. Xiao, "Low RMS phase error 28 GHz 5-bit switch type phase shifter for SG applications," Electron. Lett., vol. 54, no. 20, pp. 118 1185, Oct. 2018.

[11] Y. -H. Lin and Z. -M. Tsai, "A Wideband Compact 5-Bit Phase Shifter With Low Loss and RMS Errors for SG Applications," in IEEE Microwave and Wireless Components Letters, vol. 31, no. 10, pp. 1134-1137, Oct 2021, doi: 10.1109/LMWC.2021.3107008.

[12] P. Sah and I. Mahbub, "A High Gain SIW Elliptically Polarized Antenna for Millimeter-Wave Applications," 2023 IEEE lntemational Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (USNC-URS[), Portland, OR, USA, 2023, pp. 1903-1904, doi: 10.l109/USNC-URSI52151.2023.10237514.

[13] P. Sah and I. Mahbub, "A 38° Wide Beam-Steerable Compact and Highly Efficient V-band Leaky Wave Antenna with Surface Integrated Waveguide for Vehicle-to-Vehicle Communication," 2023 IEEE Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS), Waco, TX, USA, 2023, pp. 1-5, doi: 10.l109/WMCS58822.2023.10194262.

[14] B. -W. Min and G. M. Rebeiz, "Single-Ended and Differential Ka-Band BiCMOS Phased Array Front-Ends," in IEEE Journal of Solid-State Circuits, vol. 43, no. 10, pp. 2239-2250, Oct. 2008, doi: 10.1109/JSSC.2008.2004336.

[I SJ G. -S. Shin et al., "Low Insertion Loss, Compact 4-bit Phase Shifter in 65 nm CMOS for SG Applications," in IEEE Microwave and Wireless Components Letters, vol. 26, no. l, pp. 37-39, Jan. 2016, doi: 10.l109/LMWC.2015.2505624.

[16] Y. -H. Lin and Z. **-M.** Tsai, "Frequency-Reconfigurable Phase Shifter Based on a 65-nm CMOS Process for SG Applications," in IEEE Transactions on Circuits and Systems ll: Express Briefs, vol. 68, no. 8, pp. 2825-2829, Aug. 2021, doi: 10.1109/TCSll.2021.3070051.

[17] A. Basaligheh, P. Saffari, S. R Boroujeni, I. Filanovsky, and **K.** Moez,"A 28-30 GHz CMOS reflection-type phase shifter with full 3600 phase shift range," IEEE Trans. Circuits Syst. ll, Exp. Briefs, vol. 67, no. 11, pp. 2452-2456, Nov. 2020.