Article

Multifunctional 2D FETs exploiting incipient ferroelectricity in freestanding SrTiO₃ nanomembranes at sub-ambient temperatures

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Incipient ferroelectricity bridges traditional dielectrics and true ferroelectrics, enabling advanced electronic and memory devices. Firstly, we report incipient ferroelectricity in freestanding SrTiO₃ nanomembranes integrated with monolayer MoS₂ to create multifunctional devices, demonstrating stable ferroelectric order at low temperatures for cryogenic memory devices. Our observation includes ultra-fast polarization switching (~10 ns), low switching voltage (<6 V), over 10 years of nonvolatile retention, 100,000 endurance cycles, and 32 conductance states (5-bit memory) in SrTiO₃-gated MoS₂ transistors at 15 K and up to 100 K. Additionally, we exploit room-temperature weak polarization switching, a feature of incipient ferroelectricity, to construct a physical reservoir for pattern recognition. Our results showcase the potential of utilizing perovskite material properties enabled by advancements in freestanding film growth and heterogeneous integration, for diverse functional applications. Notably, the low 180 °C thermal budget for fabricating the 3D-SrTiO₃/2D-MoS₂ device stack enables the integration of diverse materials into silicon complementary metal-oxide-semiconductor technology, addressing challenges in compute-in-memory and neuromorphic applications.

Perovskite materials have exhibited substantial potential for advancing the development of electronic devices and memory technologies[1–3]. In addition, a few perovskites stand out due to their exceptional properties, such as incipient ferroelectricity, which can significantly enhance their functionalities. Incipient ferroelectricity in a material indicates the presence of a polar soft mode that does not fully transition to ferroelectricity due to quantum effects inhibiting the change[4]. The most notable examples of incipient ferroelectrics include strontium titanate (SrTiO₃), calcium titanate (CaTiO₃), and potassium tantalate (KTaO₃)[5,6]. Although these materials are expected to retain their

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paraelectric or incipient ferroelectric properties even at low temperatures, stable ferroelectric orders can emerge in thin films due to nonidealities such as strain, defects, doping, and other structural modifications, even at room temperature[7,8]. Despite these exotic properties, incipient ferroelectric materials remain largely unexplored for developing solid-state devices for computing and storage applications.

In this article, we report the observation of incipient ferroelectricity at room temperature in freestanding nanomembranes of $SrTiO_3$ (STO) synthesized using hybrid molecular beam epitaxy (MBE). In addition, we observe a transition to a stable ferroelectric order below 100 K, which persists down to 15 K. We further exploit the incipient ferroelectricity in STO nanomembranes by integrating them with monolayer and semiconducting MoS_2, grown via metal-organic chemical vapor deposition (MOCVD), to develop solid-state devices for computing and cryogenic storage applications. Specifically, we exploit the pseudo-non-volatile polarization switching in STO-gated MoS_2 field effect transistors (FETs) at room temperature as a fading memory for reservoir computing (RC). Whereas the stable ferroelectric order at low temperatures allows us to present a cryogenic memory device with a fast-switching speed < 10 nanoseconds, a low-switching voltage < 6 V, nonvolatile retention projected to extend beyond 10 years, endurance surpassing 100,000 cycles, and the capability to store 32 distinct conductance states or 5-bit memory storage at 15 K and up to 100 K.

Note that, achieving high-quality, pinhole-free perovskite films with uniform coverage and minimal defect density on various semiconducting channel materials, including Si, remains a formidable challenge[9]. In this context, the recent breakthrough in hybrid MBE on the synthesis of freestanding[10] single-crystalline, epitaxial perovskite nanomembranes[11,12] using a binary oxide sacrificial layer, holds significant importance[13]. Such freestanding 3D STO nanomembranes[14] have already been integrated with mechanically exfoliated 2D semiconductors like MoS_2, leading to FETs with a high on/off current ratio of 10^8 and a minimum subthreshold swing of 66 mV decade^{-1} at room temperature[15]. Furthermore, monolayer MoS_2 has been integrated with STO membranes to realize a back-gated FET[16], resulting in enhanced performance. Given the relatively modest thermal demands for assembling 3D/2D nanomembrane-based devices, they can serve as catalysts for innovation, enabling the development of more compact and efficient devices within the CMOS back-end. Yet, the full potential of 3D/2D stacks becomes evident when they are leveraged for multifunctionality, tapping into the distinct electronic properties of the constituent materials within the stack, such as incipient ferroelectricity. This study bridges this gap by developing a cryogenic memory device and a hardware accelerator for RC based on STO-gated MoS_2 FETs. Supplementary Fig. 1 provides a concise overview of the key findings reported in this study.

Results

Characterization of freestanding 3D and 2D nanomembranes

A hybrid MBE system was utilized to synthesize an epitaxial, and crystalline SrO (002) sacrificial layer followed by an STO (001) film on LaAlO$_3$ (001) substrate as shown in Fig. 1a and discussed in detail in an earlier work[13]. Strontium (Sr) was supplied using an elemental solid source, titanium (Ti) was introduced through a metal-organic precursor, titanium tetra isopropoxide (TTIP), with oxygen (O_2) supplied from a radio frequency (RF) plasma source. Before initiating growth, the LAO substrates were heated to a temperature of 950 °C and cleaned with oxygen plasma for 10 minutes. Further details on the synthesis of STO are provided in the Methods section. The film quality was assessed using reflection high-energy electron diffraction (RHEED), as shown in Fig. 1b. The RHEED image displays a streaky pattern, indicating a smooth, epitaxial STO film. The atomic force microscopy (AFM) image in Fig. 1c reveals an atomically smooth

surface with a roughness of ~ 0.55 nm. The bright feature on the surface is likely due to hydration spots, attributed to the hygroscopic sacrificial layer[17]. Figure 1d presents the Wide-angle X-ray diffraction (XRD) 2θ-ω coupled scan of the STO/SrO/LAO (001) structure, confirming single-crystalline and epitaxial growth of SrO (002) and STO (001) on the LAO (001) substrate. The film exhibits clear Bragg peaks corresponding to STO, SrO, and LAO. In addition, the peak position of the as-grown STO (002) diffraction condition is found to be at 46.378° corresponding to an out-of-plane lattice parameter of $a_{STO} = 3.913$ Å, indicating the partially strained STO film. However, as shown in Supplementary Fig. 2, after transferring the STO film onto the SiO_2 substrate, the peak position was found to be at 46.473° corresponding to $a_{STO} = 3.905$ Å, indicating that the STO nanomembrane is fully relaxed. Figure 1e presents cross-sectional scanning transmission electron microscopy (STEM) high-angle annular dark-field (HAADF) imaging and energy-dispersive X-ray spectroscopy (EDS) elemental mapping of the as-grown STO film on SrO/LAO. The images confirm the phase purity and crystallinity of the STO layer.

Next, we characterized the freestanding MoS_2 monolayer film grown via MOCVD on a 2-inch a-plane sapphire substrate, as shown in Supplementary Fig. 3. Figure 1f–i shows the Raman spectra and corresponding spatial colormaps of two Raman-active modes, E_{2g}^1 and A_{1g}, along with their peak separation across a 20 μm × 20 μm area. The mean and standard deviation for E_{2g}^1 and A_{1g} were ~ 384.7 cm^{-1} and ~ 0.1 cm^{-1} and ~ 405.1 cm^{-1} and ~ 0.1 cm^{-1}, respectively, with a peak separation mean of ~ 20.3 cm^{-1} and a standard deviation of ~ 0.1 cm^{-1}. Figure 1j, k displays the photoluminescence (PL) spectra and the spatial colormap of the PL peak position across the same area. The PL peak position averaged around 1.84 eV with a standard deviation of ~ 0.008 eV, confirming the monolayer nature of the MoS_2 film. Finally, the STEM-HAADF image of MoS_2, viewed along the c-axis (Fig. 1l), along with selected area electron diffraction (SAED) in Fig. 1m, reveals the crystalline 2H phase. Additional information regarding the growth and characterization of STO nanomembrane and monolayer MoS_2 films is available in the Methods section.

Integration of 2D/3D nanomembranes

Next, 3D and 2D nanomembranes were stacked using a low-thermal budget fabrication process flow for the construction of FeFETs. Initially, electron beam (e-beam) lithography followed by e-beam evaporation was employed to create patterns for local back-gates comprising a stack of 5 nm Ti/ 25 nm Pt on a commercially acquired SiO_2/Si substrate. Next, a thin polydimethylsiloxane (PDMS) sheet was attached to the top of the as-grown STO thin film. Subsequently, the stack was immersed in a deionized (DI) water bath to etch away the sacrificial SrO layer[13] This process resulted in the creation of an STO membrane adhering to the PDMS sheets. Supplementary Fig. 4 provides optical images of the STO membrane attached to PDMS. Next, the PDMS/STO membrane was transferred onto our pre-constructed back-gate metal stack, and the PDMS stamp was mechanically extracted, leaving the STO on the substrate to function as the back-gate dielectric. The monolayer MoS_2 was then transferred onto the local back-gate islands using a poly(methylmethacrylate) (PMMA)-assisted wet transfer technique. The device's channel length ($L = 1$ μm) and width ($W = 1$ μm) were defined through e-beam lithography, followed by reactive ion etching (RIE) with SF_6 plasma at a temperature of 5 °C. Finally, source and drain contacts were patterned via e-beam lithography, and a 40 nm Ni/30 nm Au layer was deposited using e-beam evaporation. Figure 2a–c illustrates the schematic diagram, top-view optical image, and top-view scanning electron microscope (SEM) image of the local back-gated 3D/2D stacked FET, which features Ni/Au contacts, a MoS_2 channel, and an STO nanomembrane as the gate dielectric. In addition, Fig. 2d, e present the cross-sectional STEM-HAADF image and corresponding elemental mapping from EDS of the
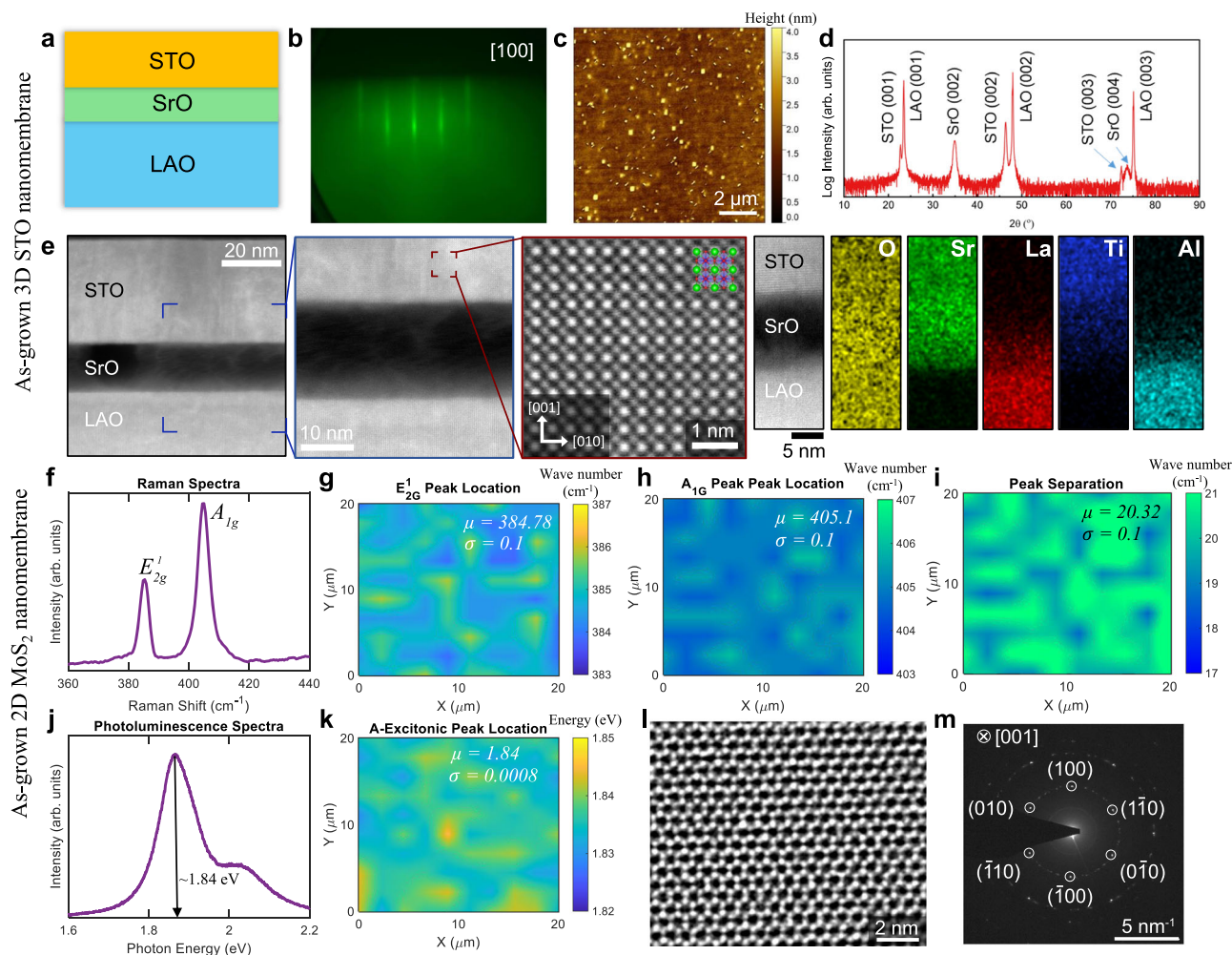
Fig. 1 | Characterization of as-grown SrTiO₃ and monolayer MoS₂. a Schematic illustrating SrTiO₃ (STO) thin film on LAO substrate, with a sacrificial layer of SrO grown via the hybrid molecular beam epitaxy (MBE). **b** Reflection high-energy electron diffraction (RHEED) pattern after STO growth. **c** The atomic force microscopy (AFM) and (**d**) X-ray diffraction (XRD) analysis of the as grown STO film. **e** Cross-sectional high-angle annular dark-field (HAADF)-scanning transmission electron microscopy (STEM) imaging and the accompanying energy-dispersive X-ray spectroscopy (EDS) elemental mapping of the STO/SrO/LAO structure indicate phase purity, single crystallinity, and uniform growth of the STO film. **f** Raman spectra obtained from metal-organic chemical vapor deposition (MOCVD) MoS₂

film using 532 nm laser at 1% power shows the characteristic in-plane E^1_{2g} and out-of-plane A_{1g} modes at 384.7 cm⁻¹ and 405 cm⁻¹ respectively, with a peak-to-peak distance of ~ 20.3 cm⁻¹. Raman maps for (**g**) E^1_{2g} peak position, (**h**) A_{1g} peak positions, and (**i**) peak separation measured over a 20 μm × 20 μm area. The mean and standard deviation values are shown in the inset. **j** Photoluminescence (PL) spectra with characteristic monolayer peak at 1.84 eV. **k** Colormap for the PL peak position, measured over a 20 μm × 20 μm area. **l** STEM-HAADF image and (**m**) selected area electron diffraction (SAED) of monolayer MoS₂ film viewed down its c-axis at an accelerating voltage of 80 kV. All of these characterizations indicate the quality of the monolayer MoS₂.

2D/3D stack, showing the interface between the STO film and MoS₂ channel.

Next, we assessed the electrical characteristics of the 3D/2D stacked FETs. The single-sweep and room-temperature transfer characteristics i.e., source-to-drain current (I_{DS}), measured against the local back-gate voltage (V_{BG}) at a constant drain-to-source voltage (V_{DS}) of 1 V for 30 STO-gated MoS₂ FETs plotted in logarithmic scale are shown in Fig. 2f. These FETs display unipolar electron transport consistent with the previous findings, attributed to the Fermi-level pinning of the metal contact in close proximity to the conduction band of MoS₂. Furthermore, small variations in the transfer characteristics of the 2D FETs can be noticed across different devices. These variations may be attributed to residues and wrinkles introduced during the 3D and 2D membrane transfer processes involving PDMS and PMMA, respectively.

Figure 2g–i, respectively, show the corresponding distributions for extracted maximum on-state current (I_{max}), on/off current ratio (I_{ON}/I_{OFF}), and subthreshold slope (SS) measured for 2 orders of

magnitude change I_{DS}. The mean values for I_{max}, I_{ON}/I_{OFF}, and SS were found to be 4.8 μAμm⁻¹, 4.8 × 10⁶, and 220 mV decade⁻¹, respectively. Here, the large SS values of the STO-gated MoS₂ FETs can be attributed to the presence of trap charges at the defect sites located at the MoS₂/STO interface. It was noteworthy that, despite having a relatively small bandgap of approximately 3.2 eV, the 80 nm STO nanomembrane exhibited a relatively low gate leakage current (I_{BG}), as indicated by the corresponding histograms extracted for $V_{BG} = 3$ V and $- 3$ V in Fig. 2j.

Incipient ferroelectricity and non-volatile retention

In order to probe the interface between STO and MoS₂, dual sweep transfer characteristics of an STO-gated MoS₂ FET were measured at room temperature as shown in Fig. 3a. We observe a counterclockwise hysteresis window, a characteristic frequently encountered in ferroelectric FETs. This counterclockwise hysteresis arises from a specific mechanism: when the positive/negative gate voltage exceeds the coercive field (E_C), the polarization in the FE film aligns toward/away from the channel as shown in Fig. 3b, resulting in accumulation/
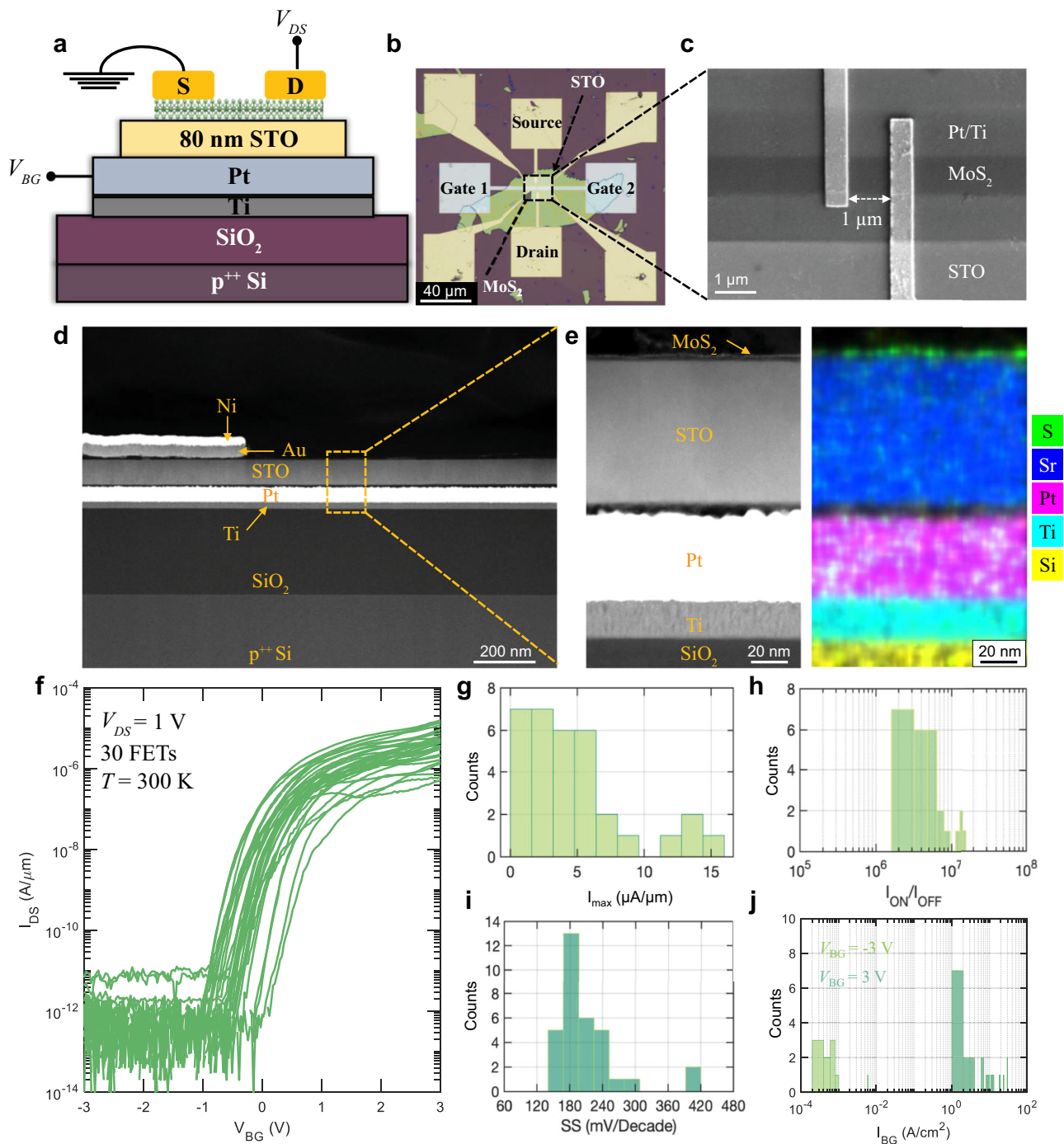
Fig. 2 | Integration of 2D MoS₂/3D STO nanomembranes for functional devices.
a Device schematic, (**b**) top-view optical image. **c** Scanning electron microscope
(SEM) image of a representative field-effect transistor (FET) based on 2D MoS₂/3D
STO nanomembranes. The FET is locally back-gated with Ti/Pt serving as the back-
gate electrode, 80 nm STO as the gate dielectric, monolayer MoS₂ as the semi-
conducting channel, and Ni/Au as the source and drain contacts. The channel
length and width of the devise are $L = 1\,\mu m$ and $W = 1\,\mu m$, respectively. **d** Cross-
sectional STEM-HAADF image of the fabricated FET based on 2D MoS₂/3D STO
nanomembranes. **e** An enlarged STEM-HAADF view of the boxed region in (**d**) and
corresponding EDX elemental mapping. **f** Transfer characteristics, i.e., source-to-
drain current (I_{DS}) as a function of the back-gate voltage (V_{BG}) for a constant
source-to-drain bias of $V_{DS} = 1\,V$, of 30 MoS₂/STO FETs. Distributions of (**g**) max-
imum on-state current (I_{max}), (**h**) on/off current ratio (I_{ON}/I_{OFF}), (**i**) subthreshold
slope (SS) measured for 2 orders of magnitude change I_{DS}, and (**j**) gate leakage (I_{BG})
extracted at $V_{BG} = -3\,V$ (light green) and $V_{BG} = 3\,V$ (shown in dark green) for these
30 MoS₂/STO FETs.

depletion of electrons in the channel, which give rise to low/high
threshold voltage, respectively. The ferroelectric-like behavior was
also confirmed by measuring the dual sweep transfer characteristics of
10 other STO-gated MoS₂ FETs, as shown in Supplementary Fig. 5, all of
which demonstrated counterclockwise hysteresis. This outcome is
surprising because bulk and pure STO typically lack ferroelectricity
due to quantum fluctuations in atomic positions, categorizing it as an

incipient ferroelectric material[17]. It is well-established that ferroelectric
behavior can emerge in STO under certain conditions, such as when it
is in the form of a thin-film, subjected to strain or strain gradients,
modified by alloying, influenced by an electric field, or exposed to
specific stress environments. [18–23]. Moreover, defects like Ti, Sr, and/or
O vacancies have been reported to induce ferroelectricity in STO thin
films[8,24,25].

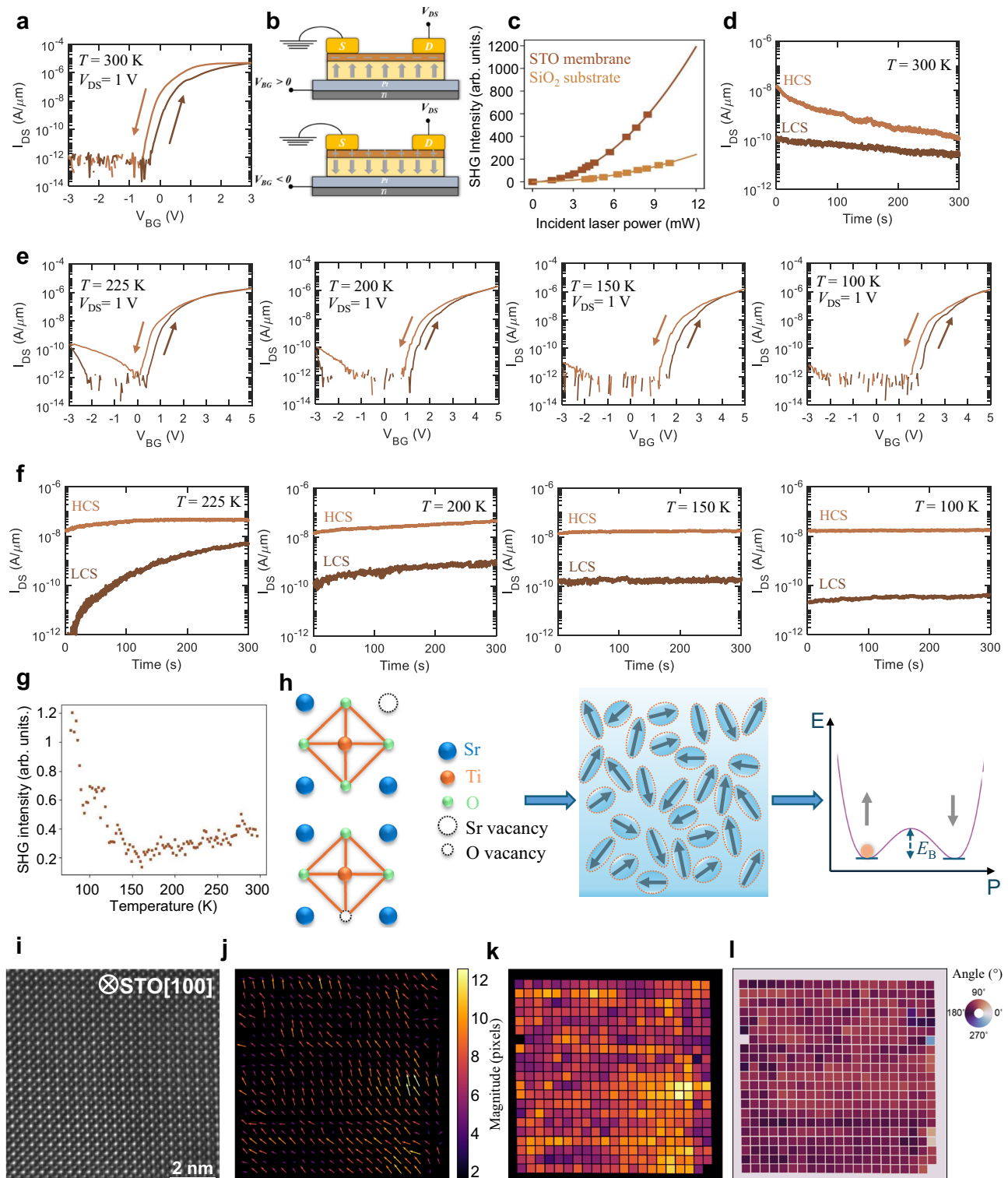**Fig. 3 | Observation of incipient ferroelectricity in STO-gated MoS₂ FET. a** Dual sweep transfer characteristics of a representative STO-gated MoS₂ FET measured at $T = 300$ K. **b** Schematic showing polarization switching in STO film can lead to low/high threshold voltage in MoS₂ FETs. **c** Optical characterization of the freestanding STO nanomembrane at $T = 300$ K using second harmonic generation (SHG) at normal incidence as a function of the incident fundamental laser power. **d** Non-volatile retention of memory states for STO-gated MoS₂ FET at $T = 300$ K. **e** Dual sweep transfer characteristics and (**f**) memory retention for STO-gated MoS₂ FET measured at different temperatures, $T = 225$, 200, 150, and 100 K. Counterclockwise hysteresis is retained at all

temperatures. However, memory retention improves significantly at lower temperatures. **g** Temperature-dependent SHG measurements show that the SHG intensity is maximum at 77 K and decreases with increasing temperature up to -150 K, followed by a gradual increase until 300 K. The enhanced SHG intensity at lower temperatures agrees with memory retention results. **h** Schematic showing the possible origin of ferroelectricity in STO nanomembrane. **i** Atomic resolution HAADF STEM image of the STO film under the contact electrode. Corresponding maps of (**j**) the projected polar displacement vector on the (100) plane, and its (**k**) magnitude and (**l**) direction.

To further understand the ferroelectric-like behavior in STO-gated MoS_2 FETs, we performed optical second harmonic generation (SHG) on the freestanding STO nanomembrane. The second harmonic response of a material requires inversion symmetry to be broken at the atomic scale, allowing SHG to reveal the presence of local polar order. Our SHG measurements used an 800 nm fundamental beam incident on the sample at normal or 45-degree incidence, and the reflected light at 400 nm was measured. Figure 3c shows the SHG intensity measured at room temperature at normal incidence as a function of the incident fundamental laser power. The incident power was optimized to ensure that the SHG signal from the SiO_2/Si substrate underneath the STO membranes was minimized. The quadratic nature of the curve indicates broken inversion symmetry, and hence provides evidence of existing polar order, even at room temperature.

Since the spontaneous and switchable polarization in ferroelectric materials can be harnessed for non-volatile storage devices, we assessed the retention for both the high conductance state (HCS) and low conductance state (LCS) over a period of 100 s, as illustrated in Fig. 3d for our STO-gated MoS_2 FET. Interestingly, the retention of the two memory states was found to be poor, suggesting that stable polarization states can be difficult to sustain for a long time in the STO nanomembrane at room temperature, owing to the incipient nature of ferroelectricity in the STO film. We also investigated the piezoresponse force microscopy (PFM) of the STO film on a gold-plated substrate at room temperature. Supplementary Figs. 6a–c shows the topography, PFM amplitude and PFM phase, respectively. The polarization reversal results, shown in Supplementary Fig. 6d, confirm domain switching, whereas the unsaturated ferroelectric phase demonstrates its instability, reaffirming the incipient nature of ferroelectricity at room temperature in STO nanomembranes.

To understand and probe the impact of incipient ferroelectricity in STO-gated MoS_2 FETs, we measured the dual sweep transfer characteristics and corresponding retention of the HCS and LCS at different temperatures, $T = 225, 200, 150$, and 100 K, as illustrated in Fig. 3e, f, respectively. Notably, a counterclockwise hysteresis is observed at all temperatures. However, as the temperature decreased, we observed a gradual enhancement in the retention of the two memory states. This suggests that stable polarization switching within the STO nanomembrane becomes more reliable at lower temperatures. We also measured the SHG intensity from STO nanomembranes as a function of temperature down to 77 K, as shown in Fig. 3g. The SHG intensity is maximum at the lowest measured temperature and decreases as the temperature is increased up to ~150 K, after which it rises gradually with temperature. Our SHG intensity variation is in excellent agreement with the electrical characterization and can explain the observed temperature-dependent nonvolatile retention of polarization switching in STO-gated MoS_2 FETs. The electrical data, combined with the SHG measurements, suggest that ferroelectricity in STO nanomembranes can be ascribed to the field-induced long-range correlation between pre-existing nanopolar regions that thermally decay with time[23]. Increasing the temperature leads to increased thermal fluctuations, that accelerate the destabilization of the polar order. This is depicted schematically in Fig. 3h. While strain-free STO is expected to be paraelectric, we believe that the observed polar order could arise due to defects such as oxygen vacancies, Sr vacancies, etc. Interestingly, the polar order observed in STO membranes persists even up to room temperature.

To further confirm the existence of incipient ferroelectric order in the STO film at room temperature, we took the cross-sectional atomic resolution STEM-HAADF images of the STO layer on [100] zone axis for the region under the electrode as shown in Fig. 3i. The atomic resolution images are further processed using the Atomap software package[26] for the detection of positions of the Sr and Ti atom columns. The projection of the polar displacement vector on the (100) plane in STO is determined by measuring the displacement of Ti atom column from the center of the four surrounding Sr atom columns on the (001) plane. A vector plot, with vectors pointing toward the Ti atom columns, is used to illustrate the magnitude and direction of the projected polar displacement on the (100) plane, as shown in Fig. 3j–l. The projected polar displacement vector of STO on (100) plane shown in the image is mostly along the same direction, pointing from bottom to top, with varying magnitudes forming several nanodomains.

It is noteworthy to highlight that a counterclockwise hysteresis may also originate from the presence of mobile ions in the dielectric or incipient ferroelectric material. Moreover, under an external electric field, the mobile ions can migrate throughout the material, resulting in a reversal in the hysteresis[27], as observed in many non-ferroelectric transistors. To substantiate that the counterclockwise hysteresis in our STO-gated MoS_2 FETs stems from the incipient ferroelectric nature of STO rather than mobile ion migration, we conducted voltage sweep-rate (t_{sweep}) dependent measurements on these FETs. Supplementary Fig. 7a shows the transfer characteristics at different temperatures, $T = 200$ K, 100 K, and 15 K t_{sweep}, varying from 2 ms (fastest) to 10 s (slowest). Note that mobile ions need sufficient activation energy to migrate, and at low temperatures, such as 100 K or below, their movement becomes severely restricted. Furthermore, if the t_{sweep} is too slow, the mobile ions will reach equilibrium with the applied field, causing the hysteresis to diminish. However, if the gate dielectric exhibits ferroelectric order, the hysteresis window would remain, as polarization switching is not strongly dependent on t_{sweep}. Supplementary Fig. 7b shows the memory or hysteresis window as a function of t_{sweep} for $T = 200$ K, 100 K, and 15 K. It is evident that the memory window predominantly remains constant as the t_{sweep} varied. Hence, it can be stated that the counterclockwise hysteresis in the STO-gated MoS_2 FETs has originated from the incipient ferroelectric nature of the STO nanomembranes.

Construction of cryogenic memory and neuromorphic hardware

The observed temperature-dependent stability of ferroelectric orders in STO-gated MoS_2 FET presents an opportunity for developing a fast, low-power, cryogenic memory at lower temperatures as well as hardware for neuromorphic computing at room temperature.

It is quite well known that cryogenic computing and memory components are crucial, particularly in the context of space electronics and in developing quantum computers. Note that conventional superconducting memories often fall short in terms of higher memory density and energy efficiency. Recently, a Si-doped HfO_2 FeFET based cryogenic memory has been demonstrated, operating at 6.9 K with large memory window even at lower temperatures[28]. In this context, we explore the possibility of developing a cryogenic memory system exploiting stable ferroelectric order in STO-gated MoS_2 FETs.

First, we evaluate the switching voltage required to operate the ferroelectric-like STO-gated MoS_2 FET at $T = 15$ K. To extract the switching voltage for the HCS, transfer characteristics were measured with different sweeping ranges, maintaining a constant negative $V_{BG} = -3$ V and progressively increasing the positive V_{BG} from 3 to 7 V in increments of 0.5 V, as depicted in Fig. 4a. To extract the switching voltage for the LCS, similar nested transfer characteristics were measured with constant positive $V_{BG} = 6$ V and gradually increasing negative V_{BG} of 0 to -4 V in the step of 0.5 V, as illustrated in Fig. 4b. The MW, which is defined as the difference between the threshold voltages (measured at an iso-current of 10 nA μm^{-1}) corresponding to the HCS and LCS are plotted against the positive and negative sweep range in Fig. 4c, The MW disappears for $V_{BG} < 3.5$ V and reaches saturation for $V_{BG} > 6$ V, indicating complete polarization switching in the STO nanomembrane for $V_{BG} = 6$ V for the HCS. Similarly, the MW vanishes for $V_{BG} > -1$ V and saturates for $V_{BG} < -3.5$ V, indicating that the switching voltage for the LCS is established at $V_{BG} = -3$ V. It is noteworthy that, even with an STO nanomembrane thickness of 80 nm, the
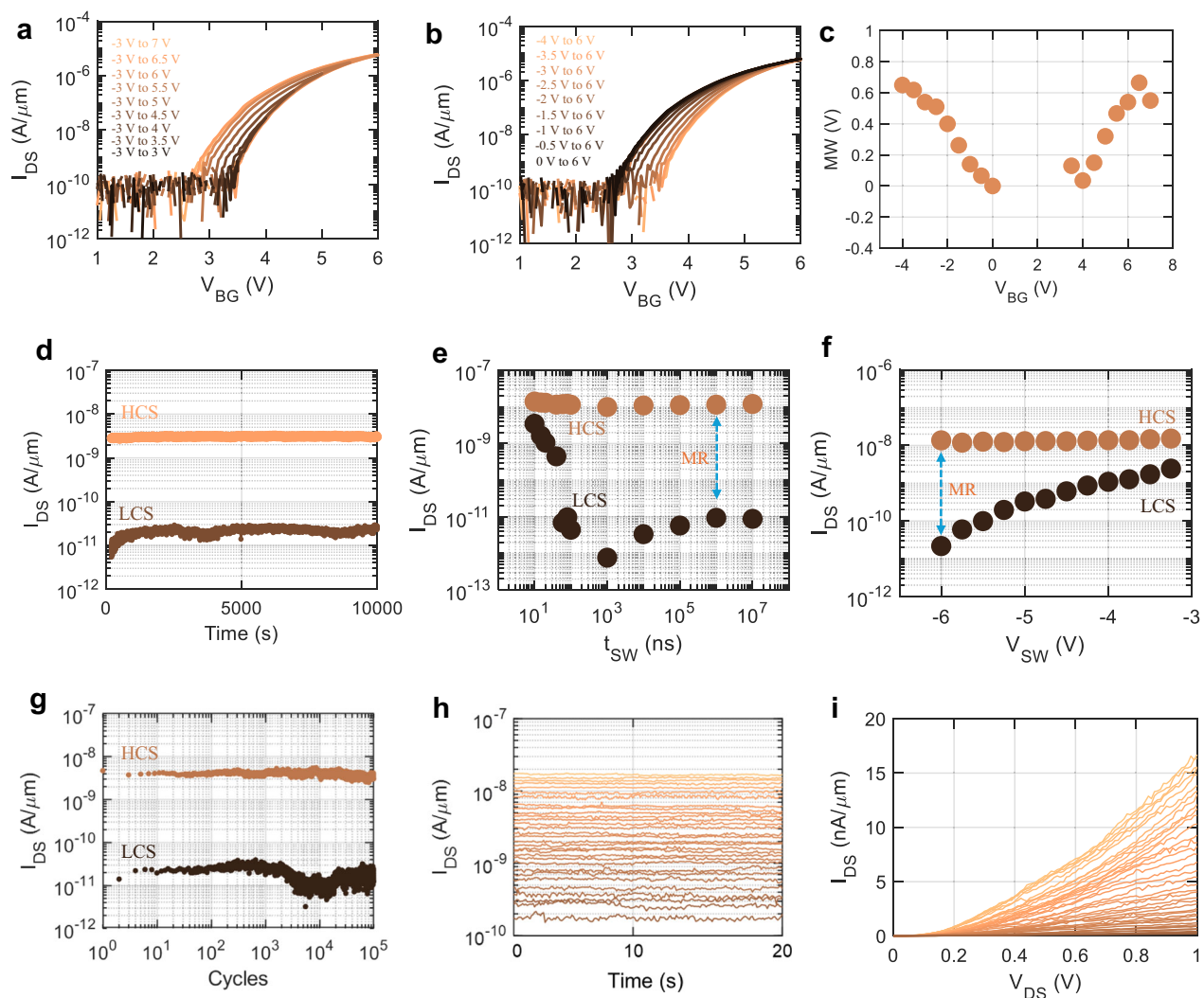
Fig. 4 | STO-gated MoS$_2$ FET as cryogenic memory. Dual sweep transfer characteristics of a ferroelectric-like STO-gated MoS$_2$ FET using different V_{BG} sweep ranges (**a**) keeping a constant negative $V_{BG} = -3$ V and gradually increasing the positive V_{BG} from 3 to 7 V and (**b**) keeping a constant positive $V_{BG} = 6$ V and gradually increasing the negative V_{BG} from 0 to -4 V. **c** Memory window (*MW*) plotted as a function of the V_{BG} range used in (**a**) and (**b**). **d** Memory retention measured for 1×10^4 s. **e** *HCS and LCS* as a function of switching time (τ_{SW}). The STO film can be switched as fast as 60 ns without any degradation to the *MR*. **f** HCS and LCS as a

function of V_{SW} for $\tau_{SW} = 10$ ns. With the application of $V_{SW} = -6$ V, the τ_{SW} can be as low as 10 ns to achieve the same MR obtained in (**e**). **g** Switching endurance for the STO film was assessed for 10^5 cycles with no degradation to the *MR*. **h** 32 memory states obtained by applying different amplitude of programming pulses of fixed $\tau_{SW} = 10$ ms to form a 5-bit memory storage device. **i** output characteristics corresponding to each memory state shown in (**h**). The output characteristics are linear, even at 15 K.

switching voltages (V_{SW}) remain below 6 V, correlating to $E_C \sim 0.75$ MV cm^{-1}.

Next, we evaluated the retention, switching speed, and endurance for a representative STO-gated MoS$_2$ FET. The retention for the HCS and LCS were measured for a duration of 10,000 seconds without any visible degradation in the MR as shown in Fig. 4d, confirming non-volatile polarization switching in the STO nanomembrane at 15 K. The projected retention was found to be more than 10 years. The switching speed for the STO film was accessed using V_{BG} pulses with a pulse width (τ_{SW}) down to 10 ns. Figure 4e shows the HCS and LCS as a function of τ_{SW}. The extracted MR function τ_{SW} is shown in Supplementary Fig. 8a. We have used $V_{BG} = 6$ V and $V_{BG} = -3$ V to switch the STO film between HCS and LCS, with τ_{SW} ranging from 10 ms down to 10 ns. We found that the STO film can be switched as fast as 60 ns without any visible degradation in the MR. However, with shorter pulses the MR decreases monotonically. Interestingly, by using higher magnitude V_{BG} pulses, MR can be recovered even for $\tau_{SW} = 10$ ns, as illustrated in Fig. 4f and Supplementary Fig. 8b. In essence, a reciprocal

relationship exists between the pulse width and pulse amplitude when switching the ferroelectric polarization: specifically, a shorter pulse width necessitates a higher pulse amplitude, and conversely, a reduced amplitude can be compensated with a longer pulse width[29]. Finally, the switching endurance for the STO film was accessed for 10^5 cycles, as shown in Fig. 4g and no degradation was seen in the MR.

Next, we leverage the minor loops found in the transfer characteristics of STO-gated MoS$_2$ FETs to showcase multi-bit memory storage within a single device. The appearance of these minor loops stems from the partial polarization switching of ferroelectric domains beneath the semiconducting channel and can be attributable to the stochastic domain switching dynamics even in incipient ferroelectric materials. Figure 4h illustrates the successful manifestation of 5-bit memory storage corresponding to 32 distinct memory states obtained by applying different amplitudes of programming pulses of fixed $\tau_{SW} = 10$ ms. The MR between the states can be increased by reducing the number of states as shown in Supplementary Fig. 9 for 2-bit and 4-bit memory storage corresponding to 4 and 16 memory states
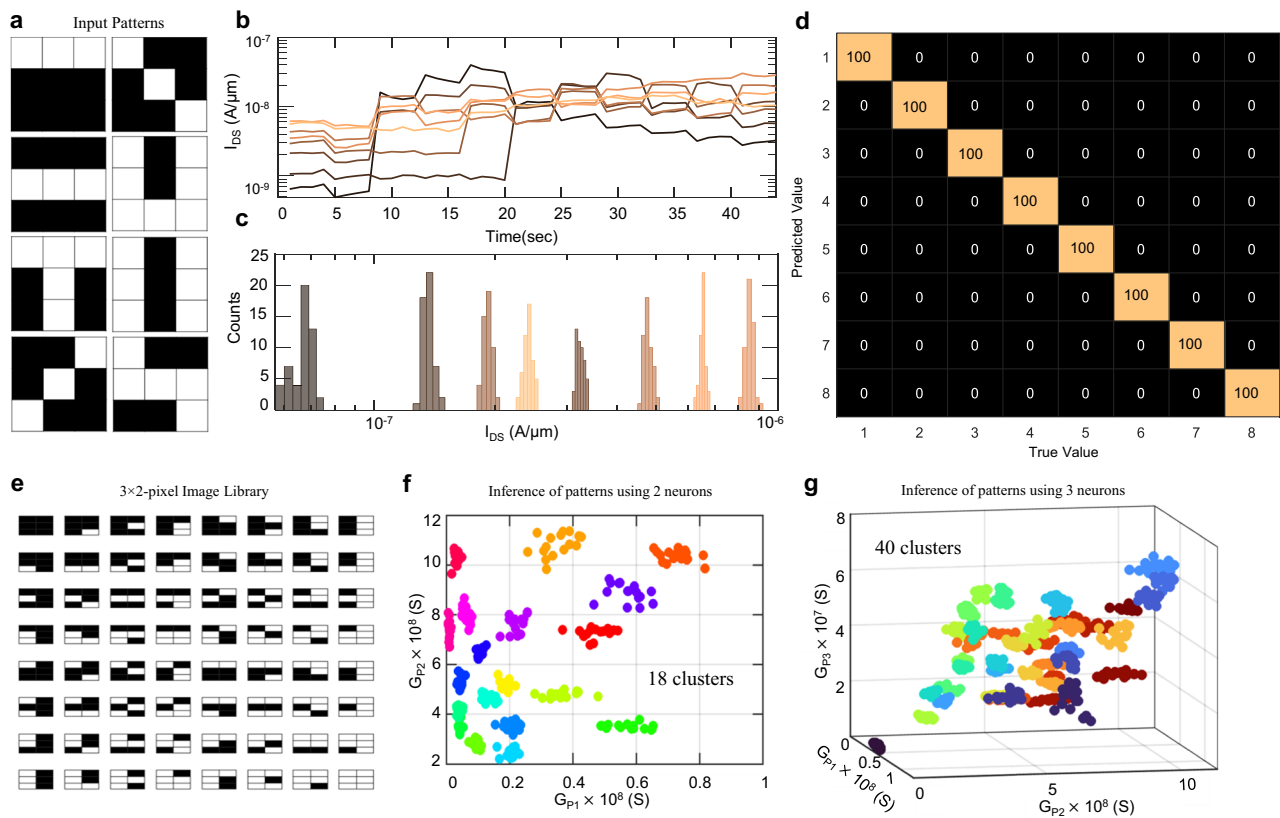
Fig. 5 | Reservoir computing at room temperature. a 8 patterns corresponding to 3 × 3-pixel images translated into voltage values (V_{BG} = 3 V and V_{BG} = − 1 V for bright and dark pixels respectively) and applied to the artificial neuron (**b**) Evolution of conductance values for 8 different patterns resulting in distinct final conductance values (G_p) distinguishing each pattern. **c** Distribution of measured conductance, G_p, corresponding to each pattern over multiple experimental cycles. **d** Confusion matrix showing 100% accuracy in distinguishing and predicting the labels for the tested patterns. **e** Image libraries consist of all possible patterns ($2^6 = 64$) corresponding to 3 × 2-pixel images. Corresponding G_p distributions for (**f**) 2 neurons and (**g**) 3 neurons in 2D and 3D plots. Distinct clusters of 18 and 40 patterns emerge, underscoring the potential to discern an increasingly greater number of patterns by expanding the number of neurons. This phenomenon capitalizes on device-to-device variations across STO-gated MoS₂ FETs, resulting in distinct conductance bands for the same pattern when applied to different devices.

Finally, Fig. 4i presents the output characteristics corresponding to each memory state, revealing linear characteristics even at low temperatures. Similar results were also observed at T = 100 K, as shown in Supplementary Fig. 10.

Multibit operation is a pivotal feature for cryogenic memory technologies that require high-density data storage. While HZO-based FeFETs demonstrate cryogenic storage capability, multi-bit implementations have not been previously achieved. In this context, our demonstration of fast switching, long retention, high endurance, low-voltage operation, and 5-bit memory in STO nanomembrane-gated 2D FETs stands out as a significant advancement in cryogenic memory technology.

Furthermore, we harness the room-temperature non-retentive polarization switching in the STO-gated MoS₂ FET to construct a physical reservoir for accelerating RC. Note that, RC, derived from the framework of recurrent neural networks (RNNs), has emerged as a powerful computational paradigm for processing time-series data and performing pattern recognition[30,31]. It utilizes a fixed, randomly connected network of nonlinear units, known as the reservoir, to map lower-dimensional data into a higher-dimensional space. RC also requires a dynamic or fading memory to ensure that the reservoir gradually forgets previous inputs as new ones are introduced, enabling it to consider both current and past inputs effectively. Here, we leverage the device-to-device variation in STO-gated MoS₂ FETs for mapping unidimensional input stimuli (gate voltage) applied to each device into multidimensional conductance space and pseudo-non-

volatile retention of polarization switching in STO as fading memory to construct the physical reservoir for RC.

First, we show that it is possible to distinguish between 8 discrete patterns corresponding to the 3 × 3-pixel images using a reservoir consisting of a single STO-gated MoS₂ FET. These patterns are shown in Fig. 5a. The pixel values were translated into V_{BG} values with V_{BG} = − 1 representing the dark pixels and V_{BG} = 3 V representing the bright pixels, then transformed into a one-dimensional array and applied to the FET. Figure 5b shows the evolution of each pattern with the final conductance (G_p) values being different for each pattern. This experiment was repeated multiple times, with the distribution G_p displayed in Fig. 5c. Evidently, despite the cycle-to-cycle variation, each distribution forms an individual band, facilitating the inference of the 8 patterns. Figure 5d shows the confusion matrix with near 100% accuracy between the predicted and true labels for the tested patterns. The discernible number of distinct patterns can exhibit super-linear growth when multiple devices are used to construct the reservoir. To illustrate, in Fig. 5e, we present a comprehensive library comprising all conceivable combinations ($2^6 = 64$) of 3 × 2-pixel images, which can serve as a foundation for generating any N × M pixel image. Supplementary Fig. 11 shows that it is difficult to discern more than 8 random patterns when the reservoir comprises only one FET, as the G_p distributions overlap. However, when we represent the G_p distributions of 2 and 3 FETs in 2D and 3D plots, distinct clusters of 20 and 48 patterns emerge, as depicted in Fig. 5f, g, respectively. This underscores the potential to discern an increasingly greater number of patterns by expanding the

number of FETs within the reservoir. Notably, the multi-bit memory and the dynamic polarization switching in STO-based 2D FETs can be harnessed across various neuromorphic computing applications, such as reinforcement learning. To address this more directly, the multi-state capabilities of STO-gated 2D FETs can be harnessed to act as multi-bit synapses capable of storing multiple weights (conductance states) in brain-inspired reinforcement learning scenarios, as shown in ref. 32.

In addition, a benchmarking table has been illustrated in Supplementary Table 1, which outlines and compares the performance metrics of our STO-based MoS$_2$ FETs against the state-of-the-art FeFET candidates. This table offers a clear, concise comparison, emphasizing the competitive advantages and distinct features of our STO-based FETs compared to other ferroelectric devices in the field.

In conclusion, the integration of crystalline STO nanomembranes with monolayer MoS$_2$ films presents a promising approach for developing BEOL-compatible ferroelectric-like FETs, as well as pioneering cryogenic memory technology. These devices not only display rapid and stable ferroelectric polarization switching at temperatures up to 200 K but also feature high-speed, low-power operation, and long-term retention. Furthermore, we utilized the unstable polarization switching at room temperature, a hallmark of incipient ferroelectricity, to construct a physical reservoir for pattern recognition. This research highlights the potential of exploiting exotic material properties through heterogeneous material integration, enabled by advances in the growth of freestanding films, for a wide range of functional applications.

Methods
Growth and characterization of STO membranes
A hybrid Molecular Beam Epitaxy (MBE) system (EVO-50 by Scienta Omicron Inc), was utilized to synthesize an epitaxial, and single crystalline 15 nm SrO (002) sacrificial layer followed by a 80 nm STO (001) film on LaAlO$_3$ (001) substrate. Sr was supplied using an elemental solid source sublimated in a thermal effusion cell, maintaining a beam equivalent pressure (BEP) of 5.8×10^{-8} Torr during SrO and STO growth. Titanium was introduced using a metal-organic precursor, titanium tetra isopropoxide (TTIP), injected through a gas injector with a vapor inlet system, achieving a BEP of 3.3×10^{-6} Torr for an adsorption-controlled stoichiometric STO growth. Oxygen was supplied via a radio frequency (RF) plasma source at a pressure of 5×10^{-6} Torr, operating at 250 W. Before the beginning of the growth, the LAO substrates were heated to a growth temperature of 950 °C (thermocouple temperature). The substrate was cleaned using the oxygen plasma for 10 minutes. Following the oxygen plasma cleaning, an epitaxial SrO(001) layer was grown using the Sr and oxygen plasma source for 15 min, followed by the growth of the epitaxial STO(001) film by co-supplying Sr, Ti, and oxygen plasma for 30 min. Film surfaces were monitored using reflection high-energy electron diffraction (RHEED) after the growth of the SrO(001) and STO(001) layers. Atomic force microscopy (AFM) was employed for surface characterization using the Nanoscope V Multimode 8 by Bruker. The structural properties of the grown film were assessed through high-resolution X-ray diffraction using the SmartLab XE by Rigaku with Cu Kα radiation.

Fabrication of local back-gate islands
To define features with a local gate island configuration, a commercially sourced p^{++}-Si substrate with a 285 nm SiO$_2$ layer was prepared by spin-coating with a bilayer of PMMA resist in a two-step process, followed by sequential baking at 185 °C and 95 °C for 60 and 90 s, respectively. Using an EBPG 5200 Vistec Electron Beam Lithography tool, individual islands were precisely patterned on the substrate. The exposed resist was developed in a 1:1 solution of 4-methyl-2-pentanone (MIBK) and 2-propanol (IPA) to reveal the patterned features. After a thorough O$_2$ plasma sputter clean, local-gate electrodes were

deposited with a 5 nm titanium and 25 nm platinum stack via a Temescal e-beam evaporator, completing the configuration.

STO nanomembrane transfer to local back-gate substrate
The transfer of the STO membrane onto the fabricated local back-gate islands was accomplished using a PDMS stamp. Initially, the PDMS stamp was delicately applied to the STO/SrO/LAO sample. Subsequently, the PDMS/STO/SrO/LAO assembly was immersed in DI water at room temperature for an hour to dissolve the SrO layer. Following the removal of the sacrificial SrO layer, tweezers were used to separate the LAO substrate from the PDMS/STO assembly. Any remaining water on the STO membrane was expelled using N$_2$ gas. The STO membrane with the PDMS was then positioned on the target substrate (the fabricated local back-gate islands) and manually pressed with a thumb, resulting in the PDMS/STO/target substrate structure. Following this, the PDMS stamp was carefully detached from the substrate using tweezers, resulting in the transfer of the STO membrane onto the fabricated local back-gate substrate.

Large-area MoS$_2$ film growth and its TEM/STEM characterization
The growth of MoS$_2$ film on 2" a-plane sapphire substrates was carried out in a metal-organic chemical vapor deposition (MOCVD) system (DOI: 10.60551/znh3-mj13) equipped with a cold-wall horizontal reactor with an inductively heated graphite susceptor with gas-foil wafer rotation. Molybdenum hexacarbonyl (Mo(CO)$_6$) (99.99%, Sigma-Aldrich) was used as the metal precursor while hydrogen sulfide (H$_2$S) was the chalcogen source with H$_2$ as the carrier gas. The Mo(CO)$_6$ powder was maintained inside stainless-steel bubbler where the temperature and pressure at 25 °C and 625 Torr, respectively. The MoS$_2$ film was grown in a single-step process[33]. Before the growth, the sapphire was ramped up under N$_2$ to the growth temperature at 1000 °C and pre-annealed for 10 mins. During the growth, H$_2$S and Mo(CO)$_6$ were introduced to the reactor for a designated time to complete MoS$_2$ film growth in a single step. The molybdenum flow rate was set as 4.7×10^{-3} sccm and the chalcogen (H$_2$S) flow rate was set as 400 sccm while the reactor pressure was maintained at 50 Torr. Then, the MoS$_2$ film was annealed under H$_2$ and H$_2$S ambient for 10 min at 1000 °C before cooling down to inhibit the decomposition of the obtained MoS$_2$ film. Using this condition, the growth of a fully coalesced monolayer MoS$_2$ was achieved in 10-30 mins across the 2" sapphire substrate. Additionally, planar view characterization of the monolayer MoS$_2$ film (in Fig. 1 l,m) was performed with the Thermo Fisher Scientific (TFS) Titan G2 60-300 S/TEM at an accelerating voltage of 80 kV.

MoS$_2$ film transfer on STO nanomembranes
The transfer of the MoS$_2$ film from the growth substrate to the application substrate was accomplished using a PMMA-assisted wet transfer method[34]. Initially, PMMA was spin-coated onto the MoS$_2$ layer on the sapphire substrate and allowed to sit for 24 hours to promote strong PMMA/MoS$_2$ adhesion. The film's edges were then lightly scratched with a razor blade before immersion in a 2 M NaOH solution heated to 90 °C. Due to the hydrophilic nature of sapphire and the hydrophobic properties of MoS$_2$ and PMMA, capillary action guided NaOH to the interface between the substrate and MoS$_2$, effectively detaching the PMMA/MoS$_2$ stack from the sapphire. The separated film was retrieved from the NaOH solution using a clean glass slide and rinsed in three consecutive water baths for 15 minutes each. It was then transferred onto the application substrate, which already contained the STO nanomembrane. Following the transfer, the substrate was baked at 50 °C and then 70 °C for 10 min each to eliminate moisture and strengthen adhesion, creating a pristine interface. Finally, the PMMA was removed by immersing the sample in acetone for one hour, followed by a 30-minute IPA bath to complete the cleaning process.

Fabrication of 2D MoS₂ transistors

To define the channel regions of the MoS_2 transistors in this study, the application substrate, with MoS_2 transferred on top, was first spin-coated with PMMA A6 at 4000 RPM for 45 s, followed by baking at 180 °C, for 90 s. The resist was then patterned using a Raith EBPG5200 e-beam lithography tool and developed in a 1:1 solution of MIBK and IPA for 60 s, followed by an IPA rinse for 45 s. The exposed MoS_2 monolayer was subsequently etched using sulfur hexafluoride (SF_6) RIE at 5 °C, for 30 s. After etching, the sample was cleaned in acetone and IPA to remove the e-beam resist. A second lithography step was conducted to define the source and drain electrodes. The substrate was spin-coated with methyl methacrylate (MMA) EL6 and PMMA A3 at 4000 RPM for 45 seconds, followed by baking at 150 °C and 180 °C, for 90 s each, respectively. E-beam lithography was used again to pattern the source and drain regions, with development in the same 1:1 MIBK/IPA solution and IPA rinse as before. The electrodes were then formed by depositing 40 nm of nickel (Ni) and 30 nm of gold (Au) via e-beam evaporation. Finally, a lift-off process was performed by immersing the sample in acetone for 1 hour, followed by a 30-minute IPA rinse to clean the substrate.

Raman and photoluminescence spectroscopy

For MoS_2, Raman and PL spectra were acquired on a Horiba LabRAM HR Evolution confocal Raman microscope, using a 532 nm laser set to 34 mW, filtered at 1%. The setup included a 100 × objective with a numerical aperture of 0.9 and gratings with 1800 gr mm^{-1} for Raman and 300 gr mm^{-1} for PL.

SEM analysis

The 2D MoS_2 transistors used in this study were examined with SEM on a Zeiss Gemini 500 field emission scanning electron microscope (FESEM) system, operating at an accelerating voltage of 5 kV.

TEM sample preparation of fabricated FET based on 2D MoS₂/3D STO nanomembranes

The TEM sample in Figs. 2d, e and 3i was carefully prepared using the TFS Scios 2 Dual Beam Focused Ion Beam Scanning Electron Microscope. To protect the device's surface during ion beam milling and thinning, a carbon layer was first applied. A cross-section of approximately 2 μm thickness, covering the target area, was then precisely lifted out and transferred in situ to a copper half-grid. Thinning of the lamella was carried out with a Ga ion beam at five sequentially reduced voltages: 30, 16, 8, 5, and 2 kV to minimize potential damage as the sample was made progressively thinner.

STEM characterization of the cross-section of fabricated FET based on 2D MoS₂/3D STO nanomembranes

The TFS Titan G2 60-300 S/TEM was utilized for both STEM and EDS analyses, as illustrated in Figs. 2d, e and 3i. The S/TEM was operated at an accelerating voltage of 300 kV, with a spot size of 6, C_2 aperture of 70 μm, a convergence angle of 25.2 mrad, and a beam current of 0.07 nA. Elemental mapping was conducted in STEM mode using the SuperX EDS system, producing intensity plot images.

TEM sample preparation and STEM characterization of the cross-section of STO/SrO/LAO

The cross-sectional sample of the STO/SrO/LAO membrane was prepared using an TFS Helios NanoLab G4 dual-beam focused ion beam. To protect the sample surface, an initial 50 nm amorphous carbon layer was deposited via sputter coating, followed by additional protective layers of 1 μm each of amorphous carbon and platinum over the region of interest. The focused ion beam was operated at 30 kV with a 2 kV electron beam. A cross-section roughly 1 μm thick was then lifted out and attached to a copper half-grid. The lamella was subsequently thinned using the ion beam at 30 kV and 5 kV, with progressively reduced current to minimize potential sample damage. A TFS F200X STEM equipped with a Super-X EDX spectrometer was used to obtain HAADF images and EDX elemental maps of the STO/SrO/LAO cross-section, as shown in Fig. 1e. The microscope was operated at 200 kV with probe convergence angle of 10.5 mrad and beam current of 50-150 pA.

Second harmonic generation (SHG) measurements

SHG measurements were done using an 800 nm linearly polarized fundamental beam from a regeneratively amplified Spectra-Physics Solstice Ace Ti:sapphire laser system (1 kHz, 100 fs). The incident power was optimized at normal incidence at room temperature to minimize the SHG signal from the SiO_2/Si substrate underneath the $SrTiO_3$ membranes. Temperature-dependent SHG response was measured at a 45-degree incidence and the reflected ppolarized SHG intensity was collected using a photo-multiplier tube via lock-in detection. A Janis 300 gas flow cryostat was used for achieving low temperatures down to 77 K and the data was collected during the heating ramp performed at 5 K/min

Electrical characterization

Electrical characterization of the fabricated devices was performed in a Lake Shore CRX-VF probe station under atmospheric conditions and at 15 K using a Keysight B1500A parameter analyzer.

Data availability

Data on the MoS_2 sample produced in the 2DCC-MIP facility, including growth recipes and characterization data, are available at https://doi.org/10.26207/mc6e-xz31. Other data that generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Code availability

The codes used for plotting the data are available from the corresponding author.

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Author contributions

S.D. conceived the idea and designed the experiments. D.S. fabricated the devices. D.S., H.R., M.D., and P.V. measured the devices. S.C., S.V., and B.J. grew the freestanding $SrTiO_3$ nanomembranes. J.S. and K.A.M. performed the high-resolution (HR) STEM on the as-grown $SrTiO_3$ nanomembranes (Fig. 1e). Z. Z. and Y. S. prepared the cross-sectional TEM sample from a 3D $SrTiO_3$/2D MoS_2 FET stack by FIB, and characterized it using STEM (Fig. 2d), under the guidance of Y.Y.. Z. Z. and Y.Y. performed HR-STEM and analyzed the polarization of $SrTiO_3$ film under contact electrode (Fig. 3 i–l). S.H., A.S., and V.G. performed SHG analysis on $SrTiO_3$ nanomembranes. C.C. and J.M.R. grew the large-area monolayer MoS_2 films. S.S.R. helped with data analysis. All authors contributed to the preparation of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information