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Monolithic and heterogeneous three-dimensional integration of two-dimensional materials with high-density vias

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Monolithic three-dimensional (M3D) integration is being increasingly adopted by the semiconductor industry as an alternative to traditional through-silicon via technology as a way to increase the density of stacked, heterogenous electronic components. M3D integration can also provide transistor-level partitioning and material heterogeneity. However, there are few large-area demonstrations of M3D integration using non-silicon materials. Here, we report heterogeneous M3D integration of two-dimensional materials using a dense inter-via structure with an interconnect (I/O) density of 62,500 I/O per mm^2. Our M3D stack consists of graphene-based chemisensors in tier 2 and molybdenum disulfide (MoS_2) memtransistor-based programmable circuits in tier 1, with more than 500 devices in each tier. Our process allows the physical proximity between sensors and computing elements to be reduced to 50 nm, providing reduced latency in near-sensor computing applications. Our manufacturing process also stays below 200 °C and is thus compatible with back-end-of-line integration.

Three-dimensional (3D) integration[1,2] can be used to increase transistor count per unit area and create processors with increased computational power[3]. It can also be used to enhance chip functionalities beyond the traditional approach of increasing transistor density. Various technologies—such as analogue devices, radiofrequency devices, sensors, memories and microelectromechanical systems—can be integrated alongside digital components in this manner[4].

There are various approaches to 3D integration. Through-silicon via (TSV) stacking offers benefits such as enhanced bandwidth and reduced interconnect lengths. TSV-based 3D integrated circuits (ICs) were originally pioneered by companies such as IBM, Samsung and Micron, and primarily concentrated on flash memories and dynamic random-access memory stacks[5–8], while other commercial providers used TSV electrodes in 3D-stacked complementary metal–oxide–semiconductor (CMOS) image sensors[9,10]. Recently, technologies such as Intel's Foveros have made it possible to create dense TSVs with a standard pitch of 50 µm, resulting in an interconnect (I/O) density of up to 400 I/O per mm^2 (ref. 11). The I/O metric is a critical performance benchmark for 3D ICs. To further increase I/O density, a transition from macro- to micro-3D heterogeneous integration via hybrid bonding is needed. This technology facilitates direct copper-to-copper pad connections with a TSV pitch of less than 10 µm, achieving 10,000 I/O per mm^2 (refs. 12,13).

Monolithic 3D (M3D) integration can achieve vias with pitches of less than 1 µm for even higher I/O density[14,15]. In M3D integration,

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functionally diverse layers of devices are sequentially stacked on the same wafer to enhance routability and design flexibility while reducing inter-tier signal delay. Thus, the approach enables transistor-level heterogeneity; for example, stacking silicon p-type field-effect transistors (p-FETs) on gallium nitride (GaN) n-type FETs (n-FETs) allows for efficient power delivery and radiofrequency solutions[16]. Similarly, integration of high-performance germanium p-FETs with Si n-FETs can advance CMOS logic applications[17]. Two-dimensional (2D) materials have been integrated at the CMOS back-end for memristive applications[18,19]. Silicon-free M3D integration was initially achieved by stacking carbon nanotube transistors and resistive memory devices[20]. However, more recent efforts have involved M3D integration of transistors made of 2D transition metal dichalcogenides such as molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2)[21–23].

In this Article, we report M3D integration of graphene-based chemitransistors with monolayer MoS_2-based memtransistors for near-sensor computing. The M3D stack includes more than 500 MoS_2 memtransistors and 500 graphene chemitransistors on each tier, which are used for data processing and acquisition, respectively, with a vertical separation between processors and sensors of less than 50 nm. By exclusively using 2D materials, we demonstrate inter-tier vias measuring $3 \times 3\ \mu m^2$ with a pitch of 4 µm, allowing us to achieve an interconnect density of 62,500 I/O per mm^2. The entire stack is fabricated at temperatures below 200 °C, making it compatible with standard back-end-of-line (BEOL) integration processes. Table 1 highlights the advances achieved in via pitch, I/O density and BEOL compatibility compared to previous technologies.

We selected monolayer MoS_2 and graphene for our demonstration because both are among the most mature 2D materials and can be grown at the wafer-scale[24]. Furthermore, MoS_2 transistors have exhibited excellent device performance and can meet the standards for advanced technology nodes[25–29], as well as enable various neuromorphic and bio-inspired applications[30–36]. Graphene-based sensors offer versatility in detecting gases, biomolecules and various chemical species due to their electrochemically inert basal plane[37–39]. Similarly, the high carrier mobility of graphene and emerging properties in stacked graphene layers open new possibilities for expanding the functionalities of 3D ICs[40,41].

Heterogeneous M3D chip using 2D materials

M3D integration of monolayer MoS_2 memtransistors and graphene chemitransistors necessitates large-area synthesis of these materials. A metal-organic chemical vapour deposition (MOCVD) technique was used to grow monolayer MoS_2 on a 5 cm (2 inch) sapphire substrate in a cold-wall horizontal reactor (see the Methods section for details), whereas graphene was commercially procured on copper (Cu) foil. Figure 1a,b show an optical image of the as-grown MoS_2 film and its Raman spectra obtained using a 532 nm laser, respectively. The in-plane E^1_{2g} (387 cm^{-1}) and out-of-plane A_{1g} (404 cm^{-1}) Raman active vibrational modes have a separation of 17 cm^{-1}, confirming the monolayer nature of the MoS_2 film. Similarly, Fig. 1c,d show an optical image of the graphene on Cu foil and its Raman spectra, respectively. The distinct Raman peaks at around 1,583 and 2,674 cm^{-1}, corresponding to the G band and 2D band, respectively, support the presence of monolayer graphene.

To construct the heterogeneous M3D stack, we selected a commercially available substrate composed of 285 nm SiO_2 on p^{++}-Si. However, it should be noted that any other substrate compatible with our fabrication process flow could also be used. The monolayer-MoS_2-memtransistor-based computational circuits were allocated to tier 1 and the graphene-chemitransistor-based sensing circuits were positioned in tier 2. This arrangement was achieved using a sequential fabrication method, as depicted schematically in Fig. 1e. To start, local back-gate electrodes (2 nm Ti/18 nm Pt) were patterned using e-beam lithography and deposited using e-beam evaporation. This was followed by atomic layer deposition (ALD) of 15 nm Al_2O_3/7 nm HfO_2/3 nm Al_2O_3 to serve as the back-gate dielectric stack for the tier 1 MoS_2 devices. In this structure, the HfO_2 layer with a smaller bandgap functions as a charge trapping layer positioned between two layers of Al_2O_3, which have larger bandgaps. This stack resembles the floating-gate stack found in traditional flash memory devices, enabling non-volatile programming of the channel conductance via charge trapping and detrapping phenomena. Next, access to the back-gate metal electrodes was achieved by etching the floating-gate stack with a boron trichloride (BCl_3) plasma etch. The MOCVD-grown monolayer MoS_2 film was then transferred from the growth substrate to the prefabricated local back-gate islands using a polymethyl methacrylate (PMMA) assisted transfer process. The MoS_2 film was then patterned through e-beam lithography and etched with sulfur hexafluoride (SF_6) to define the channel areas. Subsequently, the source–drain contacts and connections for the comparator circuits were delineated using e-beam lithography, followed by the deposition of 20 nm Au/20 nm Ni/10 nm Au and a subsequent lift-off process.

After finishing the fabrication of the tier 1 devices, a 50 nm layer of Al_2O_3 was deposited to act as the interlayer dielectric (ILD) separating tier 1 and tier 2. A 1 nm-thick seed layer of evaporated aluminium was applied to improve the nucleation of ALD-deposited Al_2O_3 to overcome the inert basal plane of 2D materials. Vias with lengths of 3 µm and widths of 3 µm were patterned into the ILD using e-beam lithography and then opened with a BCl_3 plasma etch. A subsequent lithography step allowed for the deposition of 2 nm Ti/28 nm Ni/30 nm Au to fill these vias. Note that, while we used a via pitch of 4 µm for the work discussed here, our technique permits even smaller via sizes and pitches, highlighting the advantages of M3D integration. Following via formation, graphene was transferred onto the chip from the Cu foil using a PMMA-assisted wet etching transfer method. The graphene devices in tier 2 do not require dedicated back-gate electrodes because they are designed for chemisensing applications in liquid environments, with the liquid effectively functioning as a top-gate. Subsequently, the graphene film was patterned using e-beam lithography and etched with oxygen plasma to define the channel regions. As with the tier 1, this step was followed by the patterning of source–drain contacts and gate electrodes, again using e-beam lithography. A stack of 2 nm Ti/28 nm Ni/30 nm Au was deposited to form these electrodes, with the excess metal being removed in a lift-off process. The final step in the fabrication of the tier 2 graphene chemitransistors involved the deposition of a 70 nm Al_2O_3 capping layer that covered the source–drain contacts to prevent leakage while leaving the gate area exposed to ensure direct contact with any liquid placed onto the chip.

The entire fabrication process occurs within a thermal budget of 180 °C. This temperature limit ensures compatibility with BEOL requirements, allowing for the possible addition of further tiers without compromising the integrity of lower ones. It also facilitates future integration with silicon front-end devices. While the fabrication process may seem straightforward, creating an M3D stack with diverse materials and dense vias requires overcoming substantial lithographic challenges. As more layers are added and structures are miniaturized, precise layer alignment is critical. It is also vital to ensure each layer is electrically isolated by the ILD to avoid leakage. This requires optimization of the fabrication process, including choosing suitable resists, etching recipes and deposition conditions for dielectrics and metals to maintain the structural and electrical integrity of the 3D structure. (Further details on the fabrication process flow are available in the Methods section.)

Figure 2a shows an optical image of a densely packed array of M3D-integrated two-tier cells based on monolayer MoS_2 memtransistors and graphene chemitransistors. The enlarged scanning electron microscopy (SEM) images shown in Fig. 2b,c reveal that each cell in the array contains four devices, namely two graphene chemitransistors located above two MoS_2 memtransistors. These two graphene chemitransistors form a chemisensor, while the two MoS_2 memtransistors

Table 1 | A comparison of different technologies based on inventor, materials used, via pitch (μm), I/O per mm², application and BEOL compatibility

Inventor	Material	Via pitch (μm)	I/O per mm²	Application	Integration type	Notable feature	Integration technique	BEOL compatibility	Reference
Samsung	Si	4	62,500	No	Die-to-wafer	Reliable, void-free vias High alignment accuracy	Hybrid copper bonding	Compatible	59
IBM	Si	40	625	Yes	Chip-to-interposer	Optimization on fine-pitch micro bumps	Cu-pillar micro-bump solder joint	Compatible	60
Intel	Si	10	10,000	No	Die-to-die	Reduced parasitic capacitance and higher interconnect density	Hybrid bonding	Not mentioned	61
IMEC	Si	1	1,000,000	No	Wafer-to-wafer	Low resistance Void-free bonding	Hybrid bonding (SiCN and Cu)	Compatible	62
Silicon Austria Laboratories	Si	10	10,000	No	Die-to-die	Shorter processing times Lower bonding temperatures	Bump-less Cu bonding	Compatible	63
Institute of Microelectronics (IME)	Si	20	2,500	No	Chip-to-wafer	High throughput and accuracy	Cu micro-pillar array	Compatible	64
UCLA	Si	7	20,400	No	Die-to-wafer	High overlay accuracy Low resistance	Cu–Cu thermal compression bonding	Compatible	65
TSMC	Si	24	1,740	High-performance computing	Chip-to-interposer	Low resistance High-density IPD	CoWoS–R⁺	Compatible	66
Hitachi	Si	20	2,500	No	Chip-to-wafer	High thermal stability chemical mechanical polishing compatibility	Hybrid bonding (polyimide and Cu)	Compatible	67
Intel	Ge/Si	–	–	No	Bottom-up fabrication	Monolithic integration	Layer transfer	Not mentioned	17
Intel	GaN/Si	–	–	Radiofrequency	Bottom-up fabrication	Monolithic integration	Layer transfer	Compatible	16
MIT and Stanford	CNT and Si	2	250,000	Gas sensing and classification	Bottom-up fabrication	Monolithic integration	Layer transfer	Compatible	20
KAUST, Tsinghua University and Institute of Micro and Nanotechnology	h-BN and Si	7	20,400	Memristive application	Bottom-up fabrication	Monolithic integration	Layer transfer	Compatible	18
MIT, Washington University in St. Louis and Yonsei University	MoS_2, WSe_2 and h-BN	–	–	AI processing	Bottom-up fabrication	Monolithic integration	Layer transfer	Compatible	22
Penn State	MoS_2/WSe_2	250	16	No	Bottom-up fabrication	Monolithic integration	Layer transfer	Compatible	21
Penn State	**MoS_2/ graphene**	**4**	**62,500**	**Near sensing computing**	**Bottom-up fabrication**	**Monolithic integration**	**Layer transfer**	**Compatible**	**This Work**

The bold font highlights features of our work on M3D integration.

constitute a comparator circuit. The chemisensors in tier 2 are connected by 3 × 3 μm² vias to the comparators in tier 1. The SEM images also show a via separation of 1 μm and thus a pitch of 4 μm between the cells. Extended Data Fig. 1 shows a schematic of the M3D IC for near-sensor compute applications. Figure 2d,e show cross-sectional images at different magnifications, obtained using scanning transmission electron microscopy (STEM) in high-angle annular dark-field (HAADF) mode, taken at the location marked with the white dashed line in Fig. 2b. The presence of the Ti/Pt gate electrode, $Al_2O_3/HfO_2/Al_2O_3$ floating-gate stack, MoS_2 channel, tier 1 source–drain contacts, Al_2O_3 ILD, graphene channel and Al_2O_3 capping layer are indicated. Figure 2f displays the energy dispersive X-ray spectroscopy (EDS) elemental mapping of the area highlighted by the light orange dashed line in the magnified view shown in the rightmost HAADF image of Fig. 2e. The

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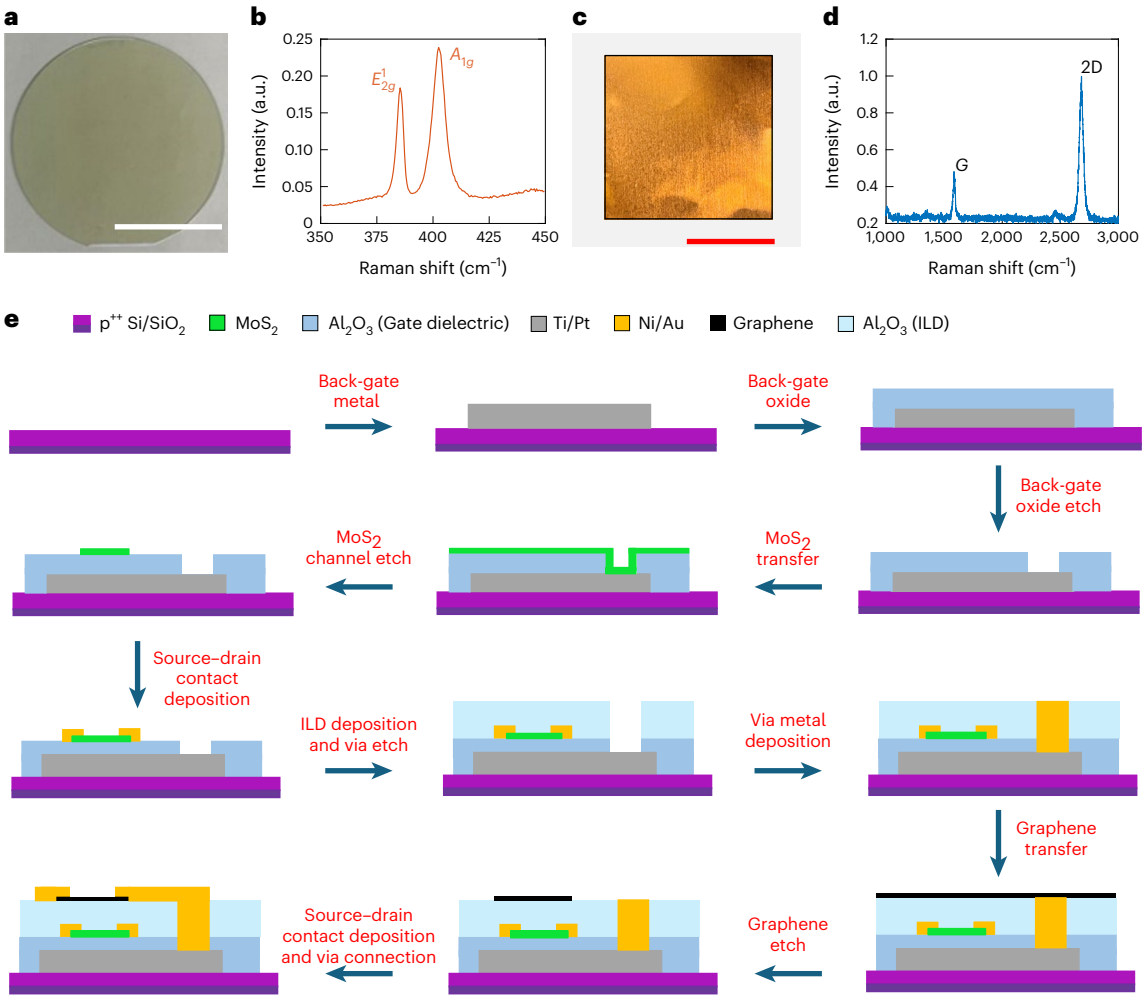

Fig. 1 | Characterization of 2D materials and fabrication process flow for M3D integration. a, Optical image of a 2 inch sapphire wafer with MOCVD-grown MoS_2. Scale bar, 2.5 cm (1 inch) **b**, The corresponding Raman spectrum with the characteristic E^1_{2g} peak at 387 cm^{-1} and A_{1g} peak at 404 cm^{-1}. **c**, Optical image of commercially purchased monolayer graphene film on a copper substrate. Scale bar, 40 mm. **d**, The corresponding Raman spectra obtained using a 532 nm laser. **e**, Fabrication process flow of the 3D monolithic and heterogeneous integration of monolayer-MoS_2- and graphene-based devices.

most notable achievement showcased by these TEM images show the precise placement and dense integration of the scaled vias. Extended Data Fig. 2 shows atomic force microscopy (AFM) images after the fabrication of tier 1 MoS_2 devices, post-ILD deposition and after via formation and fabrication of tier 2 graphene devices. Note that the topographic features are preserved after each fabrication step. Furthermore, the surface roughness remained less than 1 nm throughout the fabrication process. This clearly shows that via fabrication does not introduce variations in topography despite the etching and deposition processes involved. Also note that we have not implemented any surface planarization in this work. Although chemical mechanical polishing, a standard step in semiconductor fabrication, will probably be adopted for M3D integration when stacking many tiers, it was found to be unnecessary for the two-tier integration demonstrated here.

MoS_2 memtransistors and comparator circuit

In our M3D IC, tier 1 is composed of monolayer MoS_2 memtransistors that serve as the primary computing elements. These devices are used for the construction of comparator circuits responsible for processing chemical signals detected by the graphene-based chemisensors in tier 2. Figure 3a shows the transfer characteristics, that is, drain current (I_{DS}) plotted against the back-gate voltage (V_{BG}), at a constant drain voltage, V_{DS}, of 1 V for 50 MoS_2 memtransistors. Here, all MoS_2 memtransistors have a channel length (L_{CH}) and width (W_{CH}) of 500 nm and 1 µm, respectively. Figure 3b–d, respectively, show the distribution of field-effect mobility (μ_{FE}) extracted from peak transconductance, subthreshold slope (*SS*) extracted for three orders of magnitude change in I_{DS} and threshold voltage (V_{TH}) extracted using the iso-current method at 100 nA µm^{-1} for the 50 devices. The median values for μ_{FE}, *SS* and V_{TH} were found to be ~3.3 cm^2 V^{-1} s^{-1}, 150 mV dec^{-1} and 0.2 V, respectively. The median μ_{FE} value here is lower than that of exfoliated flakes[42,43], which is expected since MOCVD-grown MoS_2 generally shows smaller grain sizes with more impurities and defects[44]. Although we have previously achieved higher μ_{FE} values through thorough optimization of growth and device design[24,45,46], the focus of our current study was not solely on enhancing the individual device performance. The *SS* was also higher than the ideal value of ~60 mV dec^{-1} owing to the use of a thicker oxide stack and the presence of non-idealities such as interface traps. By using high-*k* dielectric materials and a thinner stack, it is possible to improve *SS*. Similarly, V_{TH} can be engineered through careful selection of the dielectric interface and metal gate work function. Extended Data Fig. 3 shows the output characteristics of a representative memtransistor with the ON-current reaching as high as 70 µA µm^{-1} for a V_{DS} of 5 V. The lower ON-current values can be attributed to the higher contact resistance, R_C, of 7 kΩ µm, associated with Ni contacts to MoS_2. Extended Data Fig. 4 shows the full R_C extraction using a transmission

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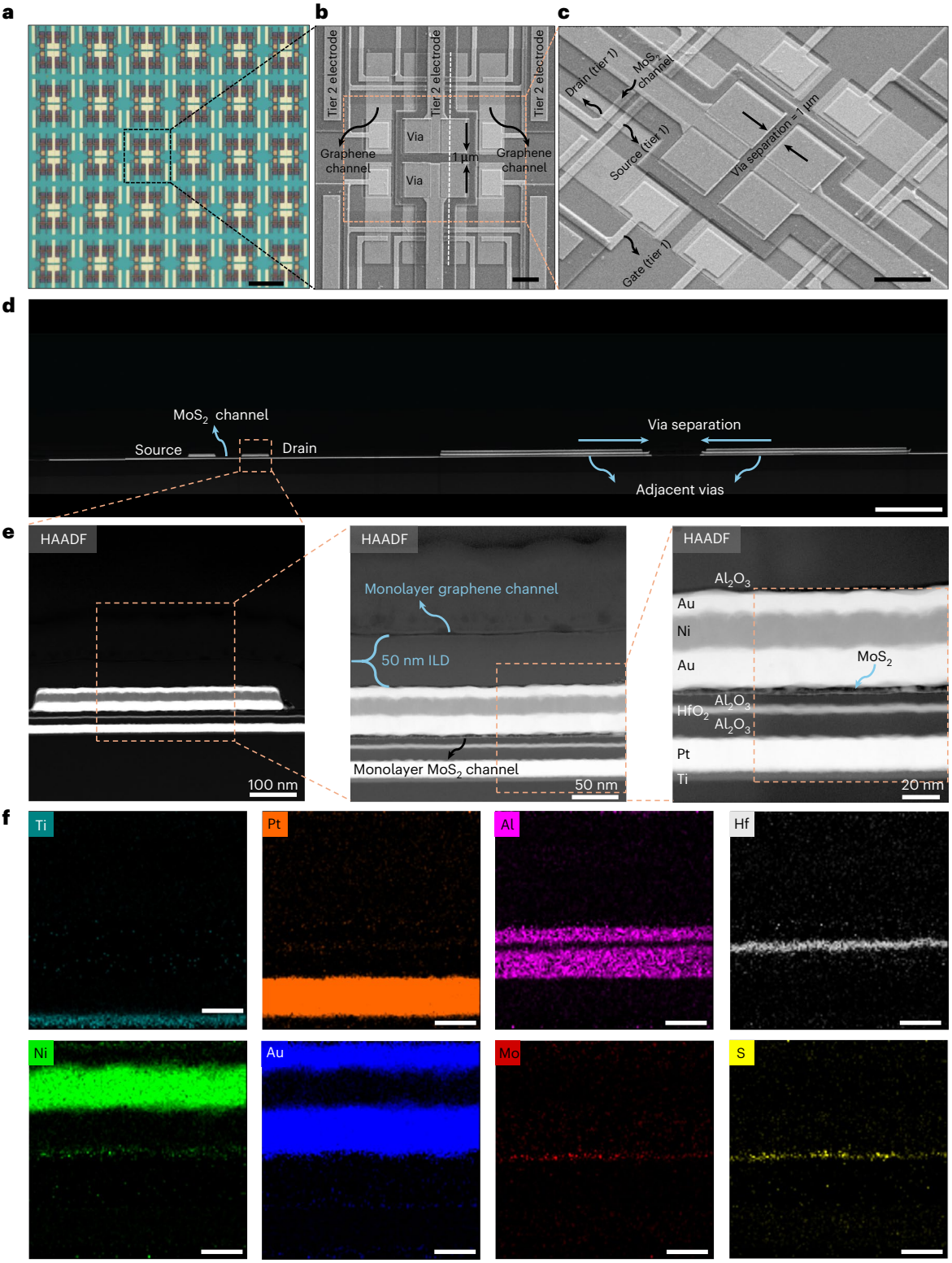

Fig. 2 | Monolithic and heterogeneous 3D ICs. a, Optical image of a densely packed array of M3D-integrated two-tier cells based on monolayer MoS_2 and graphene. Scale bar, 25 µm. **b**, Enlarged SEM image showing that each cell in the array contains four devices, including two graphene chemitransistors above two MoS_2 memtransistors. Scale bar, 3 µm. **c**, An angled SEM image. Notably, the via width and pitch achieved in this work are 3 and 4 µm, respectively. Scale bar, 3 µm. **d**, Cross-sectional STEM–HAADF image. Scale bar, 1 µm. **e**, Enlarged version of the HAADF images taken at the location marked with light orange dashed line, showing the entire M3D stack involving both MoS_2 and graphene channels with a separation of 50 nm. **f**, Enlarged version of EDS mass percentage elemental mapping showing the MoS_2 memtransistor and its floating-gate stack. Scale bars are 20 nm.

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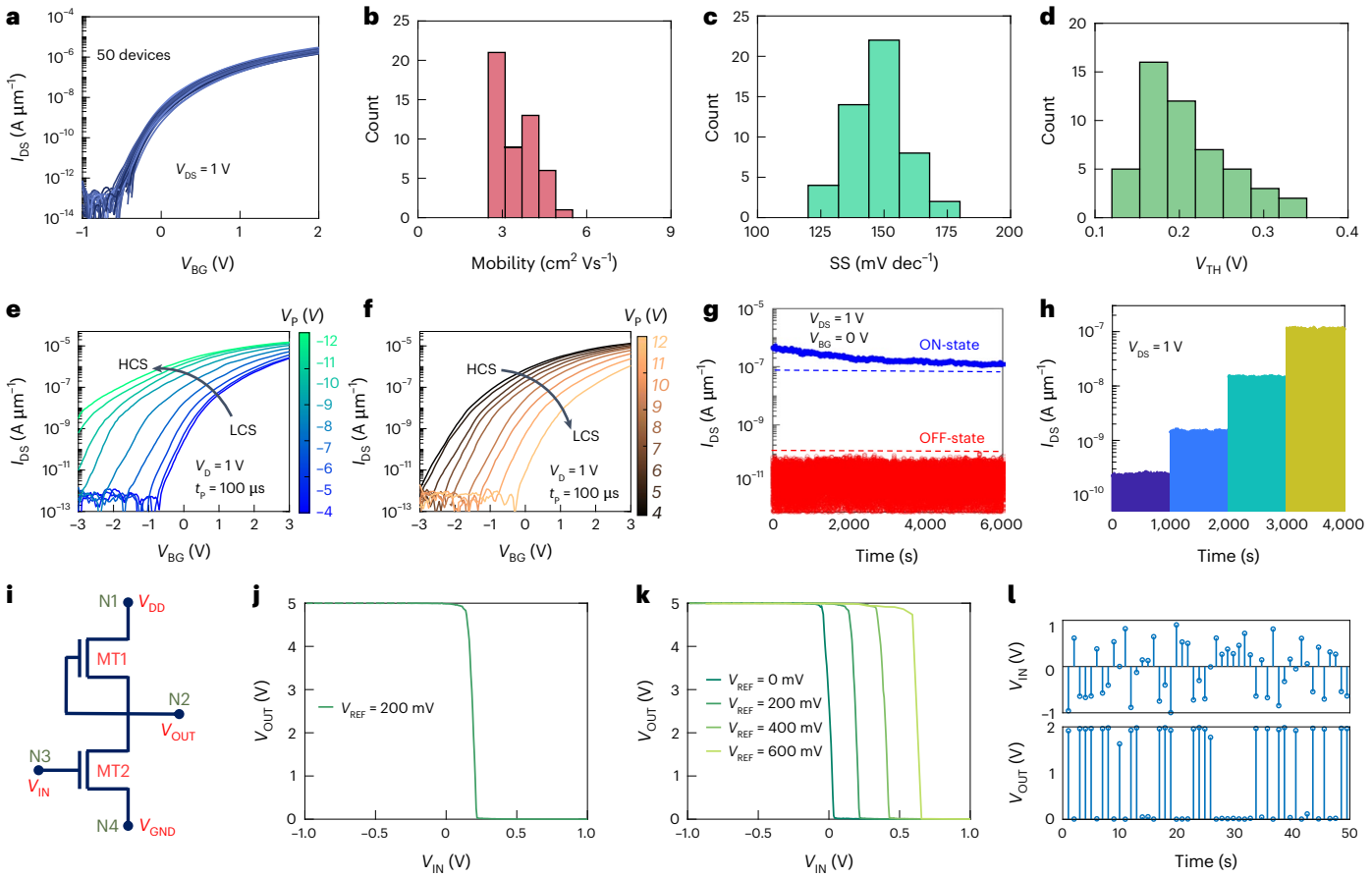

Fig. 3 | Characterization of MoS_2 memtransistors in tier 1. a, Transfer characteristics, that is, source-to-drain current, I_{DS} versus back-gate voltage, V_{BG}, taken at a constant drain voltage, V_{DS}, of 1 V, for 50 MoS_2 memtransistors with a L_{CH} and W_{CH} of 1 μm. **b**–**d**, Histograms showing the μ_{FE} (**b**), *SS* (**c**) and V_{TH} (**d**) for these 50 devices. **e**,**f**, Transfer characteristics of a representative memtransistor after programming or erasing with positive (**e**) and negative (**f**) voltage pulses of varying magnitudes for 100 μs each. **g**, Non-volatile retention for high and low conductance states measured using a V_{BG} of 0 V and a V_{DS} of 1 V for 6,000 s. **h**, Analogue programming and retention for four distinct conductance states. **i**, Circuit diagrams for a comparator consisting of two MoS_2 memtransistors (MT1 and MT2). **j**, Transfer curve for the comparator, that is, the output voltage, V_{OUT}, as a function of the input voltage, V_{IN}. Switching occurs at a V_{IN} of 200 mV, which is denoted as the reference voltage, V_{REF}, for the comparator. **k**, Different V_{REF} obtained by programming MT2. **l**, V_{OUT} achieved in response to an arbitrary input waveform for a V_{REF} of 0 V and a V_{DD} of 2 V.

line model geometry. This R_C value is consistent with previous literature on Ni–MoS_2 contacts[46,47]. However, it is much higher than recent reports using bismuth (Bi) and antimony (Sb) as contacts to MoS_2 (refs. 26,48). Nevertheless, integrating these exotic materials into standard fabrication processes poses compatibility challenges. Although enhancing the performance of MoS_2 memtransistors in future M3D ICs is a desirable goal, the current performance level is sufficient for the applications intended in this work.

A key feature of our MoS_2 memtransistors is their programmability, which allows reconfiguration of circuits on the basis of application need. Figure 3e,f shows the transfer characteristics of a representative MoS_2 memtransistor after programming with positive and negative voltage pulses applied to the local back gate, with varying magnitudes ranging from 4 to 12 V and −4 to −12 V, respectively, with the same pulse time for 100 μs each. The resulting shifts in V_{TH} can be attributed to the trapping and detrapping of carriers in the floating-gate stack. Figure 3g illustrates the non-volatile retention for the high and low conductance states measured using a V_{BG} of 0 V and a V_{DS} of 1 V for 6,000 s. The memory ratio (MR) between the two states show minimal degradation from ~4×10^3 to ~10^3. The projected retention before MR decays to 1 was found to be around 1 day on the basis of the experimental fit. Similarly, Fig. 3h shows non-volatile retention characteristics for four distinct analogue conductance states, each for 1,000 s. Extended Data Fig. 5 presents the programming endurance over 1,000 cycles. Although demonstrating longer-term retention and additional endurance cycles would be ideal, the current performance is adequate for numerous edge applications.

Figure 3i shows the circuit diagrams for a comparator consisting of two MoS_2 memtransistors (MT1 and MT2), connected in series. Note that MT1 is made to serve as a depletion load by shorting its gate terminal to its source terminal. Figure 3j shows the transfer curve for the comparator, that is, the output voltage, V_{OUT}, measured at node, N2, as a function of the input voltage, V_{IN}, applied to node N3 (the gate terminal of MT2). For V_{IN} = −1 V, MT2 is in the OFF-state (open circuit), pulling up V_{OUT} to the V_{DD} of 5 V, which is applied to the source terminal of MT1 (node N1). Similarly, for V_{IN} = 1 V, MT2 is in the ON-state (short circuit), pulling down V_{OUT} to the V_{GND} of 0 V, which is applied to the drain terminal of MT2 (node N4). This explains why V_{OUT} switches from 5 to 0 V as V_{in} is swept from −1 to 1 V. This switching occurs at V_{IN} = 200 mV, which is denoted as the reference voltage, V_{REF}, of the comparator. Interestingly, V_{REF} can be adjusted by programming MT2 as shown in Fig. 3k. Extended Data Fig. 6 shows the comparator output for different V_{DD}. Finally, Fig. 3l shows the output of the comparator in response to an arbitrary input waveform for a V_{REF} of 0 V and a V_{DD} of 2 V. It is important to note here that, while the ILD affects the performance of the MoS_2 memtransistors due to n-type surface charge transfer doping from ALD-grown Al_2O_3 (ref. 49), as shown in Extended Data Fig. 7, the functionalities of MoS_2 memtransistor-based circuits are not adversely

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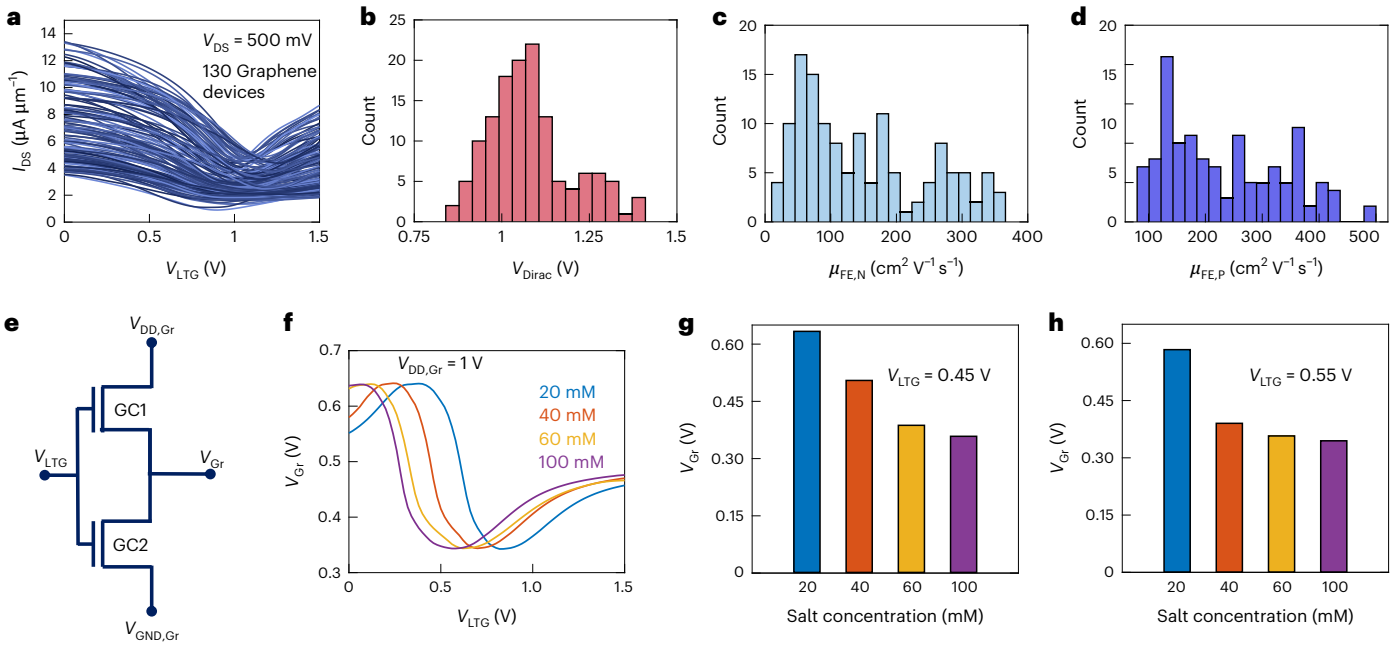

Fig. 4 | Electrical characterization of graphene chemitransistors. a, Transfer characteristics of 130 graphene chemitransistors taken at a V_{DS} of 500 mV. **b**–**d**, Distribution of V_{Dirac} (**b**), $\mu_{FE,N}$ (**c**) and $\mu_{FE,P}$ (**d**) for all 130 graphene chemitransistors. **e**, Schematic diagram of a graphene-based chemisensor consisting of two graphene chemitransistors, GC1 and GC2, connected in series. **f**, V_{Gr} as a function of V_{LTG} with a $V_{DD,Gr}$ of 500 mV under different concentration of NaCl solution (20, 40, 60 and 100 mM). **g**, Monotonic V_{Gr} evolution with increasing NaCl concentration obtained at two different V_{LTG} values of 0.45 and 0.55 V.

affected. For example, the observed shift in V_{TH} is compensated using the programming capability of the floating-gate stack to ensure proper logic levels for the intended applications.

Graphene chemitransistor-based sensing module

Tier 2 of our M3D IC incorporates graphene chemitransistors that are specifically engineered to allow direct application of chemical solutions onto the chip for chemisensing. These solutions play the role as a liquid top-gate for the graphene chemitransistors, due to the formation of an electric double layer at the graphene channel and chemical solution interface. This electric double layer functions as an ultra-thin dielectric layer and is therefore crucial for controlling the conductance of the channel when an electrical bias is applied to the solution[50]. Figure 4a shows the transfer characteristics, that is, I_{DS} plotted as a function of the liquid top-gate voltage (V_{LTG}), for 130 graphene chemitransistors in aqueous solution at a constant V_{DS} of 500 mV. The observed transfer curves are quintessential to graphene with the global minima referred to as the Dirac points. Additionally, the graphene chemitransistors exhibit ambipolar transport, that is, they demonstrate both electron and hole conduction, which is a direct consequence of graphene being a zero-bandgap semiconductor. Figure 4b–d, respectively, depict the distribution of the Dirac voltage (V_{Dirac}), that is, the applied V_{LTG} that results in a minimum I_{DS}, and the electron and hole mobility values ($\mu_{FE,N}$ and $\mu_{FE,P}$) extracted from their respective peak transconductances for these 130 graphene chemitransistors. The median values for V_{Dirac}, $\mu_{FE,N}$ and $\mu_{FE,P}$ were found to be 1.1 V, 126 cm^2 V^{-1} s^{-1} and 219 cm^2 V^{-1} s^{-1}, respectively. The device-to-device variation can be ascribed to imperfections introduced in the graphene during growth, transfer and/or chemitransistor fabrication processes[51–53]. Although such variation is generally undesirable for most applications, here it presents an opportunity for designing a chemisensor, as discussed in the following section.

Each chemisensor in our M3D IC comprises two graphene chemitransistors (GC1 and GC2) connected in series as shown using the circuit schematic in Fig. 4e. The output from the chemisensor is obtained at node N2. Figure 4f shows the output voltage (V_{Gr}) as a function of V_{LTG} with a supply voltage ($V_{DD,Gr}$) of 1 V when deionized (DI) water with different concentrations of NaCl is used as the liquid solution. The distinct shapes of these response curves directly arise from the device-to-device variation. Without this variation, the output of the chemisensor would be a horizontal straight line with a V_{Gr} of 500 mV irrespective of the chemical solution. Nevertheless, the V_{Gr} obtained at V_{LTG} values of 0.45 and 0.55 V show monotonic changes with the increasing concentration of NaCl in DI water, as illustrated using the bar plots in Fig. 4g. This confirms the functioning of the graphene-based circuit as a chemisensor, offering the ability to adjust the V_{LTG} for optimal sensitivity.

Additionally, it should be noted that the characteristics of the voltage transfer curve can vary depending on the position of the Dirac points in individual graphene chemitransistors, as illustrated in Extended Data Fig. 8. While the exact shape of these curves is not critical for the application demonstrated here, consistent performance is crucial for future practical use. This will require further development of graphene devices. Initially, minimizing device-to-device variation through optimized CVD growth conditions and improved transfer processes is key. Subsequently, we can reintroduce variation between two graphene chemitransistors by utilising the memristive properties of graphene, as detailed in our previous work[54]. Although our current study intentionally uses device-to-device variation to achieve the desired curve shape, our aim is to control this variation to guarantee reproducibility.

M3D chip for near-sensor computing applications

Near-sensor computing is a transformative approach that allows processing of data close to where it is generated, as opposed to transmitting it over long distances to central processing units: that is, cloud-based computing. Such a shift enables real-time analysis of data, leading to lower latency and faster decision making, and contributes to better bandwidth, accuracy and energy efficiency. As a result, this proximity-driven approach has far-reaching implications in many applications, with extra consideration to the field of chemical sensing. For example, in environmental monitoring and

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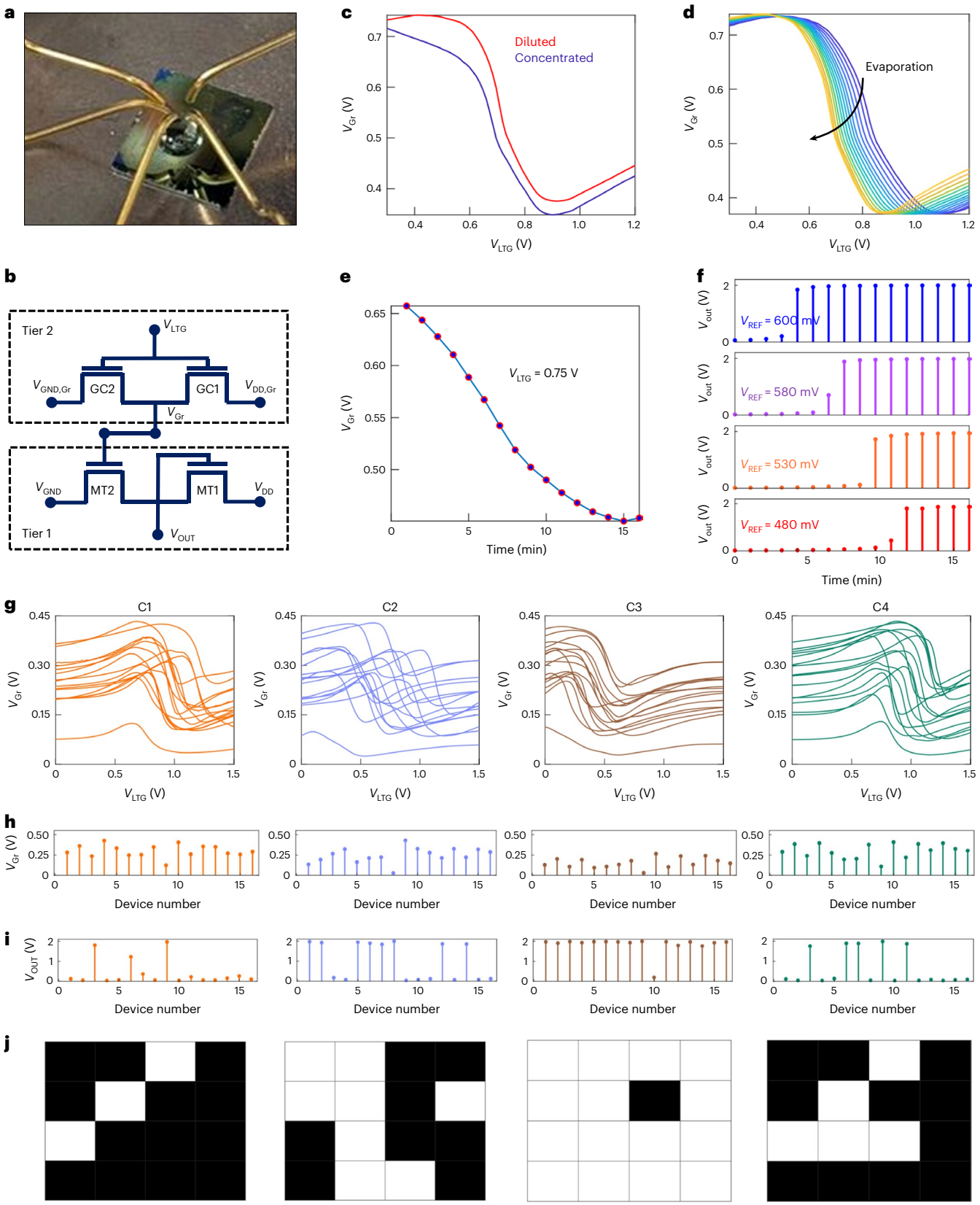

Fig. 5 | Near-sensor compute using M3D ICs. a, Optical image of the M3D chip with a chemical solution on top. **b**, 3D circuit layout illustrating the connection between a graphene-chemitransistor-based chemical sensor in tier 2 and an MoS_2-memtransistor-based comparator in tier 1, enabled by an inter-tier via. **c**, Transfer curves for the chemisensor in response to two different sugar solutions. **d**, Temporal evolution of the transfer curves for the dilute sugar solution when left to evaporate for 15 min. **e**, V_{Gr} measured at a V_{LTG} of 0.75 V (**e**) and corresponding output from the comparator, V_{OUT} (**f**), with different programmed V_{REF}, as a function of time. **g**,**h**, Transfer curves for 16 chemisensors in response to four different chemicals, C1 to C4 (**g**), and corresponding V_{Gr} extracted at a V_{LTG} of 0.6 V (**h**). **i**,**j**, One-dimensional (**i**) and 2D (**j**) digital code for each chemical obtained using the same circuit architecture shown in **b**.

industrial process control, the ability to detect chemical events or anomalies in real-time enables early warning systems and proactive measures to mitigate potential risks and safety issues. We illustrate this concept by using our M3D IC to detect instances where the concentration of a certain chemical in a solution rises above a set limit, as shown in Fig. 5a.

The near-sensor computing architecture used for the task is illustrated in Fig. 5b. Here, the output node of a graphene-chemitransistor-based chemisensor in tier 2 is connected to the input node of an MoS_2-memtransistor-based comparator circuit in tier 1, as facilitated by an inter-tier via. Figure 5c displays the transfer curves for the chemisensor when exposed to two different sugar solutions created by mixing a sugary beverage with water in ratios of 1:1 (dilute, red curve) and 2:1 (concentrated, blue curve). These curves were recorded immediately after the solutions were applied to the chip. In contrast, Fig. 5d illustrates how these response curves evolve over time as a dilute sugar solution is left to evaporate for 15 min, gradually increasing its sugar concentration. Figure 5e shows V_{Gr} measured at V_{LTG} = 0.75 V as a function of time as the solution evaporates. As can be seen, V_{Gr} starts at ~0.7 V and eventually decreases to 0.5 V after 10 min; this can be read as if the device is shifting from the dilute transfer characteristics shown in Fig. 5c to the more concentrated transfer characteristics due to an increase in sugar concentration. This establishes that V_{Gr} serves as an indication of sugar level in the solution. Note that while we have not functionalized individual graphene chemisensors, functionalized multiplexed arrays[55] can enhance the selectivity and sensitivity of our proposed architecture when incorporating more complex and diverse chemicals.

Next, to develop an alert system, the analogue output voltage (V_{Gr}) needs to be transformed into a digital signal to trigger subsequent modules. This is accomplished using the programmable comparator based on MoS_2 memtransistors depicted in Fig. 5f, for several distinct reference voltages, V_{REF}. Notably, the output logic shifts when the sugar concentration surpasses a specific allowable limit predefined by V_{REF}. As anticipated, the time required to activate the alert system is shorter when the objective is to signal at lower concentrations and longer at higher concentrations. The non-idealities observed in the digitization process can be ascribed to the lower gain of the comparator circuit reducing the abruptness of state transition from 0 V to V_{DD}, that is, digital 0 state to the digital 1 state. The gain can be improved either by using a CMOS inverter, which will require integration of both n- and p-type 2D memtransistors[56], or by cascading multiple depletion-mode inverters. Extended Data Fig. 9 shows the results of digitization using a three-stage-cascaded-inverter-based comparator circuit.

We also show how the 3D IC array shown in Fig. 2a can be exploited for chemical codification by harnessing the response variation among the graphene-based chemisensors. Figure 5g shows the transfer curves for 16 chemisensors in response to four different chemicals, C1 to C4. Figure 5h shows the corresponding V_{Gr} values extracted at V_{LTG} of 0.6 V, which form an analogue code for each chemical. Using the same circuit architecture shown in Fig. 5b, this analogue code can be converted to a one-dimensional or 2D digital code as shown Fig. 5i,j, respectively. The comparator V_{REF} was set to 250 mV. Note that by tuning the read voltage, V_{LTG}, or by using the programmability of the MoS_2-memtransistor-based comparator to adjust V_{REF}, it is possible to generate different codes for the same chemicals, as shown in Extended Data Fig. 10. Nevertheless, while these demonstrations are straightforward, they have broad implications for near-sensor computing, offering potential application in more complex scenarios through the integration of intricate circuits and additional sensors. Also, the physical proximity of less than 50 nm between sensing and computing modules achieved in our heterogeneous M3D chip based on 2D materials is better than state-of-the-art packaging solutions that use distinct technologies in these components.

Conclusions

We have reported a monolithic heterogeneous 3D integration of graphene-based chemitransistors and monolayer-MoS_2-based memtransistors across two tiers using a dense inter-tier via structure with an interconnect density of 62,500 I/O per mm^2. The M3D stack can be fabricated at temperatures below 200 °C, making it compatible with BEOL integration. Notably, the vertical proximity between sensors and computing elements in our stack is 50 nm, surpassing current 3D packaging solutions and potentially reducing computational latency and improving bandwidth.

Methods

Large-area monolayer MoS_2 film growth

Monolayer MoS_2 was deposited on epi-ready 2-inch c-sapphire substrate by MOCVD. An inductively heated graphite susceptor equipped with wafer rotation in a cold-wall horizontal reactor (https://doi.org/10.60551/znh3-mj13) was used to achieve uniform monolayer deposition. Molybdenum hexacarbonyl ($Mo(CO)_6$) and hydrogen sulfide (H_2S) were used as precursors. $Mo(CO)_6$ maintained at 25 °C and 625 torr in a stainless-steel bubbler was used to deliver 4.7×10^{-3} sccm of the metal precursor for the growth, while 400 sccm of H_2S was used for the process. MoS_2 deposition was carried out at 1,000 °C and 50 torr in H_2 ambient, with monolayer growth being achieved in 11 min. Before growth, the substrate was baked at 1,000 °C in H_2 for 10 min. Following growth, the substrate was cooled in H_2S to 300 °C to inhibit the decomposition of the MoS_2 film. More details on the growth process can be found in an earlier study[57].

MoS_2 film transfer to local back-gate island

Film transfer from the growth substrate to the application substrate was performed using a PMMA-assisted wet transfer process[58]. First, the as-grown MoS_2 on the sapphire substrate was spin-coated with PMMA and left to sit for 24 h to ensure good PMMA–MoS_2 adhesion. The corners of the spin-coated film were then scratched using a razor blade and immersed in DI water kept at 50 °C for 2 h. Capillary action caused the DI water to be preferentially drawn into the substrate–MoS_2 interface, owing to the hydrophilic nature of sapphire and hydrophobic nature of MoS_2 and PMMA, separating the PMMA–MoS_2 stack from the sapphire substrate. The separated film was then fished from the DI water using a clean glass slide and rinsed in three separate water baths for 15 min each before finally being transferred onto the application substrate. Subsequently, the substrate was baked at 50 and 70 °C for 15 min each to remove moisture and promote film adhesion, thus ensuring a pristine interface, before the PMMA was removed by immersing the sample in acetone for 1 h and the substrate was cleaned with a subsequent 30 min isopropyl alcohol (IPA) bath.

SEM

SEM of the 2D MoS_2 transistors used in this study was conducted using a Zeiss Gemini 500 field emission SEM system at an accelerating voltage of 5 kV.

TEM sample preparation

The TEM sample depicted in Fig. 2d was prepared using a Thermo Fisher Scientific (TFS) Scios 2 DualBeam focused ion beam SEM instrument. The sample was coated with two carbon layers initially: the first layer, ~0.5 µm thick, was deposited by a 1.6 nA electron beam to protect the surface of MoS_2 and WSe_2 layer from the following Ga ion beam damage during the second layer of carbon deposition. The second layer, approximately 3 µm thick, was deposited using a 0.3 nA Ga ion beam to provide surface protection for later ion beam milling and sample thinning. After this coating process, the sample with a 2-µm-thick cross-section from the region of interest was extracted and transferred in situ to a copper half-grid. Then the lamella was thinned using a Ga ion beam at progressively lower voltages (30, 16, 8, 5 and 2 kV) to minimize ion beam damage as the sample became thinner.

STEM characterization of the cross-section

In this study, the TFS Titan3 G2 60-300 S/TEM was used to perform STEM and EDS analyses, as shown in Fig. 2d–f. To mitigate carbon deposition, a 15 min beam shower was applied in the STEM setting, with a dwell time of 0.05 µs, ×5,000 magnification and 150 µm C2 aperture. The STEM and EDS analyses were operated with an acceleration voltage of 300 kV, featuring a spot size of 6, a C2 aperture of 70 µm and a convergent angle of 25.2 mrad. Elemental mapping was performed using the Super-X EDS system in STEM mode. A series of HAADF-STEM images of the 3D IC were captured at a beam current of 0.07 nA, followed by EDS mappings at a beam current of 0.30 nA. EDS analysis was conducted using Esprit software, incorporating 1/8 Q-Map preprocessing and the series fit deconvolution method. Peak-to-background (P/B) ZAF quantification was used to generate mass percentage (norm.) elemental maps, with a postfilter averaging 9 pixels.

AFM

AFM was used to study the surface morphology, coverage and thickness of the deposited layers. Scanasyst air probe AFM tips with a nominal tip radius of about 2 nm and spring constant of 0.4 N m^{-1} were used for the measurements, and the images were collected using peak-force tapping mode with a peak force of 14 nN and a scan speed of 2 Hz.

Raman spectroscopy

Raman characterization on MoS_2 and graphene was taken using a Horiba LabRAM HR Evolution confocal Raman microscope with a 532 nm laser. The power was 34 mW filtered at 1%. The objective magnification was ×100 with a numerical aperture of 0.9, and the grating had a spacing of 1,800 gr mm^{-1} for Raman.

Electrical characterization

Electrical characterization of the fabricated devices was performed using a semi-automated Formfactor 12000 probe station under atmospheric conditions with a Keysight B1500A parameter analyser. A continuous wave white light source was used for all experiments involving light illumination unless otherwise stated.

Data availability

Data on samples produced in the 2DCC-MIP facility, including growth recipes and characterization data, are available at https://doi.org/10.26207/f095-ha45. Other data that support the finding of this study are available from the corresponding author on reasonable request.

Code availability

The codes used for plotting the data are available from the corresponding authors on reasonable request.

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Author contributions

S.D. conceived the idea and designed the experiments. S.G. and Y.Z. fabricated all the 3D chips. S.D., S.G. and Y.Z. performed the experiments, analysed the data, discussed the results and agreed on their implications. C.C. grew the 2D materials under the supervision of J.M.R. Z.Z. and Y.S. performed the focused ion beam and TEM for the 3D chip under the supervision of Y.Y. T.F.S. performed the SEM of the 3D chip. N.U.S. performed the Raman experiment. A.O. performed the AFM measurements. S.G., Y.Z. and S.D. contributed to the preparation of the paper.

Competing interests

The authors declare no competing interests.

Additional information

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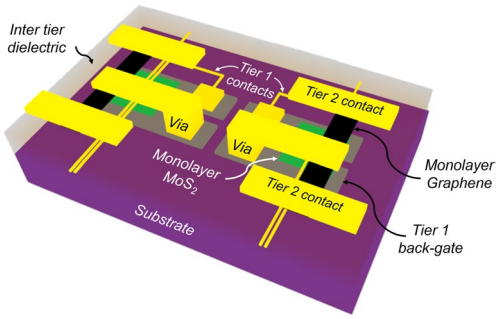

Extended Data Fig. 1 | Monolithic and heterogeneous 3D integration of 2D materials. Schematic showing the M3D stack comprising graphene chemitransistor-based chemisensors in tier 2 connected to MoS_2-memtransistor-based comparator in tier 1 for near sensor computing application.

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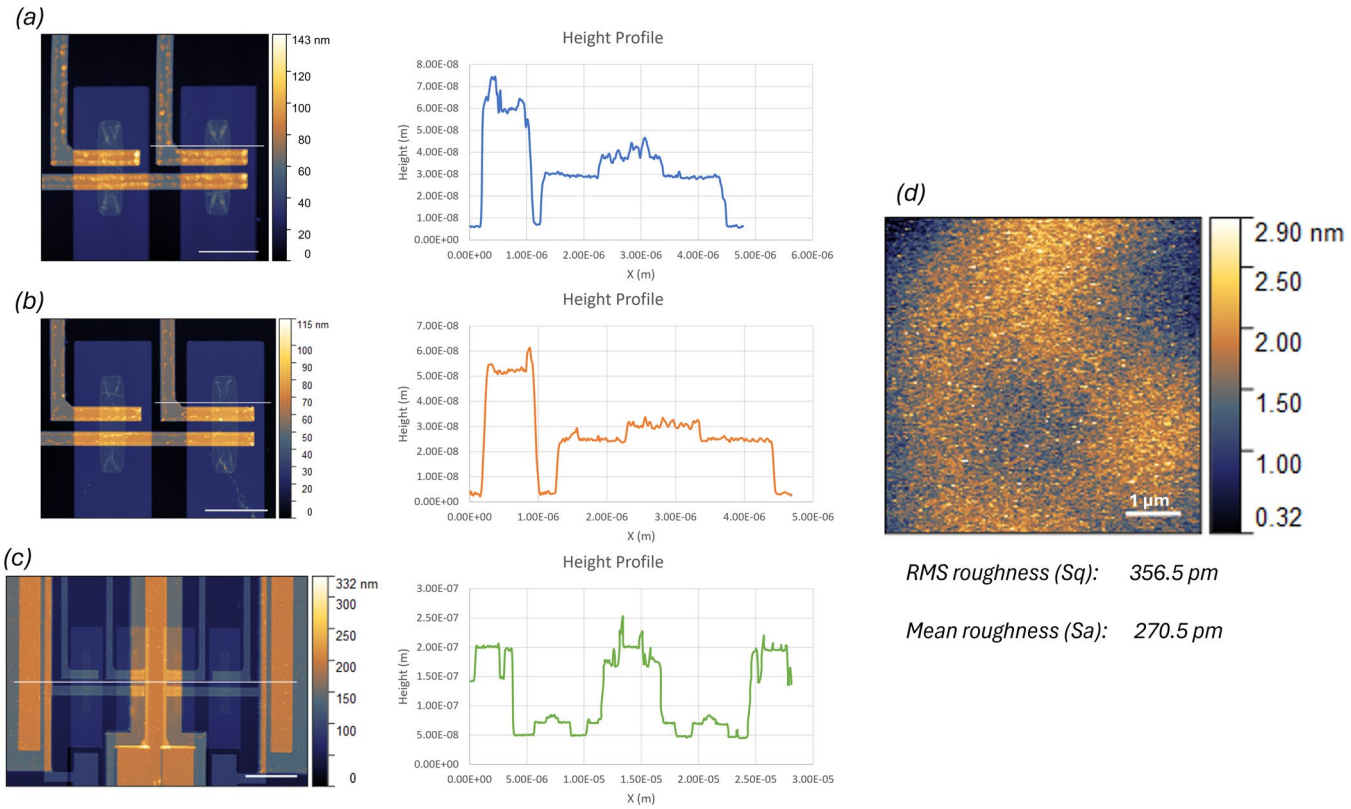

Extended Data Fig. 2 | Surface topography and roughness of M3D IC. Atomic force microscope (AFM) images and height profiles after **(a)** fabrication of tier 1 MoS_2 devices, **(b)** post-ILD deposition, and **(c)** after the via formation and fabrication of tier 2 graphene devices**. (d)** Surface roughness on top of the ILD over 5 µm × 5 µm area showing a mean roughness of 270 pm.

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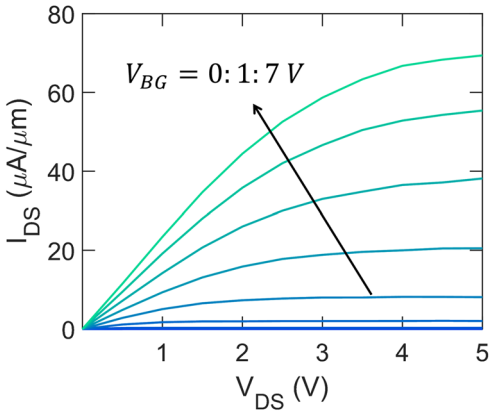

Extended Data Fig. 3 | Output characteristics for an MoS_2 memtransistor. Output characteristics, that is, source-to-drain current, I_{DS}, versus drain voltage, V_{DS}, at different back-gate voltage, V_{BG}, ranging from 0 to 7 V in steps of 1 V, for a representative MoS_2 memtransistor.

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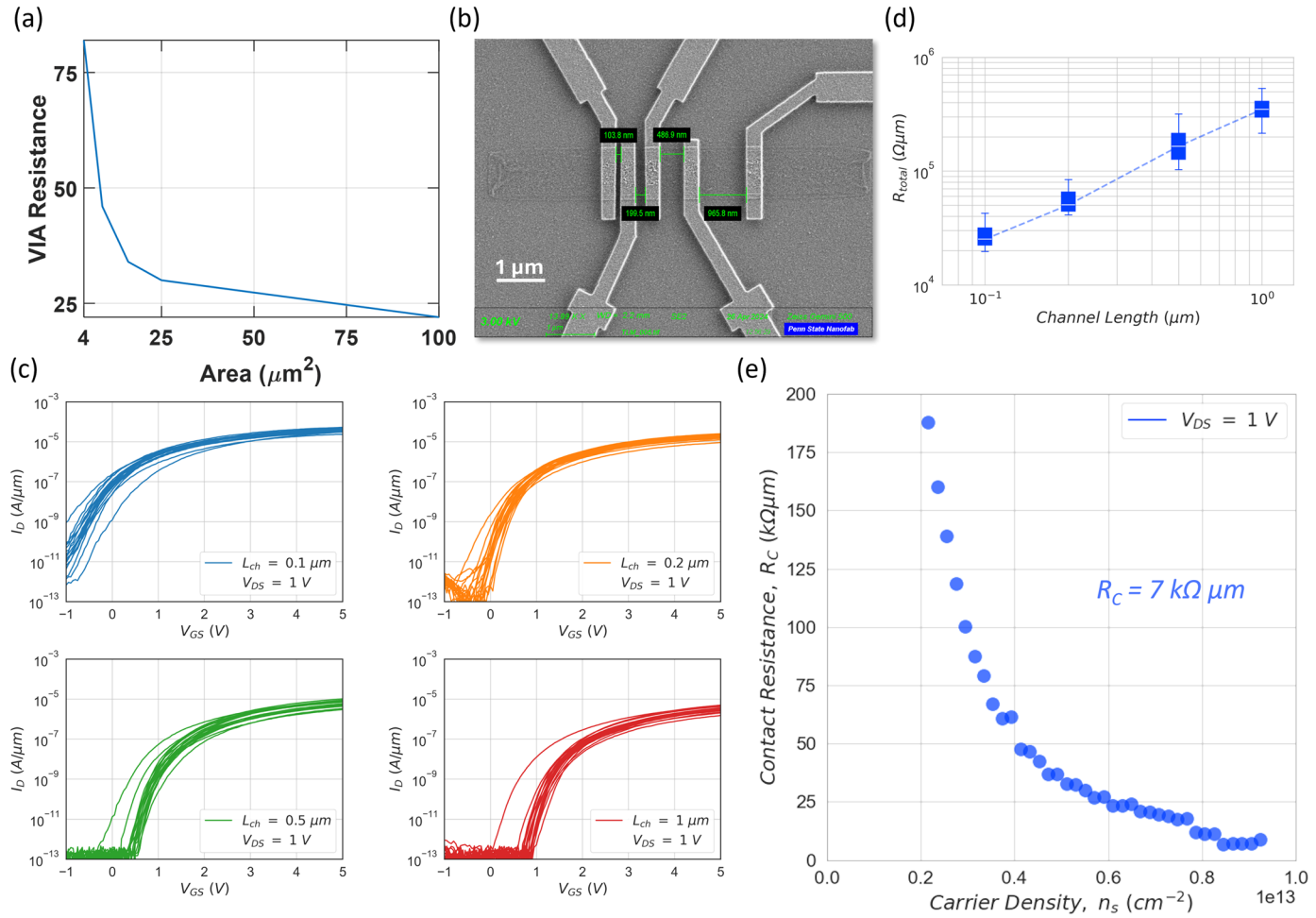

Extended Data Fig. 4 | Extraction of contact resistance for MoS_2 memtransistors. (a) Via resistance as a function of via-area. **(b)** SEM image of the traditional transmission line measurement (TLM) design showing channel lengths of 100 nm, 200 nm, 500 nm, and 1000 nm used to extract the contact resistance. **(c)** Corresponding transfer characteristics for MoS_2 memtransistors obtained from 25 TLM structures. **(d)** Extracted total resistance (R_T) as a function of L_{CH} for an inversion carrier density, $n_s = 5 \times 10^{12}$ cm^{-2}. **(e)** R_C extracted from the y-intercept of the R_T versus L_{CH} plots as a function of n_s. $R_T = R_{CH} + 2R_C$. R_{CH} is proportional to L_{CH} and inversely proportional to the carrier density (n_s), R_C, however, is independent of L_{CH}.

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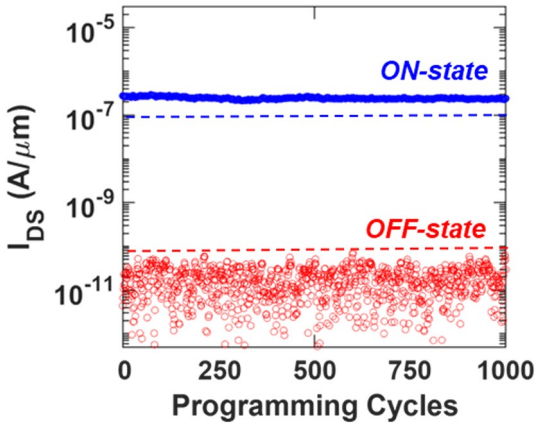

Extended Data Fig. 5 | Endurance measurements for an MoS_2 memtransistor. The read current measured at a V_{BG} of 0 V using a V_{DS} of 1 V every time after programming a representative MoS_2 memtransistor in its high and low conductance states for a total of 1000 cycles. No degradation in the memory ratio (MR) highlights the fact that our MoS_2 memtransistors offer high endurance.

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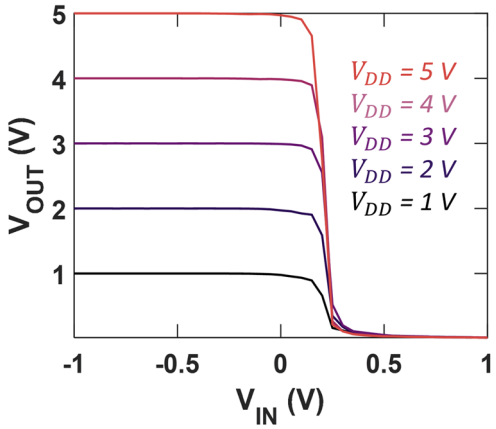

Extended Data Fig. 6 | Supply voltage dependence of an MoS_2 memtransistor based comparator. Transfer characteristics of a representative MoS_2-memtransistor-based comparator for different V_{DD}.

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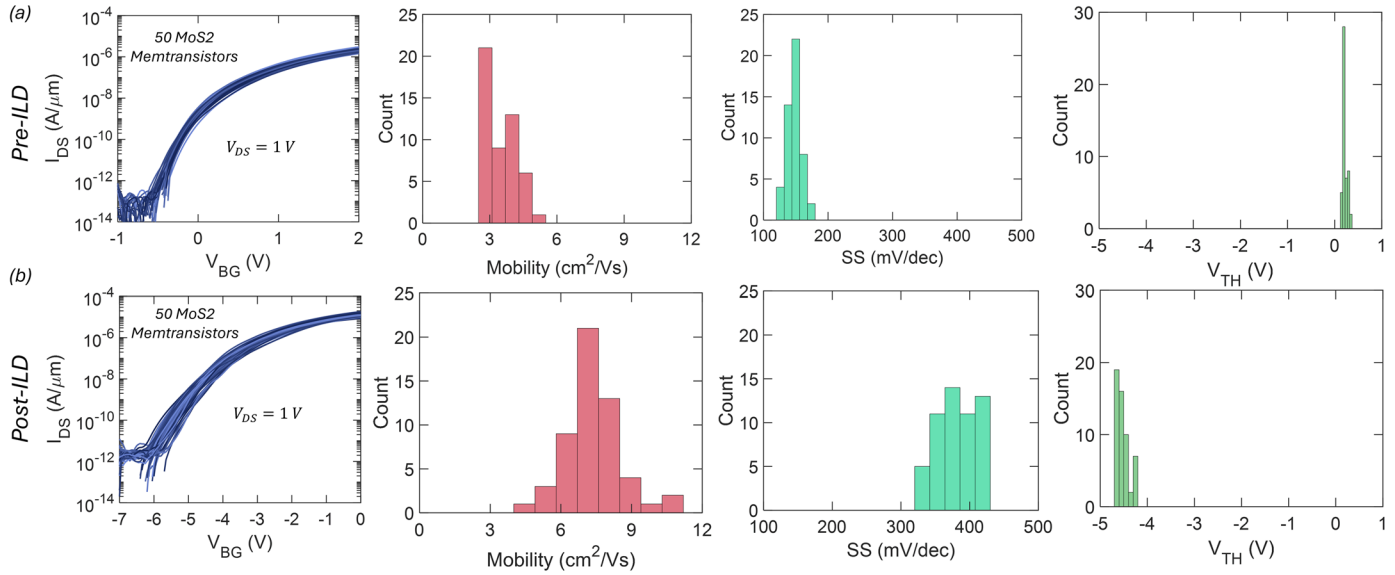

Extended Data Fig. 7 | Impact of ILD on MoS_2 memtransistors. Transfer characteristics and extracted distributions for threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), and subthreshold swing (SS) for 50 MoS_2 memtransistors with an L_{CH} of 500 nm **(a)** before and **(b)** after the ILD deposition. We observed a negative 4.5 V shift in the median V_{TH} value, which can be ascribed to n-type surface charge transfer doping (SCTD) from ALD Al_2O_3. Additionally, there was an improvement in the median μ_{FE} from 3.31 $cm^2V^{-1}s^{-1}$ to 7.27 $cm^2V^{-1}s^{-1}$. However, the median SS experienced a degradation from 150 mV/dec to 375 mV/dec. Despite these changes, it is important to note that the functionalities of MoS_2 memtransistors were not adversely affected. For example, the observed shift in V_{TH} could be compensated using the programming capability of the FG stack to ensure proper logic levels for the intended applications.

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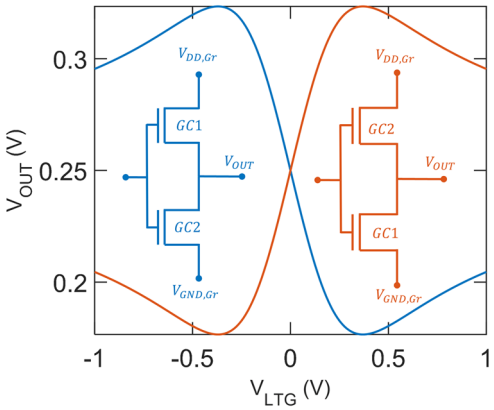

Extended Data Fig. 8 | Impact of variability on chemisensor output. Voltage transfer curves appear complementary when GC1 and GC2 are swapped.

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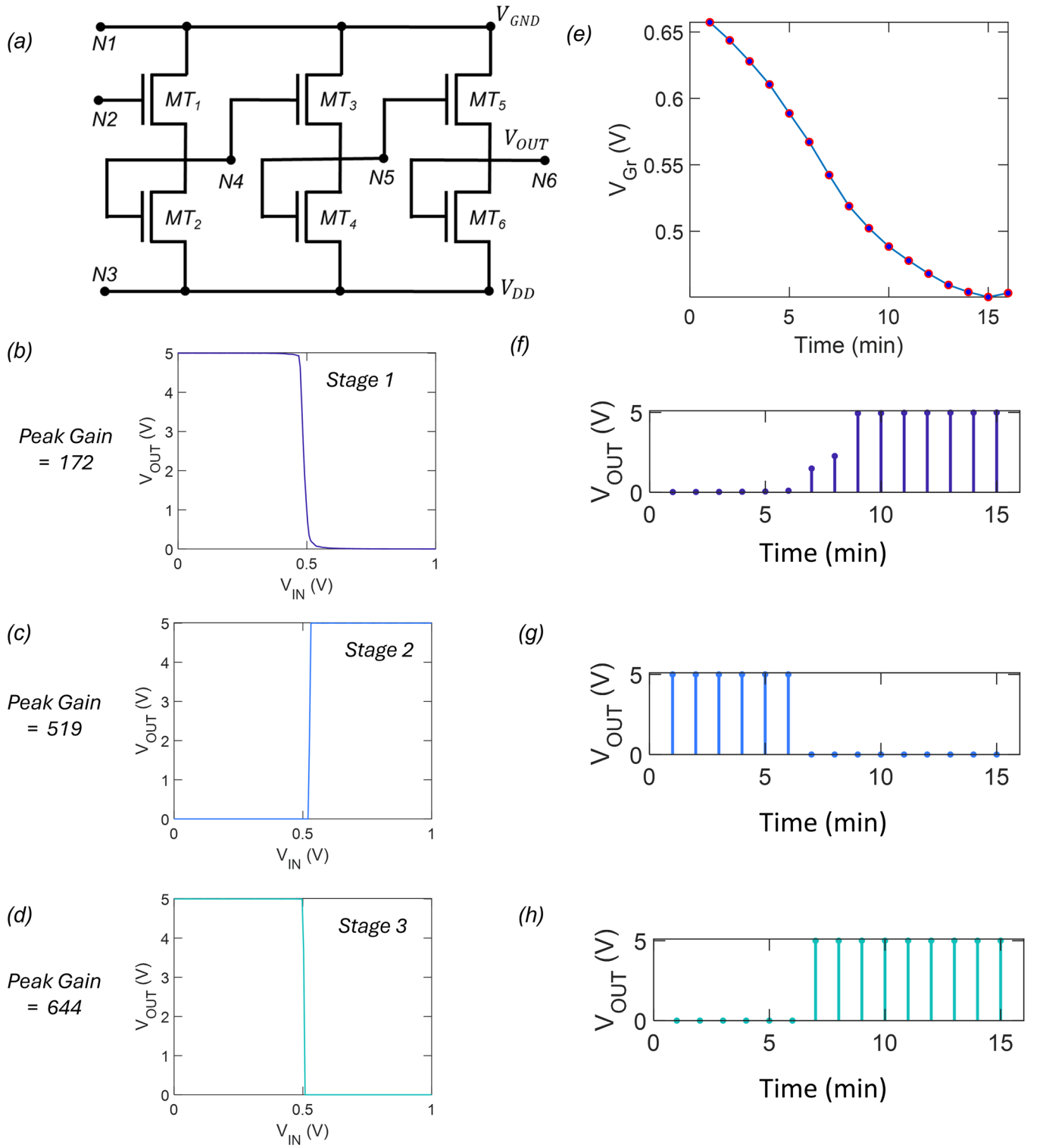

Extended Data Fig. 9 | Digitization using a three-stage cascaded inverter-based comparator. (**a**) Schematic of a three-stage-inverter-based comparator circuit. Voltage transfer characteristics measured at the output of **(b)** stage 1, **(c)** stage 2, and **(d)** stage 3. Clearly, the gain improves from 172 in stage-1 to 519 in stage-2 to 644 in stage-3. **(e)** Analogue output voltage (V_{Gr}) from graphene chemisensor. Results of digitization at the output of **(f)** stage 1, **(g)** stage 2, and **(h)** stage 3. Clearly, cascading a higher number of inverters to construct the comparator allows better digitization.

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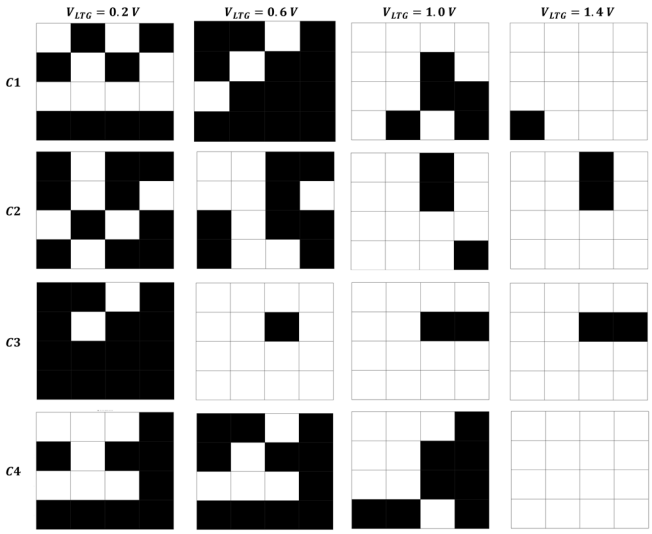

Extended Data Fig. 10 | 2D digital codes using M3D integration platform. Different 2D digital codes generated from the same 4 chemicals (C1, C2, C3, and C4) under different V_{LTG}, ranging from 0.2 V to 1.4 V.