nature nanotechnology

Article

https://doi.org/10.1038/s41565-024-01705-2

Monolithic three-dimensional integration of complementary two-dimensional field-effect transistors

Received: 5 December 2023

Accepted: 27 May 2024

Published online: 23 July 2024

Check for updates

Rahul Pendurthi[1] ✉, Najam U Sakib[1], Muhtasim Ul Karim Sadaf[1], Zhiyu Zhang[1], Yongwen Sun[1], Chen Chen[2], Darsith Jayachandran[1], Aaryan Oberoi[1], Subir Ghosh[1], Shalini Kumari[2,3], Sergei P. Stepanoff[3], Divya Somvanshi[4], Yang Yang[1,5,6], Joan M. Redwing[2,3,5], Douglas E. Wolfe[1,3,6] & Saptarshi Das[1,3,5,7] ✉

The semiconductor industry is transitioning to the 'More Moore' era, driven by the adoption of three-dimensional (3D) integration schemes surpassing the limitations of traditional two-dimensional scaling. Although innovative packaging solutions have made 3D integrated circuits (ICs) commercially viable, the inclusion of through-silicon vias and microbumps brings about increased area overhead and introduces parasitic capacitances that limit overall performance. Monolithic 3D integration (M3D) is regarded as the future of 3D ICs, yet its application faces hurdles in silicon ICs due to restricted thermal processing budgets in upper tiers, which can degrade device performance. To overcome these limitations, emerging materials like carbon nanotubes and two-dimensional semiconductors have been integrated into the back end of silicon ICs. Here we report the M3D integration of complementary WSe_2 FETs, in which n-type FETs are placed in tier 1 and p-type FETs are placed in tier 2. In particular, we achieve dense and scaled integration through 300 nm vias with a pitch of <1 μm, connecting more than 300 devices in tiers 1 and 2. Moreover, we have effectively implemented vertically integrated logic gates, encompassing inverters, NAND gates and NOR gates. Our demonstration highlights the two-dimensional materials' role in advancing M3D integration in complementary metal–oxide–semiconductor circuits.

The relentless pursuit of 'More Moore' through the scaling down of transistor dimensions over six decades has been driven by innovations in device architecture, such as the development of fin field-effect transistor (FET) technology[1], the integration of high-κ dielectrics[2], improved interconnects[3] and advancements in extreme ultraviolet lithography[4]. These innovations have consistently contributed to the increasing density of integrated circuit (IC) components. Interestingly, although device-level scaling has been impressive, it has far outpaced packaging-level advancements. This highlights the significance of three-dimensional (3D) integration—an 'orthogonal scaling' approach that offers a promising strategy for increasing device integration density and effectively addresses the constraints inherent in traditional device dimension scaling[5]. 3D integration presents numerous advantages over traditional planar geometry, including reduced footprint, lower power consumption, higher bandwidth, shorter connection routing and lower parasitic losses from interconnects[6,7]. Additionally,

A full list of affiliations appears at the end of the paper. ✉e-mail: rqp5233@psu.edu; sud70@psu.edu

it enables the heterogeneous stacking of various elements, such as memory and image sensors, in a concept known as 'More than Moore' technology[8,9].

Industrial approaches to 3D integration utilize copper microbumps and through-silicon vias (TSVs) to stack separately fabricated dies[10]. However, TSVs have large footprints, leading to substantial parasitic capacitances and thermal/mechanical stresses[11]. Monolithic 3D (M3D) integration addresses these limitations by sequentially fabricating inter-tier vias on a single die. This approach results in higher vertical interconnect density, shorter wire lengths (enabling higher speed and lower power loss) and transistor-level partitioning[12,13]. M3D integration also allows for the incorporation of non-silicon materials in one or more tiers to enhance performance[14] or enrich functionalities[15]. Recently, M3D integration has incorporated low-dimensional materials such as carbon nanotubes and transition metal dichalcogenides (TMDCs)[16–21]. However, M3D integration with complementary FETs from the same (non-silicon) semiconducting material remains underexplored due to limited progress in developing n-type carbon nanotube FETs and p-type two-dimensional (2D) FETs. Although the demonstrations of 3D stacking of n-type MoS_2 with p-type $MoTe_2$ (ref. 22) and n-type MoS_2 with p-type WSe_2 (ref. 23) mark a step forward in the M3D integration of complementary FETs, its complete potential remains unexplored as both device and via dimensions were relatively large.

In this study, we demonstrate the M3D integration of a two-tier complementary metal–oxide–semiconductor (CMOS) chip based on n- and p-type FETs made from large-area WSe_2 synthesized through a metal–organic chemical vapour deposition (MOCVD) technique. We have also achieved transistor-level partitioning, resulting in the placement of 340 n-type FETs on tier 1 and 340 p-type FETs on tier 2. An important milestone in this research is the demonstration of a densely integrated inter-tier vias measuring 300 nm in width and placed with a pitch of 1 µm, rivalling state-of-the-art packaging solutions[24]. In addition, 3D CMOS circuits including 27 inverters, 12 NAND gates and 12 NOR gates have been successfully realized. Furthermore, the M3D CMOS stack was manufactured at temperatures not exceeding 200 °C, making it compatible for integration at the back end of line for hybrid 2D/Si technologies[25].

Synthesis of WSe_2 films and enabling complementary 2D FETs

Figure 1a shows the optical image of an array consisting of M3D-integrated, two-tier CMOS ICs based on WSe_2 FETs. Each cell in the array (Fig. 1b) contains four devices, in which two p-FET WSe_2 FETs are positioned directly above two n-FET WSe_2 FETs. Figure 1c shows an angled, false-coloured scanning electron microscopy (SEM) image of a two-stage CMOS inverter circuit. In this configuration, 300 nm vias are placed within 1 µm of each other to form the series connection between the tier-1 n-FET and tier-2 p-FET devices, highlighting the dense via integration capabilities achieved in this work. Figure 1d,e shows the schematic and corresponding false-coloured SEM image of an M3D-integrated NAND gate, respectively. Figure 1f–h shows the high-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) image and energy-dispersive X-ray spectroscopy (EDS) elemental mapping for the M3D stack, taken at the cross-section indicated by the red dashed line in Fig. 1e.

To achieve an M3D-integrated CMOS chip based on 2D FETs, large-area synthesis of the targeted 2D channel material is required. The multilayer (three to four layers) WSe_2 films used in this study were grown using an MOCVD system[26]. Further details about the growth conditions and synthesis parameters are outlined in Methods. An optical image showcasing the two-inch-wide multilayer WSe_2 growth is presented in Fig. 2a. The multilayer formation was confirmed by atomic force microscopy (Fig. 2b), revealing a coalesced three-/four-layered film with some multilayer islands. Additional HAADF-STEM imaging (Fig. 2c) displays the crystalline 2H structure of the WSe_2 film. The photoluminescence (PL) spectra, captured from ten different areas across the wafer (Fig. 2d), indicates an average peak position at approximately 1.64 eV, further substantiating the multilayer growth. Finally, Fig. 2e presents the Raman spectra collected from the same locations, with detection of the in-plane E^1_{2g} (249 cm^{-1}), out-of-plane 2LA(M) (258 cm^{-1}) and B_{2g} (310 cm^{-1}) Raman modes providing additional evidence of the multilayer composition of the WSe_2 film used in this study.

Next, a polymethyl methacrylate (PMMA)-assisted wet transfer technique (Methods) was used to transfer the WSe_2 films from the sapphire substrate to the device fabrication substrate for assessing the electrical performance. The uniformity of the film post-transfer was confirmed using Raman spectroscopy, with the results being presented in Supplementary Section 1. A crucial step for achieving CMOS capabilities using WSe_2 films is the choice of layer thickness, contact metal and interlayer dielectric (ILD) material. A multilayer (three to four layers) WSe_2 film was selected due to its stability in ambient conditions, high performance, ease of large-area synthesis and, most importantly, capability to achieve ambipolar conduction while maintaining a relatively large ON/OFF current ratio of $>10^4$. These characteristics enable CMOS capabilities, as well as achieve low static power consumption, which is in stark contrast to n-channel metal–oxide–semiconductor-based logic using unipolar 2D materials, such as MoS_2. Extended Data Fig. 1a,b shows the transfer characteristics, that is, the drain current (I_{DS}) plotted against the applied back-gate voltage (V_{BG}), of FETs with Pd contacts based on bilayer and multilayer (three to four layer) WSe_2 films, respectively, grown via MOCVD. Extended Data Fig. 1c,d shows the corresponding histograms for $I_{p_{MAX}}$ and $I_{n_{MAX}}$, respectively, which correspond to the maximum hole and electron currents. Clearly, the multilayer WSe_2 FETs show higher p-branch current compared with the bilayer WSe_2 FETs, with almost two times improvement in $I_{p_{MAX}}$. Even more dramatic improvements are seen in the n-branch current, with ~20 times improvement for multilayer WSe_2. This can be attributed to the smaller bandgap[27] of multilayer WSe_2 compared with monolayer/bilayer WSe_2 and mid-gap pinning of the metal Fermi level[28], making it easier to achieve ambipolar transport.

In addition to layer thickness, the choice of contact metal also plays a critical role in enabling CMOS functionality for WSe_2 FETs. Extended Data Fig. 2a displays the transfer characteristics of 250 devices utilizing Pd and Ni contacts on WSe_2 films, respectively. The Pd contacts primarily yielded p-type characteristics whereas a nearly 100-fold reduction in the p-branch current was observed with Ni contacts, as illustrated by the $I_{p_{MAX}}$ histograms shown in Extended Data Fig. 2b. Ni contacts also enhanced the n-branch current by almost threefold, as evident from the $I_{n_{MAX}}$ histograms shown in Extended Data Fig. 2c. This observation can be ascribed to the differences in how the Fermi levels of Pd and Ni align with the WSe_2 bandgap—both metals enable ambipolar transport; however, Pd aligns closer to the valence band, whereas Ni aligns closer to the conduction band[29].

To further enhance the n-FET performance, surface charge transfer doping was exploited using sub-stoichiometric Al_2O_3 grown via atomic layer deposition (ALD). Extended Data Fig. 3a,b shows the transfer characteristics of 50 WSe_2 FETs with Ni contacts before and after the deposition of Al_2O_3, along with the corresponding histograms for $I_{n_{MAX}}$, respectively. A clear negative shift in the threshold voltage and nearly 100 times improvement in the average $I_{n_{MAX}}$ confirms the n-type doping of WSe_2 using ALD Al_2O_3. The p-branch current was also suppressed by nearly six orders of magnitude, enabling nearly unipolar WSe_2 n-FETs. The observed n-type doping can be attributed to fixed charges and trap states at the WSe_2/Al_2O_3 interface that increase the electron concentration in the WSe_2 channel[30]. This is analogous to modulation doping in high-electron-mobility transistors[31]. In addition, no degradation is seen in the subthreshold slope for the n-branch (SS_n), as illustrated by the histograms shown in Extended Data Fig. 3c, indicating that the donation of electrons stems from donor states that are not located within the bandgap of

https://doi.org/10.1038/s41565-024-01705-2

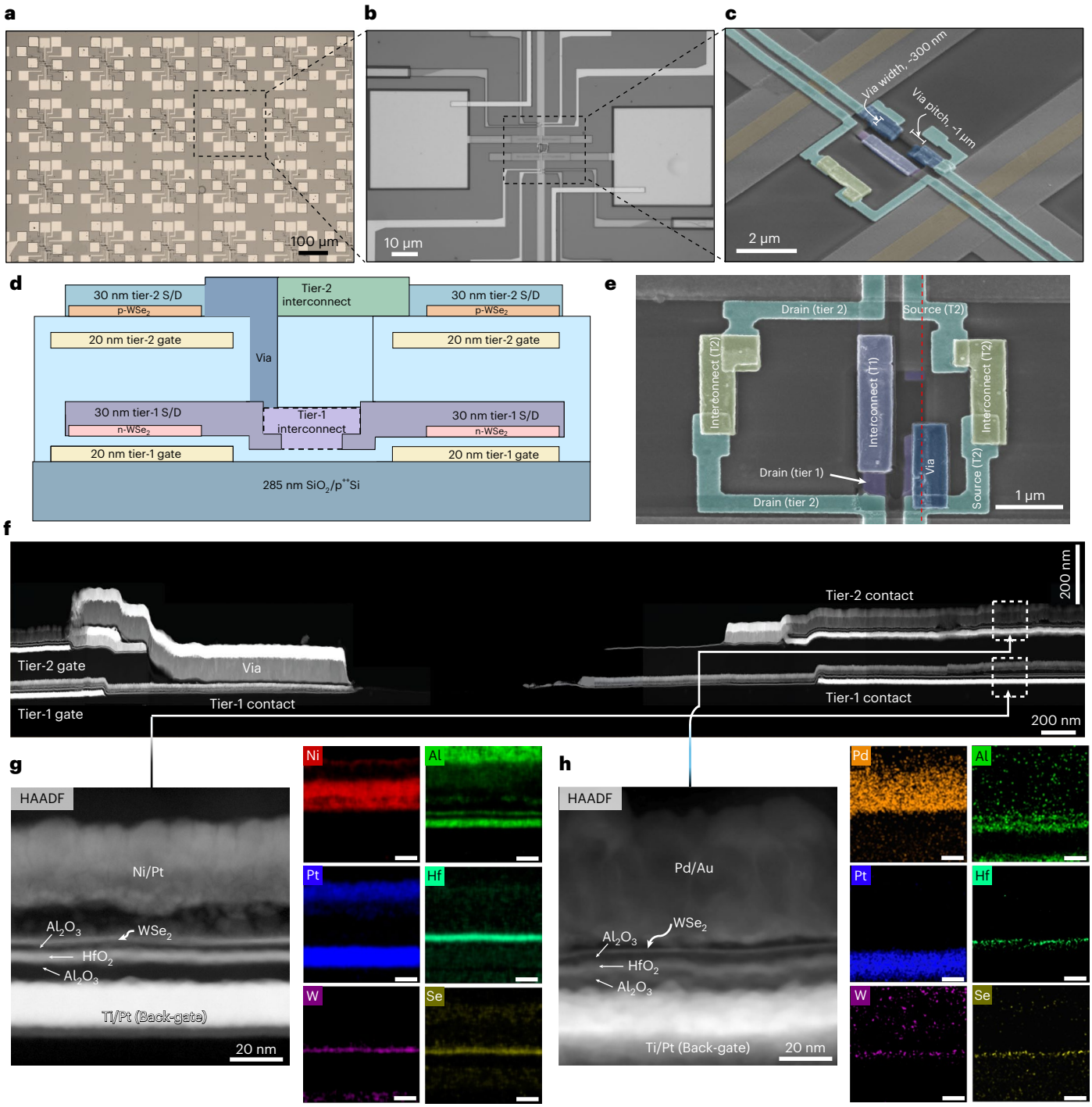


Fig. 1 | M3D integration of CMOS WSe_2 FETs. a, Optical image showing an M3D-integrated, two-tier CMOS circuit based on WSe_2 FETs. **b**, In this configuration, each cell comprises four devices. Here two p-FET devices are positioned directly on top of two n-FET devices. **c**, Angled, false-coloured SEM of the two-tier cell, corresponding to a two-stage inverter circuit. In particular, the via width and pitch achieved in this work are 300 nm and 1 µm, respectively. **d**,**e**, Schematic (**d**) of an M3D-integrated CMOS NAND circuit, with the associated false-coloured SEM image (**e**). The interconnects and vias are labelled, highlighting the dense connectivity obtained through M3D integration. **f**, HAADF-STEM image showing the cross-section of the 3D NAND circuit, taken at the red dotted line given in (**e**). Vertical elongation was applied in **f** to reveal features better. **g**,**h**, Zoomed-in HAADF-STEM and EDS elemental mapping of tier-1 (**g**) and tier-2 (**h**) WSe_2 devices. Scale bars for (**g**) and (**h**), 20 nm.

WSe_2 (ref. 30). Further discussions on the doping-induced trap states and impact on the hysteresis window due to the deposition of ALD Al_2O_3 are available in Supplementary Section 2.

Raman and PL spectroscopy were also implemented to understand the effects of ILD deposition. Extended Data Fig. 4a shows the Raman spectra, in which a redshift of ~1 cm^{-1} is observed in the E^1_{2g} peak, which is indicative of an increased electron concentration in WSe_2 (ref. 32). This is further evidenced by the redshift in the PL emission spectra, along with the broadening of the main peak (Extended Data Fig. 4b). The redshift and peak broadening correlate to the formation of negatively charged trions originating from an increased electron concentration in the WSe_2 film[33–35]. Density functional theory (DFT)

https://doi.org/10.1038/s41565-024-01705-2

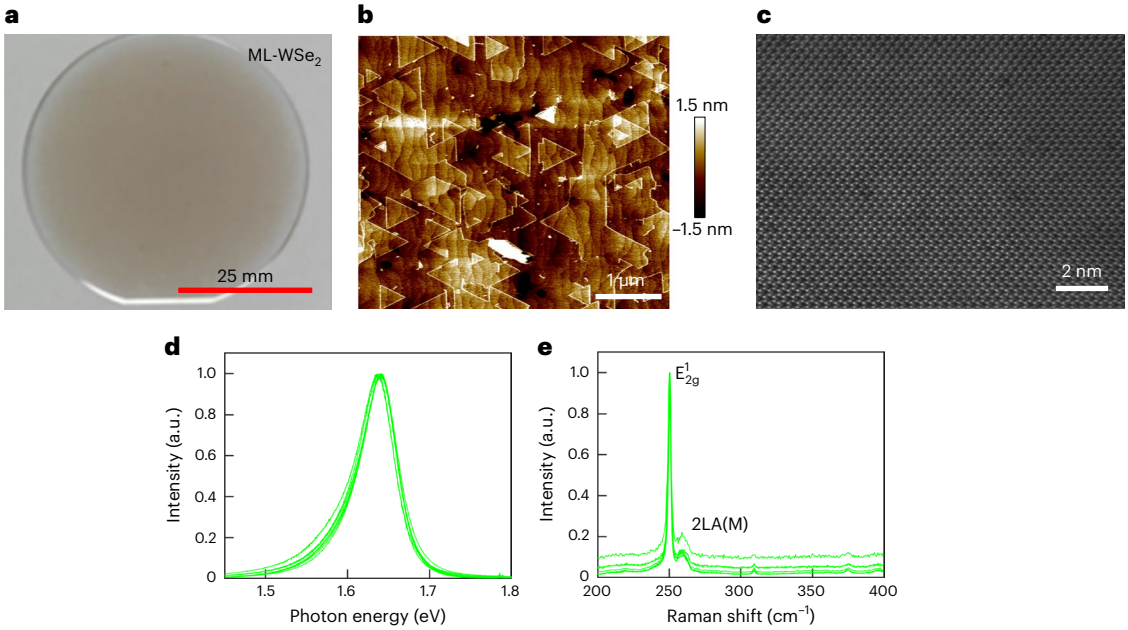


Fig. 2 | Synthesis of large-area MOCVD WSe_2 and fabrication of a 3D stack. **a**, Optical image of the two-inch growth of multilayer (ML) WSe_2 using MOCVD. **b**, Atomic force microscopy image of ML-WSe_2 at the centre of the wafer. Multilayer islands are observed on the coalesced film. **c**, HAADF-STEM image of the ML-WSe_2 taken from the *c* axis, showing the atomic structure of the as-grown film. **d**, PL spectra of the WSe_2 film. The peak position was found to be ~1.65 eV, correlating to multilayer WSe_2. **e**, Raman spectra of the WSe_2 film consisting of the characteristic in-plane E^1_{2g} peak at 249 cm^{-1} and out-of-plane 2LA(M) peak at 258 cm^{-1}. Raman and PL spectra were both taken at ten spots across the two-inch WSe_2 wafer.

calculations were also employed to examine the influence of Al_2O_3 dielectric deposition on WSe_2. A detailed discussion on the band structure of pristine WSe_2 as well as Al_2O_3-capped WSe_2, along with the projected density of states calculations before and after ALD, is described in Supplementary Section 3.

Fabrication of two-tier 3D CMOS ICs

Following the optimization of WSe_2 film thickness, contact metal and dielectric interface, the fabrication of a WSe_2-based, two-tier M3D CMOS IC was accomplished on a 285 nm SiO_2/p^{++} Si substrate. In principle, any lithography-compatible substrate can be utilized to achieve a 3D CMOS IC. Both tiers of devices consist of a 2 nm Ti/18 nm Pt back-gate and a 9 nm Al_2O_3/3 nm HfO_2/3 nm Al_2O_3 back-gate dielectric stack, with an equivalent oxide thickness (EOT) of ~6 nm. The implemented gate stack provides a flash-memory-like functionality for realization of in-memory computing applications. A detailed discussion on the memory stack and its functionalities can be found in Supplementary Section 4. As discussed earlier, to enable n-FET and p-FET devices in tier 1 and tier 2, respectively, different contact materials were employed: 20 nm of Ni/10 nm of Pt for tier-1 n-FET devices and 20 nm of Pd/10 nm of Au for tier-2 p-FET devices. To ensure electrical isolation between the n-FET devices of tier 1 and the p-FET devices of tier 2, an ~82-nm-thick layer of ALD-grown Al_2O_3 was used as an ILD while also servings as the n-type doping layer for tier-1 n-FET devices. Finally, a via-last approach was implemented to establish the required connections between the devices in tier 1 and tier 2, facilitating the demonstration of our circuit. The vias were constructed using 90 nm Ni and 30 nm Au, ensuring robust connectivity across tiers with a via width of 300 nm. This achievement in via dimensions underscores the enhanced packing density enabled by M3D integration techniques. The process used for achieving 3D CMOS integration is detailed in Supplementary Section 5, and a thorough explanation of the fabrication steps is available in Methods as well as in our previous work[20].

The device characteristics for tier-1 devices were re-evaluated after the completion of tier-2 fabrication. Figure 3a,f shows the transfer characteristics of 340 tier-1 and tier-2 devices, respectively, in which a nearly four-order magnitude decrease in the p-branch characteristics and two-order magnitude improvement in the n-branch characteristics are observed between the tier-1 and tier-2 devices. All devices discussed have a channel length (L_{CH}) and channel width (W) of 300 nm and 1 μm respectively, unless stated otherwise, and all the parameters were extracted for a drain bias (V_{DS}) of 1 V. Figure 3b shows the distribution of the threshold voltage extracted from the n-branch ($V_{TH\text{-}n}$) extracted using the iso-current method at a drain current (I_{DS}) of 100 nA μm^{-1} for tier-1 devices. The average $V_{TH\text{-}n}$ acquired for the n-branch of the tier-1 devices was 1.35 V, with a standard deviation of 0.97 V. The subthreshold slope for the n-branch (SS_n; Fig. 3c) for two orders of magnitude change in I_{DS} was also extracted, in which a minimum SS_n of 142 mV dec^{-1}, an average SS_n of 282 mV dec^{-1} and a standard deviation of 73 mV dec^{-1} were achieved for tier-1 devices. Figure 3d shows the distribution of the n-branch ON-current (I_n), extracted for a carrier concentration (n_s) of 1.4×10^{13} cm^{-2} corresponding to an overdrive voltage (V_{OV}) of 3.4 V. The maximum I_n achieved was 26.00 μA μm^{-1}, with a mean and standard deviation of 10.80 and 5.84 μA μm^{-1}, respectively. Finally, Fig. 3e shows the distribution of the extracted electron field-effect mobility (μ_n), obtained using the peak-transconductance method. The maximum electron mobility obtained was 6.90 $cm^2\ V^{-1}\ s^{-1}$, with an average and standard deviation of 3.11 and 1.38 $cm^2\ V^{-1}\ s^{-1}$, respectively.

Figure 3g–j outlines the extracted device parameters for the p-branch in tier-2 devices. Figure 3g shows the distribution of $V_{TH\text{-}p}$ for the same iso-current (100 nA μm^{-1}), with an average $V_{TH\text{-}p}$ value of −0.84 V and a standard deviation of 0.33 V. The distinct $V_{TH\text{-}p}$ ranges observed between the tier-1 and tier-2 devices are pivotal for achieving CMOS circuits with discrete and well-defined logic levels. The avoidance of overlap in the threshold voltage is essential, as it ensures that each device operates at its designated logic level. The subthreshold slope for the p-branch (SS_p; Fig. 3h) is extracted for two orders of magnitude change in I_{DS}, in which a minimum SS_p of 244 mV dec^{-1}, average SS_p of 570 mV dec^{-1} and standard deviation of 160 mV dec^{-1} were achieved. Although further passivation strategies to minimize the defect density present in WSe_2 must be explored to further improve the subthreshold slopes, the achieved SS_n and SS_p values were found to be adequate for

https://doi.org/10.1038/s41565-024-01705-2

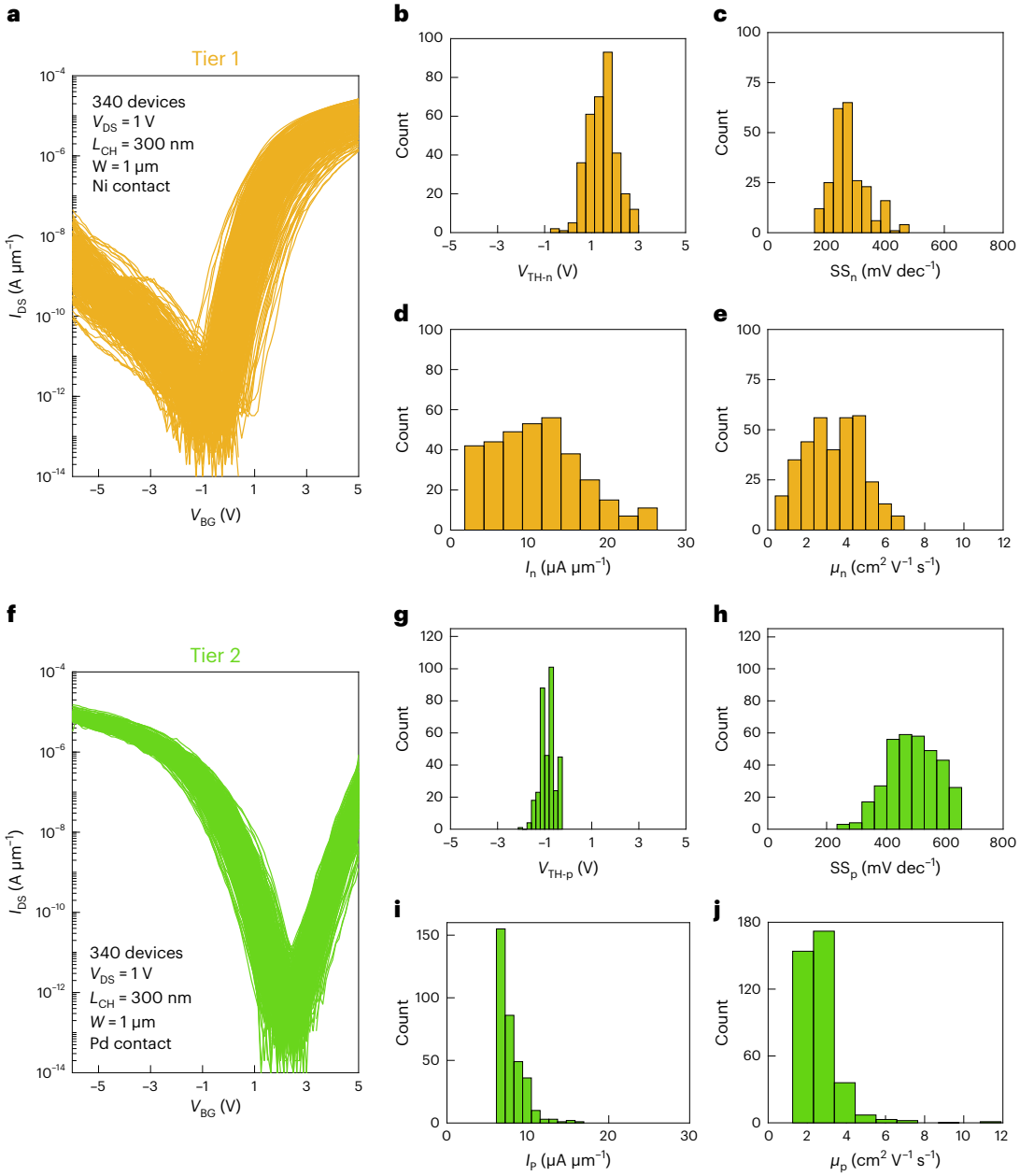


Fig. 3 | M3D-integrated CMOS WSe_2 FETs. a, Transfer characteristics of 340 tier-1 WSe_2 n-FETs of channel length (L_{CH}) of 300 nm and width (W) of 1 µm. **b**–**e**, The corresponding histograms of threshold voltage (V_{TH-n}) (**b**) extracted at a drain current (I_{DS}) of 100 nA µm^{-1} for the n-branch, subthreshold slope (SS_n) for two orders of change in I_{DS} (**c**), ON-current (I_n) (**d**) and electron field-effect mobility (μ_n) (**e**). **f**–**j**, Transfer characteristics of 340 tier-2 WSe_2 p-FETs (**f**), with the corresponding histograms showing the distributions of V_{TH-p} for the p-branch (**g**), SS_p (**h**), I_p (**i**) and hole field-effect mobility (μ_p) (**j**). Note that all the parameters were extracted at a drain bias (V_{DS}) of 1 V.

the proper functioning of WSe_2 FET-based CMOS inverters and logic gates, which will be illustrated in the subsequent sections. Figure 3i shows the distribution of the p-branch ON current (I_p), extracted for a carrier concentration (p_s) of 1.64×10^{13} cm^{-2} corresponding to V_{OV} of −4 V. The maximum I_p achieved was 16.00 µA µm^{-1}, with the mean and standard deviation of 7.85 and 1.64 µA µm^{-1}, respectively. Note that the ON current for WSe_2-based n-FET and p-FET are relatively similar, which is critical for the design of ICs. In Supplementary Section 6, we provide a benchmarking discussion on the device-to-device variation among WSe_2 FETs against existing silicon technology. Although further improvement in material quality and interfaces can enhance the performance, our approach of combining contact and dielectric engineering to achieve nearly symmetric n-FET and p-FET characteristics is noteworthy.

Additionally, it is worth mentioning that the device-to-device variation between tier-1 and tier-2 devices is more significantly affected by the growth and transfer process of the WSe_2 film, rather than the enhanced topographical complexities observed in tier 2. Extended Data Fig. 5a shows the transfer characteristics between 240 planar and tier-2 devices with Pd contacts, in which the channel material for both sets of devices was synthesized under similar growth conditions and was transferred via the same PMMA-assisted wet transfer technique. Interestingly, the tier-2 devices exhibit higher I_{pMAX} (Extended Data Fig. 5b) reduced device-to-device variation, as evidenced by the V_{TH-p} distribution (Extended Data Fig. 5c) and lower SS_p (Extended Data Fig. 5d). This established that the topography plays a secondary role in device-to-device variation in two-tier M3D integration of WSe_2 FETs. However, we believe that a chemical mechanical polishing technique

https://doi.org/10.1038/s41565-024-01705-2

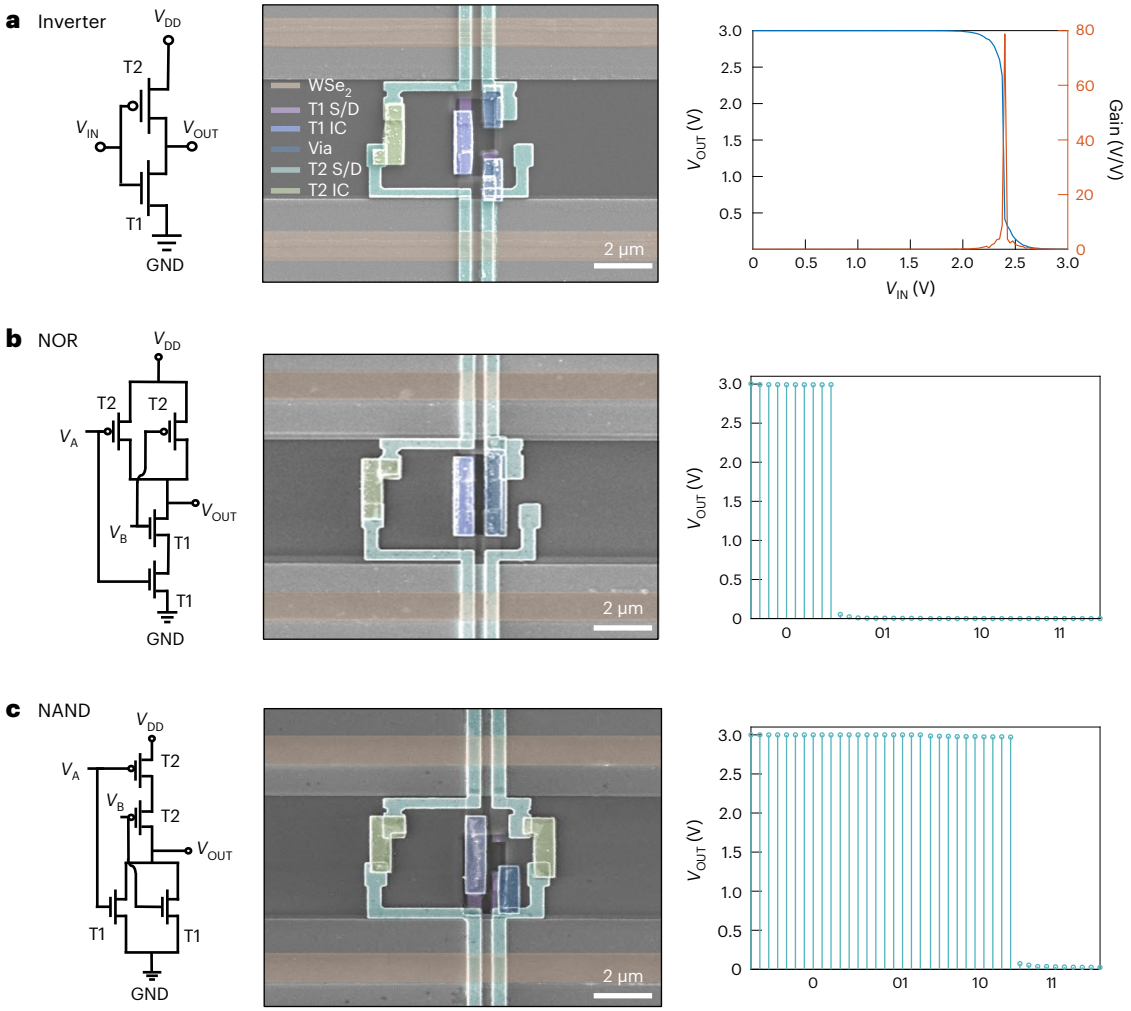


Fig. 4 | M3D integrated logic gates. a–**c**, Schematic, false-coloured SEM image and output characteristics of a representative M3D integrated inverter (**a**), NOR gate (**b**) and NAND gate (**c**). The peak gain achieved in the best-performing inverter was ~79 for V_{DD} = 3 V. Distinct logic levels were obtained for the NAND and NOR gates.

can be introduced as more tiers are incorporated into M3D chips, effectively addressing the challenges linked to topography.

Another valid consideration is the feasibility of demonstrating p-FETs on any tier, even when the device is encapsulated with an ILD. Extended Data Fig. 6a,b shows 40 WSe_2 FETs with Pd contacts before and after 5 nm HfO_2 ALD deposition. Clearly, no improvement in the n-branch characteristics is observed, although the p-branch current does degrade. It is worth mentioning that additional p-doping strategies, such as substitutional doping with vanadium or surface charge transfer doping with WO_xSe_y or NO_x, can be implemented to further enhance the p-FET characteristics[36–38]. Extended Data Fig. 6c shows the transfer characteristics of the WSe_2 FETs with the HfO_2 ILD after 20 s of O_2 plasma. A positive shift in V_{TH}, along with an increase in the p-branch current and suppression of the n-branch current is observed. In other words, through careful engineering of the contact and dielectric interfaces, it is possible to create unipolar WSe_2 p-FETs and n-FETs, making them an excellent option for constructing CMOS circuits.

Monolithic and 3D integrated CMOS circuits

Following the electrical characterization of n-FET devices in tier 1 and p-FET devices in tier 2, electron-beam lithography (EBL) was employed to define 1 μm × 6 μm rectangles. Reactive ion etching (RIE) was then utilized to etch the exposed ILD, providing access to the tier-1 devices. EBL and electron-beam evaporation (EBE) were then carried out to define and deposit 300 nm vias connecting the tier-1 and tier-2 devices, thereby forming the intended circuit. It is important to note that EBL provides exceptional alignment precision, a critical parameter influencing the allowable pitch of microbumps for die stacking. Figure 4a–c shows the circuit schematic, false-coloured SEM images, and output characteristics of a representative M3D-integrated inverter, NOR gate and NAND gate, respectively. The supply voltages were maintained at V_{DD} = 3 V and V_{SS} = 0 V for all circuit demonstrations. The top-performing inverter achieved a peak gain of ~79 at V_{DD} = 3 V, which is comparable with the gain values obtained in vertically integrated inverters reported in previous studies for the same V_{DD} (refs. 17,22,39,40). Extended Data Fig. 7a,b shows the output characteristics and distribution of the peak gain achieved in the 27 fabricated inverters, underscoring the robustness of the proposed via fabrication process flow. Note that the state transition point for the inverters does not always occur at $V_{IN}/2$, which could lead to increased power usage and reduced noise immunity. To address this issue, our programmable back-gate stack can be employed to adjust the inverter's switching threshold (Extended Data Fig. 7c). By applying a programming voltage to the back-gate stacks of both tier-1 and tier-2 devices, it is possible to alter the threshold voltages of both n-type and p-type WSe_2 FETs and hence adjust the inflection point. The programmed inverters demonstrated a low noise margin (NM_L) and high noise margin (NM_H) of 1.23 and 1.49 V, respectively, nearing the ideal 1.50 V mark and aligning with results from similar studies on WSe_2-based CMOS inverters[41]. The NAND and NOR gates exhibit proper functionality, with clear differentiation between the logic levels.

Although deviations from the ideal output are observed in some circuits due to unwanted conduction in the pull-up p-FET or pull-down n-FET networks, the ratio between 'high' and 'low' logic states remains substantial. This can be corrected through further suppression of the n-branch in the p-FETs and the p-branch in the n-FETs to enhance the circuit performance. Supplementary Section 7 discusses strategies to accomplish unipolar conduction in WSe_2 FETs.

Conclusion

In conclusion, our work demonstrates the successful achievement of dense and scaled M3D integration for the realization of CMOS circuits based on n- and p-type WSe_2 FETs through the utilization of 300 nm vias with a pitch of ~1 µm, connecting over 200 devices in a two-tier chip. Furthermore, the demonstration of superior packing and connectivity in M3D is exemplified through the fabrication of vertically integrated logic gates, encompassing inverters, NAND gates and NOR gates. This demonstration not only emphasizes the feasibility of M3D for 2D CMOS devices but also highlights the potential of 2D materials to drive advancements in 'More Moore' technologies.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41565-024-01705-2.

References

1. Yu, E. et al. FinFET scaling to 10 nm gate length. In *Digest International Electron Devices Meeting* 251–254 (IEEE, 2002).
2. Mistry, K. et al. A 45nm logic technology with high-*k*+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging. In *2007 IEEE International Electron Devices Meeting* 247–250 (IEEE, 2007).
3. Natarajan, S. et al. A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size. In *2014 IEEE International Electron Devices Meeting* 3.7.1–3.7.3 (IEEE, 2014).
4. Turkot, B., Carson, S. & Lio, A. Continuing Moore's law with EUV lithography. In *2017 IEEE International Electron Devices Meeting (IEDM)* 14.4.1–14.4.3 (IEEE, 2017).
5. Iyer, S. S. Three-dimensional integration: an industry perspective. *MRS Bull.* **40**, 225–232 (2015).
6. Dhananjay, K., Shukla, P., Pavlidis, V. F., Coskun, A. & Salman, E. Monolithic 3D integrated circuits: recent trends and future prospects. *IEEE Trans. Circuits Syst., II, Exp. Briefs* **68**, 837–843 (2021).
7. Srivastava, N. & Banerjee, K. Interconnect challenges for nanoscale electronic circuits. *JOM* **56**, 30–31 (2004).
8. Li, Y. et al. Monolithic 3D integration of logic, memory and computing-in-memory for one-shot learning. In *2021 IEEE International Electron Devices Meeting (IEDM)* 21.5.1–21.5.4 (IEEE, 2021).
9. Kagawa, Y. & Iwamoto, H. 3D integration technologies for the stacked CMOS image sensors. In *2019 International 3D Systems Integration Conference (3DIC)* 1–4 (IEEE, 2019).
10. Ingerly, D. B. et al. Foveros: 3D integration and the use of face-to-face chip stacking for logic devices. In *2019 IEEE International Electron Devices Meeting (IEDM)* 19.6.1–19.6.4 (IEEE, 2019).
11. Batude, P. et al. Advances in 3D CMOS sequential integration. In *2009 IEEE International Electron Devices Meeting (IEDM)* 1–4 (IEEE, 2009).
12. Samal, S. K., Nayak, D., Ichihashi, M., Banna, S. & Lim, S. K. Monolithic 3D IC vs. TSV-based 3D IC in 14nm FinFET technology. In *2016 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)* 1–2 (IEEE, 2016).
13. Batude, P. et al. 3-D sequential integration: a key enabling technology for heterogeneous co-integration of new function with CMOS. *IEEE Trans. Emerg. Sel. Topics Circuits Syst.* **2**, 714–722 (2012).
14. Rachmady, W. et al. 300mm heterogeneous 3D integration of record performance layer transfer germanium PMOS with silicon NMOS for low power high performance logic applications. In *2019 IEEE International Electron Devices Meeting (IEDM)* 29.7.1–29.7. 4 (IEEE, 2019).
15. Then, H. W. et al. 3D heterogeneous integration of high performance high-*K* metal gate GaN NMOS and Si PMOS transistors on 300mm high-resistivity Si substrate for energy-efficient and compact power delivery, RF (5G and beyond) and SoC applications. In *2019 IEEE International Electron Devices Meeting (IEDM)* 17.3.1–17.3.4 (IEEE, 2019).
16. Shulaker, M. M. et al. Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. *Nature* **547**, 74–78 (2017).
17. Tong, L. et al. Heterogeneous complementary field-effect transistors based on silicon and molybdenum disulfide. *Nat. Electron.* **6**, 37–44 (2023).
18. Zhu, J. et al. Low-thermal-budget synthesis of monolayer molybdenum disulfide for silicon back-end-of-line integration on a 200 mm platform. *Nat. Nanotechnol.* **18**, 456–463 (2023).
19. Zhu, K. et al. Hybrid 2D–CMOS microchips for memristive applications. *Nature* **618**, 57–62 (2023).
20. Jayachandran, D. et al. Three-dimensional integration of two-dimensional field-effect transistors. *Nature* **625**, 276–281 (2024).
21. Kang, J.-H. et al. Monolithic 3D integration of 2D materials-based electronics towards ultimate edge computing solutions. *Nat. Mater.* **22**, 1470–1477 (2023).
22. Xia, Y. et al. Wafer-scale demonstration of MBC-FET and C-FET arrays based on two-dimensional semiconductors. *Small* **18**, 2107650 (2022).
23. Liu, M. et al. Large-scale ultrathin channel nanosheet-stacked CFET based on CVD 1L MoS_2/WSe_2. *Adv. Electron. Mater.* **9**, 2200722 (2022).
24. Lau, J. H. Recent advances and trends in advanced packaging. *IEEE Trans. Compon. Packag. Manuf. Technol.* **12**, 228–252 (2022).
25. Vinet, M. et al. 3D monolithic integration: technological challenges and electrical results. *Microelectron. Eng.* **88**, 331–335 (2011).
26. Xuan, Y. et al. Multi-scale modeling of gas-phase reactions in metal-organic chemical vapor deposition growth of WSe_2. *J. Cryst. Growth* **527**, 125247 (2019).
27. Desai, S. B. et al. Strain-induced indirect to direct bandgap transition in multilayer WSe_2. *Nano Lett.* **14**, 4592–4597 (2014).
28. Das, S. & Appenzeller, J. WSe_2 field effect transistors with enhanced ambipolar characteristics. *Appl. Phys. Lett.* **103**, 103501 (2013).
29. Schulman, D. S., Arnold, A. J. & Das, S. Contact engineering for 2D materials and devices. *Chem. Soc. Rev.* **47**, 3037–3058 (2018).
30. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High current density in monolayer MoS_2 doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).
31. Drummond, T., Morkoc, H., Lee, K. & Shur, M. Model for modulation doped field effect transistor. *IEEE Electron Device Lett.* **3**, 338–341 (1982).
32. Park, Y. J., Katiyar, A. K., Hoang, A. T. & Ahn, J.-H. Controllable p- and n-type conversion of $MoTe_2$ via oxide interfacial layer for logic circuits. *Small* **15**, 1901772 (2019).

33. Das, T., Youn, S., Seo, J. E., Yang, E. & Chang, J. Large-scale complementary logic circuit enabled by Al_2O_3 passivation-induced carrier polarity modulation in tungsten diselenide. *ACS Appl. Mater. Interfaces* **15**, 45116–45127 (2023).
34. Lockhart de la Rosa, C. J. et al. Highly efficient and stable MoS_2 FETs with reversible n-doping using a dehydrated poly(vinyl-alcohol) coating. *Nanoscale* **9**, 258–265 (2017).
35. Chen, K. et al. Air stable n-doping of WSe_2 by silicon nitride thin films with tunable fixed charge density. *APL Mater.* **2**, 092504 (2014).
36. Kozhakhmetov, A. et al. Controllable p-type doping of 2D WSe_2 via vanadium substitution. *Adv. Funct. Mater.* **31**, 2105252 (2021).
37. Chiang, C. C., Lan, H. Y., Pang, C. S., Appenzeller, J. & Chen, Z. Air-stable p-doping in record high-performance monolayer WSe_2 devices. *IEEE Electron Device Lett.* **43**, 319–322 (2022).
38. Oberoi, A. et al. Toward high-performance p-type two-dimensional field effect transistors: contact engineering, scaling, and doping. *ACS Nano* **17**, 19709–19723 (2023).
39. Sachid, A. B. et al. Monolithic 3D CMOS using layered semiconductors. *Adv. Mater.* **28**, 2547–2554 (2016).
40. Jia, X. et al. High-performance CMOS inverter array with monolithic 3D architecture based on CVD-grown n-MoS_2 and p-$MoTe_2$. *Small* **19**, 2207927 (2023).
41. Pang, C.-S. et al. Atomically controlled tunable doping in high-performance WSe_2 devices. *Adv. Electron. Mater.* **6**, 1901304 (2020).

[1]Engineering Science and Mechanics, Penn State University, University Park, PA, USA. [2]2D Crystal Consortium Materials Innovation Platform, Penn State University, University Park, PA, USA. [3]Materials Science and Engineering, Penn State University, University Park, PA, USA. [4]Department of Physics, Harcourt Butler Technical University, Kanpur, India. [5]Materials Research Institute, Penn State University, University Park, PA, USA. [6]Nuclear Engineering, Penn State University, University Park, PA, USA. [7]Electrical Engineering, Penn State University, University Park, PA, USA. ✉e-mail: rqp5233@psu.edu; sud70@psu.edu

Methods

WSe_2 synthesis

The growth of a multilayer WSe_2 on two-inch-diameter *c*-plane sapphire was carried out in an MOCVD system (https://doi.org/10.60551/znh3-mj13) in the 2D Crystal Consortium Materials Innovation Platform (2DCC-MIP) facility at Penn State. The MOCVD system is equipped with a cold-wall horizontal reactor with an inductively heated graphite susceptor with gas-foil wafer rotation[26]. Tungsten hexacarbonyl ($W(CO)_6$) with purity of ≥99.9% (trace metals basis) purchased from Sigma-Aldrich was used as a metal precursor. Hydrogen selenide (H_2Se) was used as a chalcogen gaseous precursor. Hydrogen (H_2) was used as a carrier gas. The $W(CO)_6$ powder was maintained at 30 °C and 400 torr in a stainless-steel bubbler. Synthesis of the WSe_2 monolayer was based on a multistep process, consisting of nucleation, ripening and lateral growth steps, as described previously[42]. In general, the WSe_2 sample was nucleated for 30 s at 850 °C, then ripened for 5 min at 850 °C and 5 min at 1,000 °C, and then grown at 1,000 °C for growth times ranging from 25 to 35 min. During the lateral growth step, the tungsten flow rate was set as 3.8×10^{-3} s.c.c.m. and the chalcogen flow rate was set as 75 s.c.c.m., whereas the reactor pressure was maintained at 200 torr. Then, the multilayer WSe_2 was annealed under ambient H_2 and H_2Se for 10 min and the ambient H_2 and H_2Se were maintained for 8 min during cool-down to provide additional time for metal adatom diffusion and to reduce selenium vacancies. Under the identical growth conditions, the number of WSe_2 layers can be manipulated by varying the growth time. The growth of a multilayer WSe_2 film was achieved using an extended growth time ranging from 25 to 35 min across the two-inch sapphire substrate, which gives rise to a multilayer WSe_2 across the entire two-inch wafer. Detailed growth and characterization data associated with the multilayer WSe_2 samples produced in this study are available at https://doi.org/10.26207/x074-bw26. This includes substrate preparation and recipe data for samples grown by MOCVD in the 2DCC-MIP facility and standard characterization data including atomic force microscopy images and room-temperature Raman/PL spectra on the samples.

Fabrication of local back-gate islands

To define the locally back-gated island regions, a commercially purchased substrate (thermally grown 285 nm SiO_2 on p^{++}-Si) was spin-coated with a bilayer electron-beam resist stack consisting of EL6 and A3 resists at 4,000 r.p.m. for 45 s. The resist stack was baked at 150 °C for 90 s and 180 °C for 90 s. The bilayer electron-beam resist was then patterned using EBL to define the islands and developed in 1:1 methyl isobutyl ketone:2-propanol (IPA) mixture for 60 s, followed by IPA for 45 s. The back-gate electrodes of 2/18 nm Ti/Pt were then deposited using EBE in a Temescal FC-2000 Bell Jar Deposition System. Liftoff of the remaining electron-beam resist and excess metal was performed using acetone, and the substrate was then cleaned using IPA. An ALD process was then implemented to grow the back-gate dielectric stack consisting of 9 nm Al_2O_3, 3 nm HfO_2 and 3 nm Al_2O_3. Access to the individual Pt back-gate electrodes was achieved via an RIE process conducted in a Plasma-Therm Versalock 700 device. EBL was used to define the access pads using ZEP electron-beam resist, which was spin coated at 2,500 r.p.m. for 45 s followed by baking at 180 °C for 3 min. After exposure, the sample was developed using n-amyl acetate at room temperature. The dielectric stack was then dry etched using BCl_3 gas at 5 °C for 25 s. Finally, the electron-beam resist was removed using a photoresist stripper (PRS 3000) and cleaned with IPA.

PMMA-assisted wet transfer technique

To fabricate the 2D FETs, MOCVD-grown monolayer films were transferred from the sapphire growth substrate to the pre-fabricated island substrate using a PMMA-assisted transfer process. Initially, the 2D film on the sapphire substrate underwent a double spin-coating process with PMMA, both at 4,000 r.p.m. for 45 s. Subsequently, the corners of the spin-coated films were scored with a razor blade before immersion in a 1 M NaOH solution maintained at 90 °C. The NaOH permeates between the substrate/film interface due to capillary forces, which delaminates the 2D film from the growth substrate. The separated film was then fished out and subjected to three rinses in a water bath before being transferred onto the device substrate. The sample was then annealed at 50 °C and 70 °C for 10 min each to improve adhesion. The sample was subsequently placed in an acetone bath for 10 min followed by an IPA bath for 10 min to remove the PMMA resist.

Via integration process

Following the fabrication of tier-2 devices, ZEP 520A resist was spin-coated onto the substrate at 2,000 r.p.m. for 45 s and subsequently annealed at 180 °C for 3 min. A 6 µm × 1 µm rectangle was defined to expose the area containing the tier-1 source and drain terminals. After exposure, the pattern was developed in n-amyl acetate for 3 min, followed by 1 min in IPA. RIE was then performed in a Plasma-Therm Versalock 700 system using a BCl_3 chemistry for 100 s. Following RIE, the residual resist was removed in a PRS 3000 bath for 10 min, followed by rinsing in IPA and water for 10 min each. To create the via connection between devices, a bilayer resist consisting of PMMA EL11 and MMA A3 was spin coated at 4,000 r.p.m. for 45 s, followed by annealing at 150 and 180 °C for 90 s each, respectively. Vias were defined using EBL; following exposure, the sample was developed in 1:1 methyl isobutyl ketone:IPA for 60 s and then IPA for 60 s. EBE of 90 nm Ni and 30 nm Au was performed to ensure connectivity between the tier-1 and tier-2 devices. After EBE, the residual resist and metal were lifted off by placing the sample in 85 °C acetone for ~20 min and IPA for 10 min.

Raman and PL spectroscopy

Raman and PL spectra were taken on the multilayer WSe_2 film as-grown on two-inch *c*-plane sapphire substrates using a WITec alpha300 apyron system within a N_2-ambient glovebox with ~5 ppm of O_2 and H_2O. Single-point Raman and PL spectra were taken using a ×100 objective at a 4 mW laser power for 30 s and three accumulations and 5 s and two accumulations, respectively.

SEM

SEM of the 2D MoS_2 transistors used in this study was conducted using a Zeiss Gemini 500 field-emission SEM system at an accelerating voltage of 5 kV.

TEM sample preparation

The TEM sample shown in Fig. 1f–h was prepared using a Thermo Fisher Scientific Scios 2 DualBeam focused ion beam (FIB) SEM instrument. The sample was first coated with two carbon layers using a 1.6 nA electron beam and 0.1 nA Ga ion beam in sequence. The first layer deposited by the electron beam was ~0.5 µm thick and was used to protect the surface WSe_2 layer from Ga ion beam damage in the next step of carbon deposition. The second layer deposited by the Ga ion beam was approximately 4 µm thick, and was used as surface protection during ion beam milling and sample thinning. Following this, an approximately 2-µm-thick sample cross-section around the region of interest was lifted out and in situ transferred to a copper half-grid. The lamella was then thinned using a Ga ion beam at five decreasing voltage levels: 30, 16, 8, 5 and 2 kV. The ion beam voltage was gradually decreased as the sample got thinner to minimize ion beam damage.

STEM characterization

The cross-sectional STEM and EDS analyses in Fig. 1 were performed using the aberration-corrected Thermo Fisher Scientific Titan3 G2 60-300 TEM/STEM instrument, which was operated at a 300 kV accelerating voltage. This instrument was set with a C2 aperture of 70 µm, a spot size of 6 and a convergent angle of 25.2 mrad. Elemental mapping by EDS was performed with the Super-X EDS system under the

STEM mode. A lower-magnification image that includes a detailed dual-electrode STEM view (Fig. 1f) was taken with a beam current of 0.07 nA. The EDS mappings were obtained using a beam current of 0.227 nA. EDS data were analysed using Esprit software with the following parameters: 1/4 Q-Map pre-processing, averaging of 9 pixels for post-filtering, and the use of mass percent (norm.) for quantification. Due to the presence of more than 11 elements in the sample and the close proximity of the X-ray edges of some elements, deconvoluting signals from each element perfectly using Esprit posed a challenge. To address this, gamma and brightness adjustments were applied in Esprit to reduce the contrast of the false-positive signals and enhance the signal-to-noise ratio. A signal was considered false-positive when a strong edge for an element was missing from the spectrum while its other edge overlapped with another element's edge. Consequently, the adjustments in gamma and brightness resulted in non-standardized color bars for each element. Thus, the elemental maps generated highlight the locations where specific elements are concentrated, but comparing the absolute intensity between different elements is not recommended. The multilayer WSe_2 in Fig. 2c was imaged down its c-axis using the same TEM/STEM instrument operated at an accelerating voltage of 80 kV. The instrument was set with a C2 aperture of 70 µm and a convergence angle of 25.2 mrad, and the collection angle range of the HAADF detector was 42–244 mrad.

Computational details

All DFT calculations were conducted using the Virtual NanoLab QuantumATK tool. We used generalized gradient approximation within the Perdew–Burke–Ernzerhof formalism and Fritz-Haber Institute (FHI) pseudopotential for exchange–correlation functionals. A Monkhorst–Pack-type mesh k-point grid of $3 \times 3 \times 1$ at an energy cutoff of 60 Hartree was utilized to sample the first Brillouin zone of the $4 \times 4 \times 1$ supercell of monolayer WSe_2. A vacuum space of 30 Å was included perpendicular to the surface to prevent coupling between neighbouring cells. Fermi–Dirac occupation methods were used to calculate the Fermi energy relative to the vacuum level. Structures were fully relaxed until the force on each atom was below 0.01 eV $Å^{-1}$ to minimize the total energy. Iteration control parameters included a Pulay mixer algorithm with a maximum of 100 steps and a tolerance limit of 10^{-5}. To study oxide–TMDC interactions, we adsorbed a few molecules of Al_2O_3 and HfO_2 dielectrics on monolayer WSe_2 surface to balance the computational efficiency and optimized using DFT to achieve minimum-energy configurations. The generalized gradient approximation was primarily utilized for the exchange–correlation potential to match the experimental bandgap (E_g = 1.54 eV) of monolayer WSe_2. Although spin–orbit coupling affects energy band splitting in free-standing TMDC layers, its impact on oxide–TMDC interactions is negligible due to strong Fermi-level pinning. Hence, spin–orbit coupling was not considered in this study.

Electrical characterization

Electrical characterization of the fabricated M3D devices was performed using a semi-automated FormFactor 12000 probe station under atmospheric conditions with a Keysight B1500A parameter analyser.

Data availability

Data on the samples produced in the 2DCC-MIP facility is available at https://doi.org/10.26207/x074-bw26. This includes the growth recipes and characterization data. Additional datasets generated during and/or analysed in the current study are available from the corresponding authors on reasonable request.

Code availability

The codes used for plotting the data are available from the corresponding authors on reasonable request.

References

42. Zhang, X. et al. Diffusion-controlled epitaxy of large area coalesced WSe_2 monolayers on sapphire. *Nano Lett.* **18**, 1049–1056 (2018).

Acknowledgements

We thank H. Ravichandran for performing the 2D material transfer for TEM analysis. The MOCVD samples were grown in the 2D Crystal Consortium Materials Innovation Platform (2DCC-MIP) facility at Penn State, which is supported by the National Science Foundation under cooperative agreement DMR-2039351.
We would like to acknowledge funding by the Department of Defense, Defense Threat Reduction Agency (DTRA), as part of the Interaction of Ionizing Radiation with Matter University Research Alliance (IIRM-URA) under contract no. HDTRA1-20-2-0002. The work was supported by the Army Research Office (ARO) through contract no. W911NF1810268, National Science Foundation (NSF) through CAREER Award under grant nos. ECCS-2042154 and ECCS-2328741.

Author contributions

S.D., R.P. and D.J. conceived the idea and designed the experiments. R.P., N.U.S., M.U.K.S. and D.J. fabricated the 3D chip. S.D., R.P., N.U.S., M.U.K.S., D.J., A.O. and S.G. performed the experiments, analysed the data, discussed the results and agreed on their implications. Y.S. and Z.Z. prepared the FIB sample and performed the cross-sectional STEM-EDS data collection and analysis for the 3D chip under the supervision of Y.Y. S.P.S. performed the in-plane STEM imaging on the ML-WSe_2. C.C. and S.K. grew and characterized the 2D materials under the supervision of J.M.R. S.G. and D.S. performed the DFT simulations. S.D., J.M.R., Y.Y. and D.E.W. secured funding for the project and supervised the students and post-docs. All authors contributed to the preparation of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

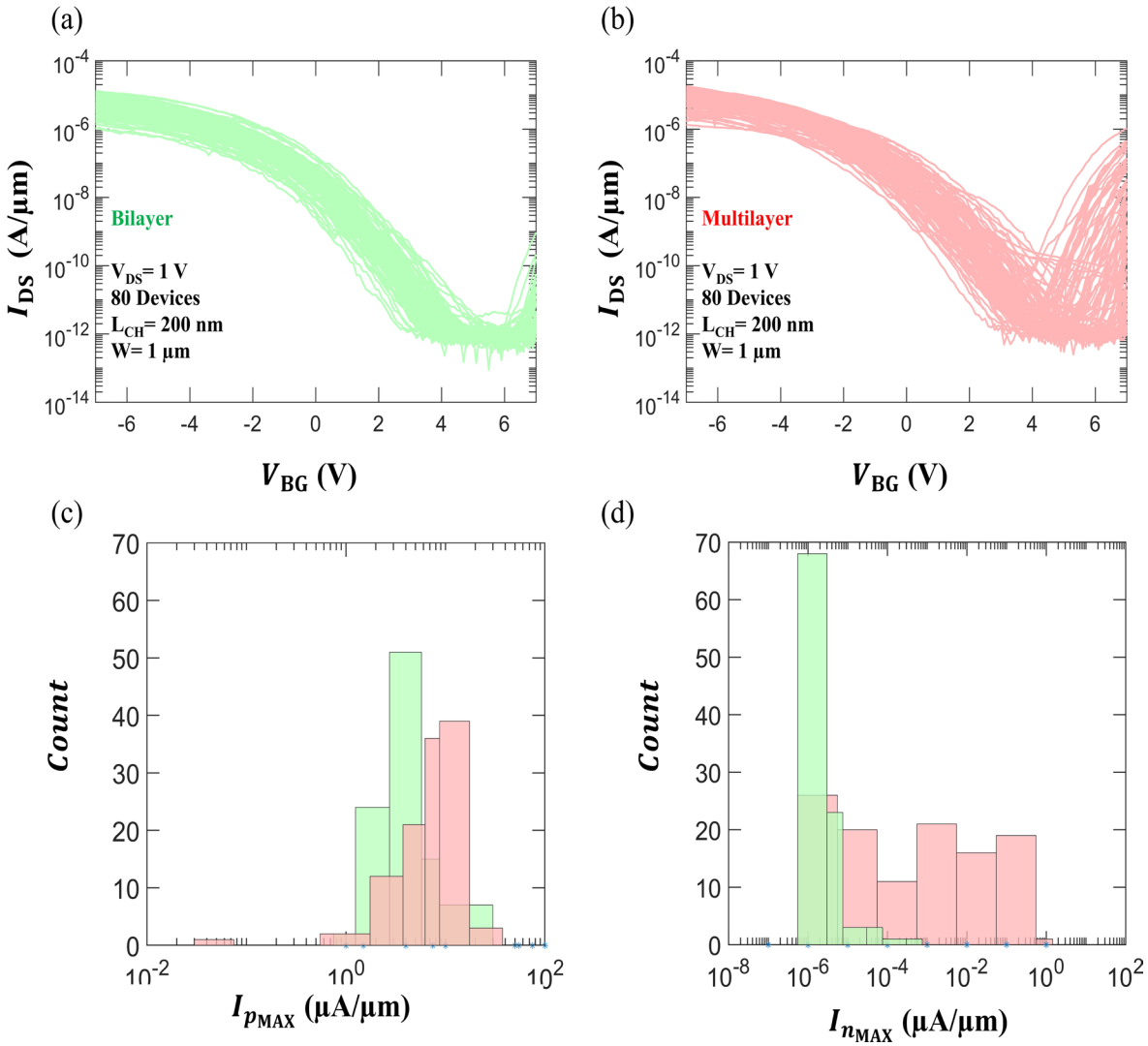
Extended data is available for this paper at https://doi.org/10.1038/s41565-024-01705-2.

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41565-024-01705-2.

Correspondence and requests for materials should be addressed to Rahul Pendurthi or Saptarshi Das.

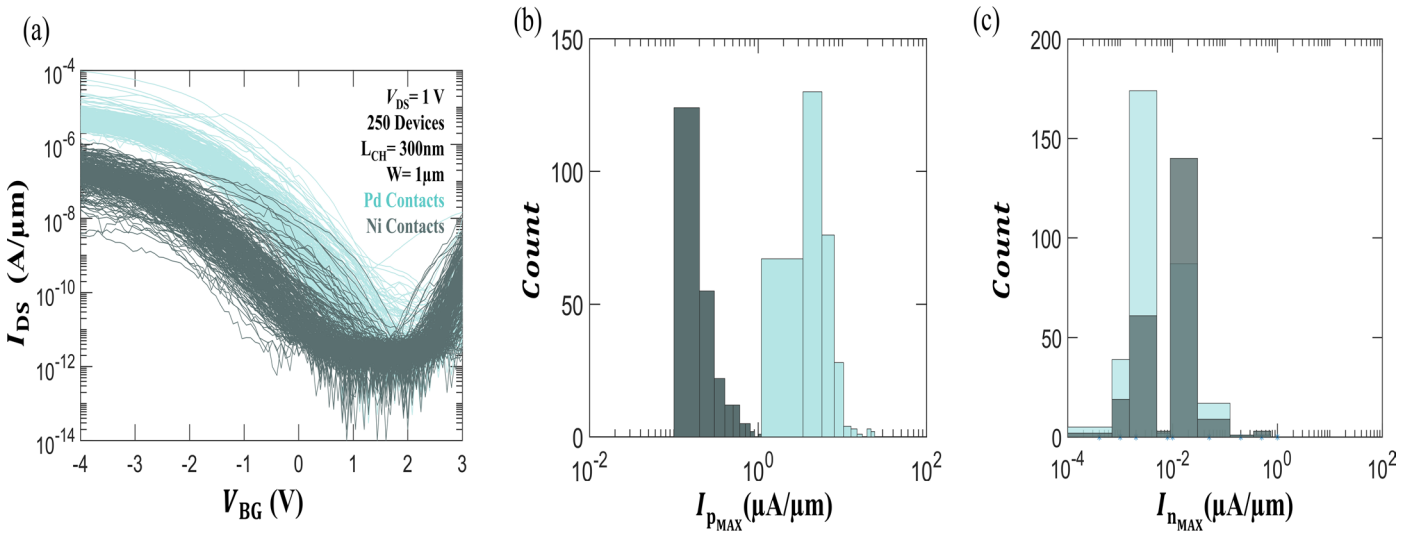
Peer review information *Nature Nanotechnology* thanks Wenzhong Bao, Yann-Wen Lan and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.

https://doi.org/10.1038/s41565-024-01705-2



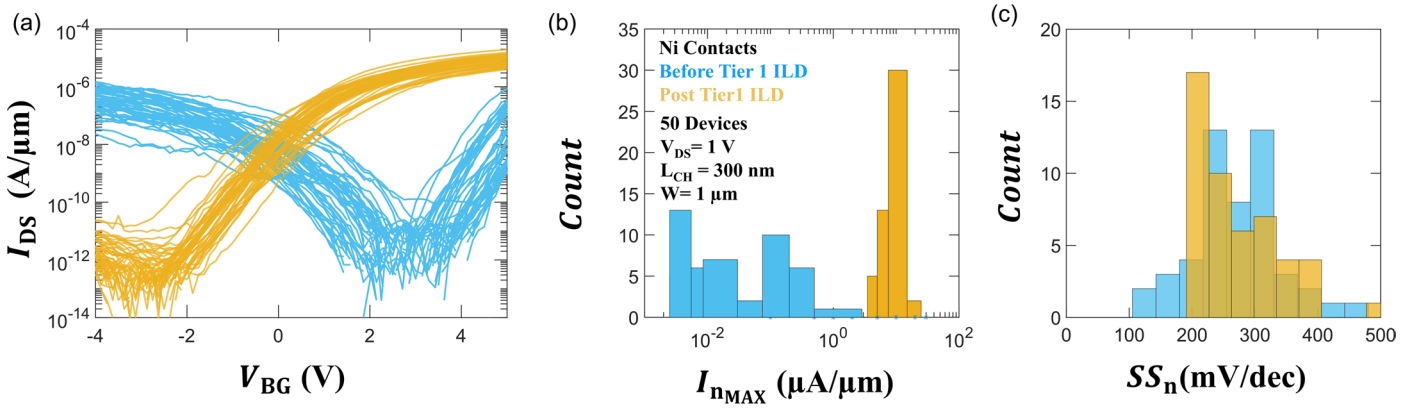
Extended Data Fig. 1 | Comparison of bilayer vs multilayer WSe_2. Transfer characteristics of FETs fabricated using **a**) bilayer, and **b**) multilayer WSe_2 films grown via MOCVD. Comparison of the extracted **c**) $I_{p_{MAX}}$ and **d**) $I_{n_{MAX}}$ for the FETs fabricated using bilayer and multilayer WSe_2.

https://doi.org/10.1038/s41565-024-01705-2



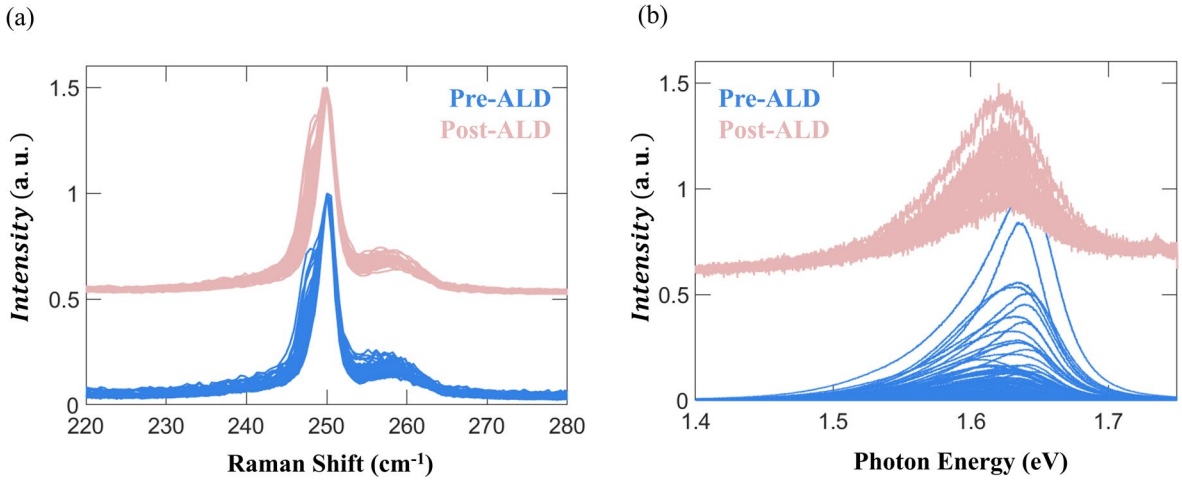
Extended Data Fig. 2 | Comparison of Pd vs Ni contacts. a) Transfer characteristics of 250 devices employing Pd and Ni contacts on WSe_2 FETs. Corresponding histograms comparing the **b**) $I_{p_{MAX}}$, and **c**) $I_{n_{MAX}}$ of the Pd- and Ni-contacted WSe_2 FETs.

https://doi.org/10.1038/s41565-024-01705-2



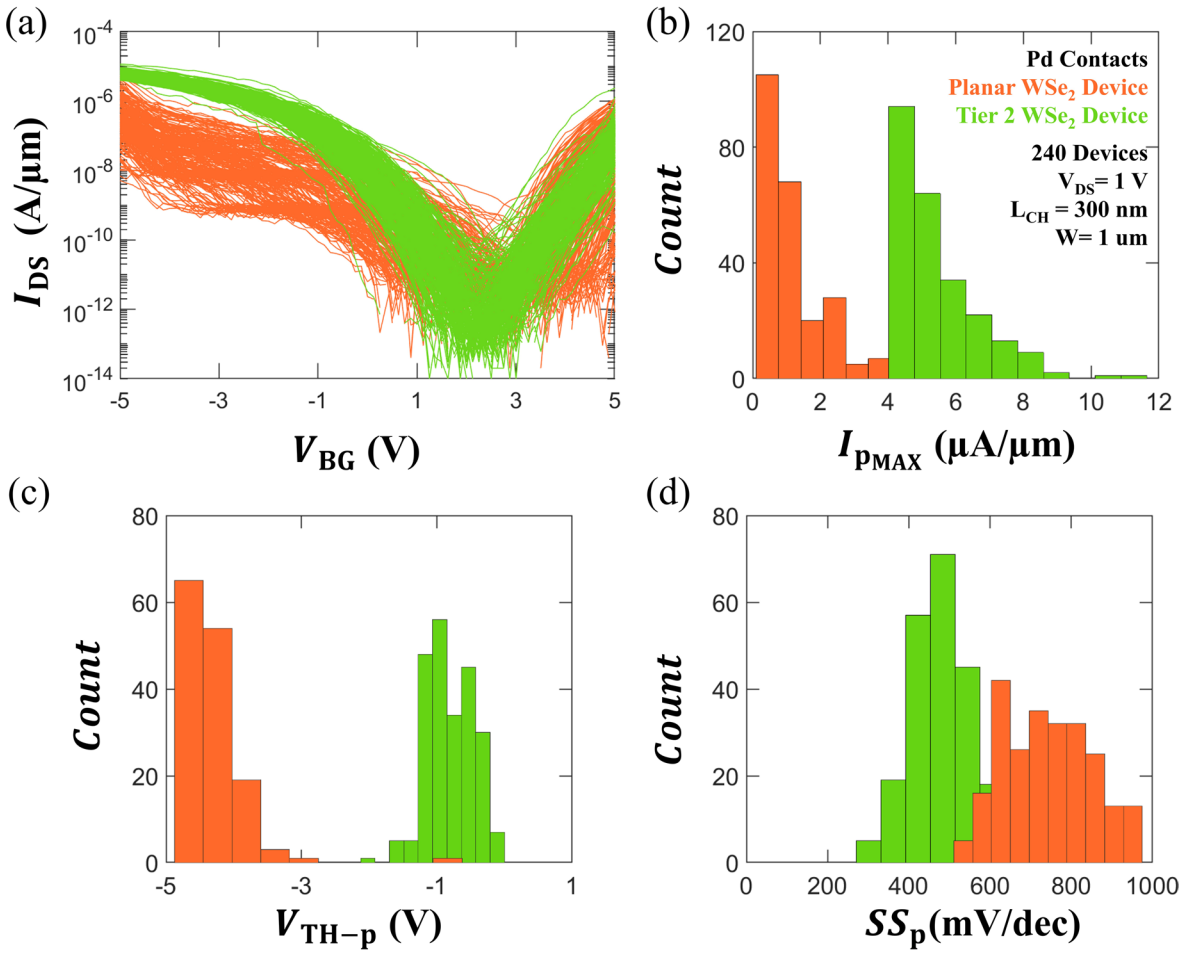
Extended Data Fig. 3 | Device performance with Ni contacts before and after ILD deposition. a) Transfer characteristics of 50 tier 1 WSe_2 FETs with nickel contacts before and after ILD deposition. The corresponding histograms show the change in **b**) $I_{n_{MAX}}$, and **c**) SS_n for both conditions. The observed improvement in IDS, shift in the $V_{TH\text{-}n}$, and lack of SS_n degradation confirms doping of the WSe_2 channel due to the deposition of the ILD.

https://doi.org/10.1038/s41565-024-01705-2



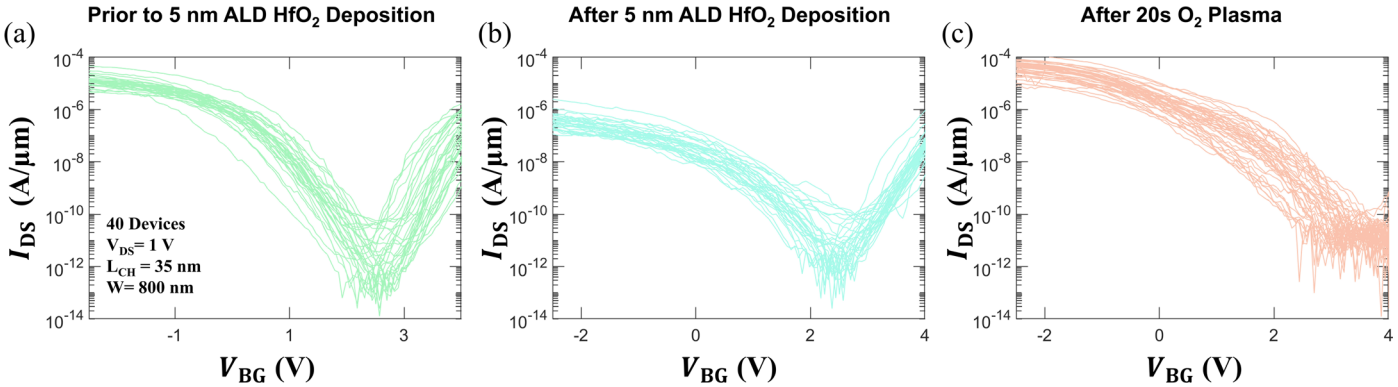
Extended Data Fig. 4 | Raman and PL before and after ALD. a) Raman and **b**) PL spectra of the WSe_2 film used in this study taken at 100 points across a representative 10 µm x 10 µm area before and after ALD of Al_2O_3.

https://doi.org/10.1038/s41565-024-01705-2



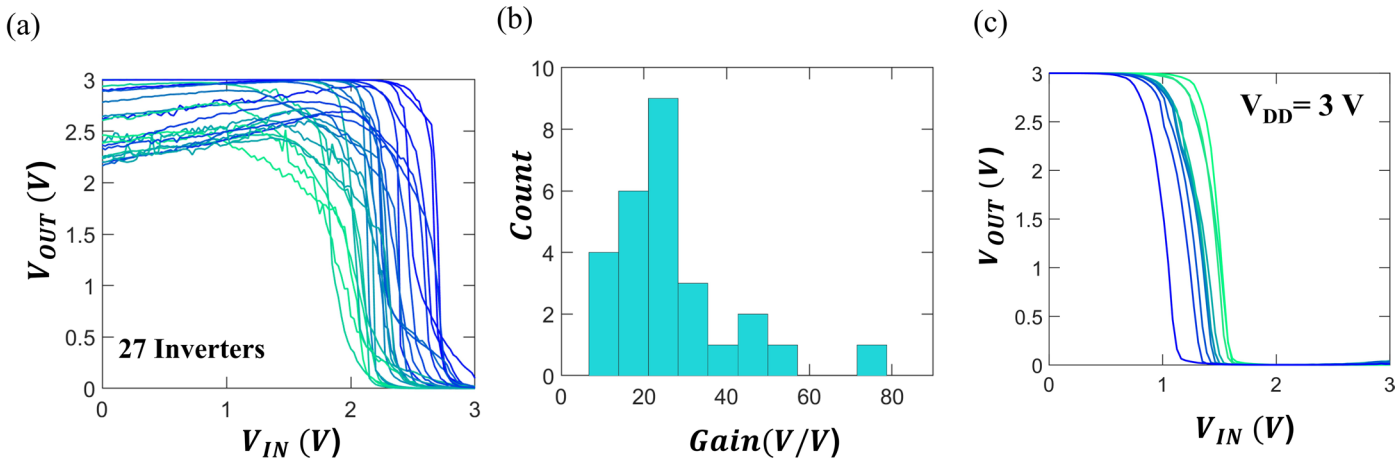
Extended Data Fig. 5 | Comparison of planar and Tier 2 WSe_2 Devices. **a**) Transfer characteristics of 240 planar and tier-2 WSe_2 FETs with Pd contacts. The corresponding histograms show the change in **b**) $I_{p_{MAX}}$, **c**) V_{TH-P}, and **d**) SS_p for both conditions. Devices fabricated on tier 2 outperform the planar devices, suggesting that the uniformity of growth and the transfer quality play a greater role in the performance and yield of devices.

https://doi.org/10.1038/s41565-024-01705-2



Extended Data Fig. 6 | Effect of HfO_2. Transfer characteristics of 40 WSe_2 FETs of L_{CH} = 35 nm and W = 800 nm **a**) before and **b**) after depositing 5 nm HfO_2, demonstrating a retention of p-branch characteristics and a lack of the n-doping that was observed during following deposition of Al_2O_3. **c**) Transfer characteristics of the HfO_2-capped WSe_2 after 20 s O_2 plasma exposure, demonstrating a retention of p-branch characteristics and a lack of the n-doping that was observed following the deposition of Al_2O_3. This approach thus enables further stacking of WSe_2 FETs beyond 2 tiers as well as customization of polarity type for each tier, based on the deposited ILD.

https://doi.org/10.1038/s41565-024-01705-2



Extended Data Fig. 7 | Inverter statistics. (**a**) Output characteristics of 27 M3D integrated inverters and **b**) the distribution of the peak gain achieved. **c**) The output characteristics of a programmable inverter, in which the inflection point can be modified based on the V_P applied.