

Ultra-low Power Analog Folded Neural Network for Cardiovascular Health Monitoring

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Abstract—Wearable sensors are increasingly used for continuous health monitoring, but their small size limits battery capacity, affecting user experience and monitoring capabilities. To overcome this, we introduce an ultra-low power analog Folded Neural Network (FNN) for physiological signal processing in a batteryless fashion. Our proposed FNN, by serializing computation, provides several benefits over traditional analog implementations, such as lower space, lower power consumption, and lower peak-to-average power ratio. We evaluate our method extensively using a dataset designed for ECG-based screening and diagnosis. Our analysis considers factors such as thermal noise, spatial requirements, and power consumption. Additionally, we evaluate detection performance, investigating various parameters of the proposed FNN. This evaluation provides insights into the optimal configuration for accurate anomaly detection. We observe a good trade-off for accuracy around 6 layers and a hidden size of 30 and further demonstrate that such architecture could be implemented in a wearable device and executed in a batteryless fashion.

Index Terms—Health Monitoring; Analog Neural Networks; Low Power Design; Wearable Computing; Distributed Sensing; Folded Neural Network.

I. INTRODUCTION

It is important to track and monitor our daily health data as it enables the identification of deviations from normal bodily patterns, facilitating early detection of diverse diseases in both clinical and pre-clinical environments. Early diagnosis is critical to preventing fatal conditions such as myocardial infarction and cardiomyopathy/heart failure [2], [3]. Wearable sensors offer a lightweight and affordable solution for tracking physiological markers, but simply collecting data is not enough. The data must be analyzed to provide meaningful insights into a person's health. Currently, most of this analysis is done on digital devices that receive data from wearable sensors, incurring high communication costs, leading to severe energy drain and low battery life of only 3 to 10 hours. To address this issue, we propose an ultra-low-power neural network folding approach on wearable devices to bypass the power consumed on data transmission and central computation.

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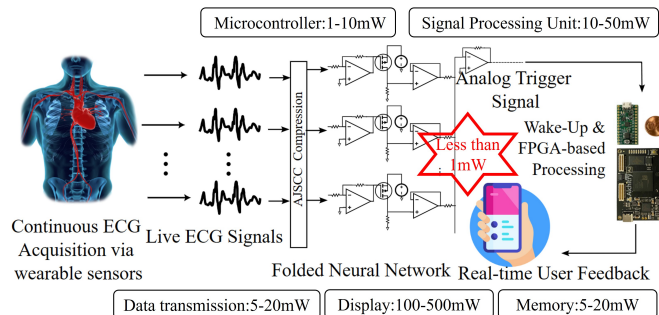


Fig. 1: Envisioned hybrid analog-digital architecture for 12-lead electrocardiogram (ECG) signal processing. Blocks represent the power budgets for conventional health monitoring. An ultra-low power Folded Neural Network (FNN) analyses the compressed Analog Joint Source-Channel Coded (AJSCC) [10] signals, with low False Negative (FN) rate while any False Positives (FP) are further analyzed by the digital system (woken up only when needed, i.e., *just in time*).

Background and Motivation: To facilitate the intelligent evaluation of physiological data, non-invasive continuous monitoring of patients using multiple wearable sensors is essential. Researchers have developed numerous non-invasive approaches to aid in screening by analyzing the body's physiological responses [4]–[7], complementing traditional diagnostic methods such as medical imaging and clinical tests. However, acquiring and analyzing these signals requires a Body-Area Network (BAN) with low-energy nodes capable of computation. In this direction, a two-tier wireless sensor network architecture has been proposed [8], [9], that we use as the underlying framework for our design (as shown in Fig. 1). The lower tier of this architecture consists of multiple smaller nodes sensing and evaluating physiological responses at various points in the body. The upper tier consists of a smaller number of cluster heads, such as mobile phones and medical devices, that compile the results from the smaller sensor nodes into meaningful information. This architecture leverages the higher processing power available in small digital handheld devices and the inexpensiveness of small sensor nodes to place multiple sensors on the body.

While the two-tiered approach presents a promising solution for BANs, it has some drawbacks in practice. One issue is the high communication cost associated with using only a few

cluster heads as central processing nodes, as it requires sending all data collected by the numerous sensors to the said cluster heads. Additionally, the nodes proposed in this approach, such as TelosB and Mote2, require batteries to be integrated into the design [11], leading to bulky, uncomfortable, and high-maintenance sensors.

Traditionally, the power budget for a wearable health monitoring sensor is distributed across various components as follows: the display, contingent on its type (e.g., OLED, LCD), may consume between 100 to 500 mW [12]; computing elements, including the Micro-Controller Unit (MCU) and signal processing unit, exhibit varying power requirements, with a low-power MCU consuming around 1 to 10 mW [13]; and the signal processing unit necessitating an additional 10 to 50 mW [14]. Flash memory, utilized for storing health data, is estimated to consume approximately 5 to 20 mW during read/write operations. Connectivity components, such as Bluetooth Low Energy (BLE) modules, typically consume between 1 to 10 mW during data transmission [15]. Consequently, the total power budget for the sensor may range from 120 to 600 mW, contingent on the specific components employed and their respective efficiencies, making it unfeasible for continuous monitoring on its own.

To address this issue, we propose a novel computation architecture for processing data onboard, referred to as Folded Neural Network (FNN). Our architecture reduces the space needed to implement and process complex neural networks in space- and resource-constrained sensors, thus bringing down the size and power consumption. By enabling local smart health monitoring on the sensor, we reduce communication between nodes and minimize the associated communication overhead. This concept is shown in Fig. 1 whereby intelligent analog sensors act as a continuous processing filter before the baton is passed on to a complex digital processor, yielding gains in both energy efficiency and continuity of detection. Bringing intelligence to the analog nodes makes the overall architecture energy efficient by reducing the need for batteries. This is evident as our proposed analog architecture consumes very low power (on the order of μ -Watts, consumed only for display or data transmission when needed) and could be powered by harvesting energy from environmental sources, such as patients' thermal heat or vibrations. Small energy harvesters working on thermo-electric principles have been shown to generate power in the order of hundreds of μ -Watts [16], [17], which could reliably power computational architectures requiring only a few μ -Watts to operate, thus eliminating batteries, and leading to further miniaturization and affordability of the sensor nodes.

Finally, while our approach for continuous physiological monitoring can be applied to many different applications, this article focuses on Electrocardiogram (ECG) as a case study. ECG is a well-established and widely used physiological signal that provides important information about the heart's function. As such, ECG is an ideal signal for continuous monitoring that can help in the early detection of heart problems and inform personalized treatment plans. Our focus on ECG allows us to demonstrate the potential of our approach in a specific and important context while also providing a starting point for

future work with other physiological signals and applications, like electroencephalogram (EEG), fitness tracking, or even the digital domain where resources available on smaller digital Field Programmable Gate Arrays (FPGAs) are constrained and could benefit from neural folding.

Our Contributions: This paper proposes and evaluates a low-powered, all-analog architecture that enables Neural Network (NN)-based computation for small, battery-less sensor nodes. Our contributions are:

- We propose a novel Folded Neural Network (FNN) architecture that enables complex NN-based analysis on sensor data by serializing computation on an analog chip.
- We demonstrate the practicality of our architecture for continuous monitoring by evaluating it on a publicly available dataset that involves ECG-based diagnosis and showcasing the ability to inform about potential anomalies.
- We detail a comprehensive noise analysis of our proposed architecture, showing the feasibility of its usage in a wearable sensor.
- We study the various trade-offs involving architectural design, the complexity of design, and the relevant power/energy consumption, and identify parameters for a batteryless operation.

Furthermore, the proposed FNN architecture refers to a hardware architecture for the low-resource (power, space) execution of feed-forward fully-connected neural network and should not be confused with Recurrent Neural Networks (RNNs), which describe a class of neural networks that include feedback in-between their layers due to which their output depends upon inputs presented earlier in time as well. This class includes Gated Recurrent Units (GRUs), Long Short-Term Memory (LSTMs), etc. [18]–[20] However, FNN does not implement recurrent networks and is, therefore, unrelated to this class.

Outline: This article is organized as follows: Sect. II positions our work with respect to related research; Sect. III explains our proposed two-step approach; Sect. IV evaluates our approach in both analog and digital domains, as well as in a hybrid manner; and Sect. V finally concludes the article.

II. RELATED WORK

We present here a brief overview of the literature closely associated with this article. Divided into three parts, the review starts with a brief foray into wearable sensor networks, leading to an exploration of the ECG signal processing domain, and finally ends with neural network processing in the analog domain.

Wearable Sensor Networks: The concept of a Wireless Sensor Network (WSN) is central in enabling a real-time monitoring system for any/all physiological signals [21]. Researchers have approached it by proposing ubiquitous healthcare networks [22] that incorporate both body-area-networks as well as wider wireless networks to enable continuous ubiquitous healthcare [23]. However, both proposed [21], [24] and implemented [25], [26] wearable WSNs have always moved the computation to the edge (digital) nodes paying little

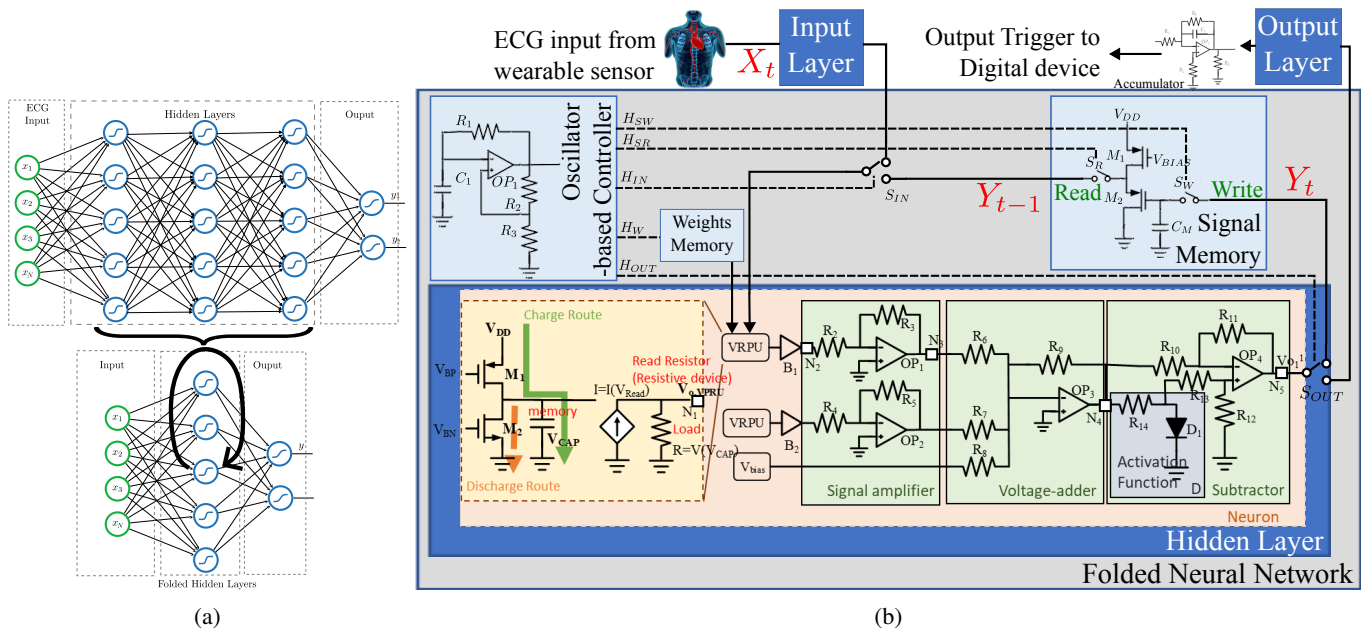


Fig. 2: (a) Illustration of the Folded Neural Network (FNN), and (b) its analog implementation. The controller is responsible for controlling the computation of hidden layers using the control signals H_{SW} , H_{SR} , H_{IN} , H_{OUT} , and H_W supporting write, read, input, output, weight-change operations respectively. The operational core of the NN is the VRPU array, building upon which we create the input layer, hidden layer, and output layer.

to no attention to the high communication costs incurred at the sensor-level, and hence, low battery-life and frequent need for recharging or replacement [23]. In this work, we target this neglected area and work towards an efficient in-situ processing scheme for low communication & power costs.

ECG Signal Processing: Changes in ECG have been linked to a wide range of conditions, such as congestive heart failure, arrhythmias [27], glycemic events [28], sleep apnea [29], Parkinson's [30], and even hypertension in general [31]. In order to successfully link ECG with the aforementioned conditions, multiple methods have been proposed including but not limited to time-frequency transforms [32], [33], Artificial Neural Networks (ANNs) [29], [34], and traditional classification algorithms such as Support Vector Machines (SVMs) [35], eigenvector decomposition [36], and hybrid signal processing [37]. However, the majority of these techniques are proposed from a signal processing point-of-view, making them unable to translate into a real-time signal processing scenario where resources are limited.

Analog Neural Processing: In order to bring efficiency to the processing of ECG signals, we propose analog signal processing architecture, situating this work closer to circuit design for signal analysis. Several architectures have been proposed, including Resistive Processing Units (RPUs) [38], memristive crossbar arrays [39], and various neural network designs [40]–[42]. In [38], we observed DC-drift at the output of each stage. To mitigate this issue, we suggested using a high pass filter at the output stage to eliminate the DC-drifts. In this vein, while architectures have been proposed, this is the first work that targets analog processing from a healthcare point-of-view and proposes a wearable-conscious fully-connected neural network analog design. We take into consideration

the required chip area, system-based accuracy for monitoring, effective wear time for the system, and power consumption to optimize our design for wearable health monitoring. By doing so, we aim to enhance the efficiency and effectiveness of ECG signal processing in the context of healthcare.

III. PROPOSED SOLUTION

As shown in Fig. 2, our Folded Neural Network (FNN) concept is based on the sequential processing of hidden layers. In this section, we present our approach in a bottom-up fashion, starting from a single neuron structure (see Sect. III-A), then moving on to detailing control structure for serialized computation (see Sect. III-B), and finally detailing how it comes together for FNN operation (see Sect. III-C).

A. VRPU-based Neuron

Given a weights matrix w , and an input vector x_{in} , an artificial neuron maps it to output $x_{out} = \sigma(w^T x_{in} + b)$, where b the bias vector, and σ represents a non-linearity. This model of a neuron is hence based on three major components: (i) multiplication, (ii) addition, and (iii) non-linearity. As shown in Fig. 2b, we implement multiplication using a Voltage-based Resistive-Programmable Unit (VRPU). Our proposed VRPU design involves a Voltage-Controlled Current Source (VCCS) offering several advantages: Firstly, it eliminates the need to precisely control the DC bias voltage on each node to ensure proper MOSFET operation; secondly, the operation of multiplication becomes more accurate. In contrast to earlier design [38], which used the gate and drain of PMOS as inputs for the RPU, the VCCS design reduces errors associated with multiplication outputs that are close to

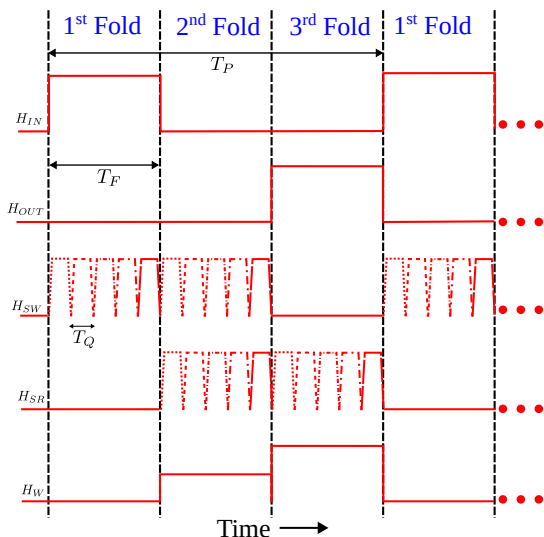


Fig. 3: Example oscillator output for 3 fold-FNN ($T_P = 3T_F$), and a temporal quantization of 5 ($T_F = 5T_Q$).

Parameter	Definition
L	Number of layers in the neural network
n_l	Number of neurons in the l^{th} layer
$W^{(l)}$	Weight matrix of the l^{th} layer
$b^{(l)}$	Bias vector of the l^{th} layer
$\sigma^{(l)}$	Activation function of the l^{th} layer
n_1	Number of neurons in the input layer
n_L	Number of neurons in the output layer
n_w	Width of the network (hidden-size)
T_F	Time taken to process one fold
$n_{l_{pf}}$	Layers processed per fold
n_F	Number of folds in one processing cycle
T_P	Processing time for one cycle
n_Q	Number of points sampled in the time window T_F
T_Q	Time in-between two consecutive samples
f_Q	Sampling/quantization frequency

TABLE I: Definitions of various parameters used for describing FNN architecture and function.

zero. V_{BP} and V_{BN} are network weights obtained by offline training and stored in the weights-memory, updated by each fold. These updates are detailed in Sect. III-B.

Furthermore, addition is implemented using an OpAmp-based voltage adder as shown in Fig. 2b. Finally, we implement two types of activation functions in this paper, namely Sigmoid, i.e., $\sigma(x) = \frac{1}{1+\exp(-x)}$ and Rectified Linear Unit (ReLU), i.e., $\sigma(x) = x \cdot [x > 0]$ using Diode-Pair (DP), and Diode-based (D) implementations [38], respectively. We take advantage of OpAmp-based design to acquire the voltage difference between two output nodes to read activation output.

B. Controller & Memory

For a fully connected neural network with L layers, let $x^{(l)} \in \mathbb{R}^{n_l}$ be the input feature vector of the l^{th} layer, where n_l is the number of neurons in that layer. The output of the l^{th} layer is given by $y^{(l)} = \sigma^{(l)}(W^{(l)}x^{(l)} + b^{(l)})$, where $W^{(l)} \in \mathbb{R}^{n_l \times n_{l-1}}$ and $b^{(l)} \in \mathbb{R}^{n_l}$ are the weight matrix and bias vector, respectively, of the l^{th} layer, and $\sigma^{(l)}$ is the activation function used in that layer. The input to the first layer is the input feature vector, i.e., $x^{(1)} = x$, and the output of

the last layer is the output of the neural network, i.e., $y^{(L)} = y$. For FNN, 1^{st} and L^{th} are considered input and output layers, with $n_1 = 12$ and $n_L = 2$ for 12 ECG input leads and 2 classification outputs, respectively. Lastly, to facilitate folding, $n_l = n_w, l \in \{2, 3, \dots, L-1\}$, where n_w is the width of the network (hidden-size).

Folding multiple hidden layers into sequential computation requires careful temporal orchestration. The most basic component of folded computation is a single fold. Let the time taken to process on fold be T_F , which also denotes the time-window of ECG signal processed at once and can involve either single or multi-layer computation, denoted by $n_{l_{pf}}$ (layers processed per fold). $n_{l_{pf}}$ depends on the realized circuit design and cannot be changed once implemented. One processing cycle—through the whole network—requires n_F folds, resulting in a processing time of $T_P := n_F T_F$. Lastly, propagation of signals through multiple folds requires saving the continuous temporal signal into discrete memory in-between folds, resulting in temporal quantization, as only a finite number of points (n_Q) can be sampled from a signal in the time window T_F . Hence, quantization time T_Q is related to the T_F as $T_F = n_Q T_Q$, with sampling/quantization frequency (f_Q) being $1/T_Q$, relating to how accurately we read/write the temporal input in between folds. A concise description of each parameter is also described in Table I for clarity.

As the weights and inputs in the VRPU are voltage-controlled, we use a capacitor as the basic memory element. We implement two types of memory: signal-memory and weights-memory. These memories are arrays of capacitors read/written by signals from the controller. The controller uses five signals, namely, H_{IN} , H_{OUT} , H_{SW} , H_{SR} , and H_W for executing input, output, write, read, and weight-change operations respectively (see Fig. 2). H_{IN} controls the tri-state switch S_{IN} , and is HIGH (connecting to 1^{st} layer output) for the first fold and LOW (connecting to feedback) for all other folds in a processing cycle. H_{OUT} controls the tri-state switch S_{OUT} , and is HIGH (connecting to L^{th} layer input) for the last fold and LOW (connecting to feedback) for all other folds in a processing cycle. H_{SW} controls write-operation to signal memory and is a bus composed of n_Q signals, each controlling an individual capacitor in the memory. The bus writes to n_Q capacitors sequentially during each fold except the last (when output is directed to the L^{th} layer input). Similarly, H_{SR} controls read-operation from signal-memory and is also a n_Q -wide bus. It reads from capacitors sequentially during each fold except the first (when input is obtained from 1^{st} layer output). Finally, H_W changes between n_F discrete levels during the processing window T_P , to load the weights $W^{(l)}$ from the weights-memory to the folded network to further control V_P and V_N in the Fig. 2 in VRPU at the gates of the left two transistors. The number of weights loaded for one fold is $n_{l_{pf}} \times n_w \times n_w$. A sample output for controller signals is shown in Fig. 3 for $n_F = 3$ and $n_Q = 5$.

C. Folded Neural Network (FNN)

The base components, i.e., neuron, controller, and memory, form the FNN architecture, as shown in Fig. 2b. Apart from

TABLE II: Accuracy Comparison of Neural Network Architectures with PhysioNet 2020 Challenge Dataset [43].

Model	Accuracy (%)	Feature Extraction
Deep transformer NN [44]	53	No features
Deep CNN [45]	66	CNN
Analog FNN (This work)	67	No features
P-QRS CNN [46]	74	P-QRS CNN
Bi-LSTM [19]	93	Bi-LSTM
LSTM [20]	94	LSTM

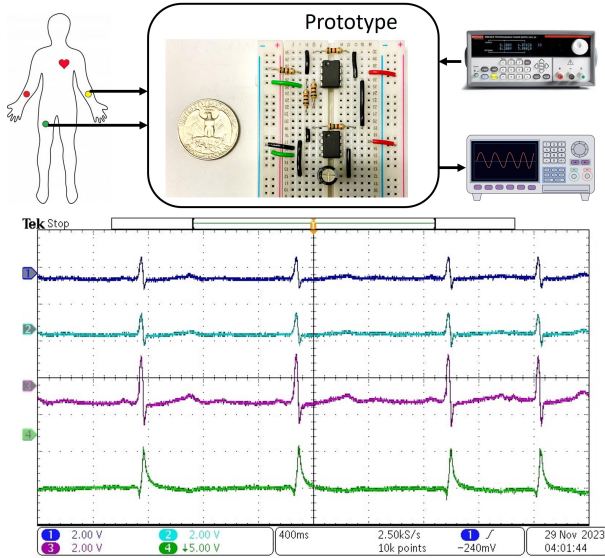


Fig. 4: Integration of dual ECG sensing inputs into a single neuron-accumulator analog classifier prototype in the experiment. CH1: The ECG signal from Sensor 1; CH2: The ECG signal from Sensor 2; CH3: The summation of CH1 and CH2; CH4: The accumulation of CH3 in the time domain.

the folded hidden layers for sequential computation, the 1st and L^{th} layers are special as they are not folded (see Fig. 2a). Furthermore, all layers except the output layer use the Sigmoid non-linearity—implemented using Diode-Pair (DP) design—, while the output layer uses an accumulator on the temporal signal to get the final decision trigger for the digital network. The 2 outputs refer to the classification between a normal or abnormal ECG signal. If the accumulated first output is greater than the second, the result is deemed normal, otherwise, it is considered abnormal, and the digital system is triggered.

Using a folded neural network approach, we save space by a factor of $\sim n_F$, with the overhead of the implementation of signal-memory (n_Q memory-elements) and the controller. At the same time, we effectively only observe the underlying ECG signal for a fraction of $1/n_F$ times, resulting in ‘continual’ monitoring instead of ‘continuous’. Furthermore, during sampling for multi-fold processing, temporal quantization is incurred with an error directly proportional to $1/n_Q$. In this article, we examine the performance trade-offs associated with each of these network parameters, including but not limited to optimal network width n_w , accuracy, F1-score, power consumption, and layers-per-fold (n_{lpf}).

IV. PERFORMANCE EVALUATION

In this section, we first show prototype of our proposed circuit in Sec. IV-A and justify the fully-connected architecture choice in use using Python training/simulation results (see Sect. IV-B). Further we use SPICE to evaluate parameters of the FNN architecture, the noise buildup with multiple-folds, and finally the interplay between power, space, performance for the analog architecture (see Sect. IV-C).

A. Prototyping

We have realized the fundamental prototype of an analog classifier, as shown in Fig. 4. This prototype encompasses the essential functions related to the addition of signals from different ECG sensors and their accumulation over time. The circuit of this prototype represents a neuron paired with an accumulator. CH1 corresponds to the ECG signal from sensor 1 multiplied by weight 1, CH2 corresponds to the ECG signal from sensor 2 multiplied by weight 2, CH3 represents the sum of the ECG signals from sensors 1 and 2, and CH4 illustrates the waveform obtained after the time accumulation of the CH3 signal. In our experimental setup, we utilized the signal generator model AFG1022 to generate ECG signals from a database. The computational power was supplied by the power supply unit 2231A-30-3, and the signals were observed using the MDO3024 oscilloscope.

B. Detection Performance

We present here the results of various metrics concerning the detection performance of FNN. This subsection starts with the description of our experimental setup, follows with a comparison with the State-Of-The-Art (SOTA) techniques, and finally ends with a detailed architectural search of our proposed design.

Experimental Setup: We use a publicly accessible dataset published under PhysioNet 2020 challenge for the classification of 12-lead ECGs [43]. The whole dataset for this challenge includes multiple sub-datasets collected from disparate sources, covering multiple geographic regions, age, and gender indices, making it a good candidate for the evaluation of our proposed architecture. The dataset contains a total of 43,101 recordings out of which 20,177 are collected from females and 22,849 are collected from males. Furthermore, 698 recordings are from ages 0–20, 5,172 from ages 20–40, 14,640 from ages 40–60, 19,115 from ages 60–80, and 3,295 from people aged 80 or above. In total, the dataset is divided into 27 classes (26 diseases and 1 normal class), which we use for the evaluation of the digital part, while we only divide the dataset into 2 classes (normal and abnormal) for the evaluation of the analog circuit. Finally, the PyTorch library was used, and the experiments were run on a Dell Precision 7920 workstation.

Comparison with SOTA: We compare our proposed network with several other related works. Table II presents this comparison in detail vis-a-vis accuracy metrics on PhysioNet 2020 challenge dataset [43]. The Deep Transformer Neural Network [44] achieves an accuracy of 53% without performing feature extraction. The Deep CNN [45], utilizing CNN for

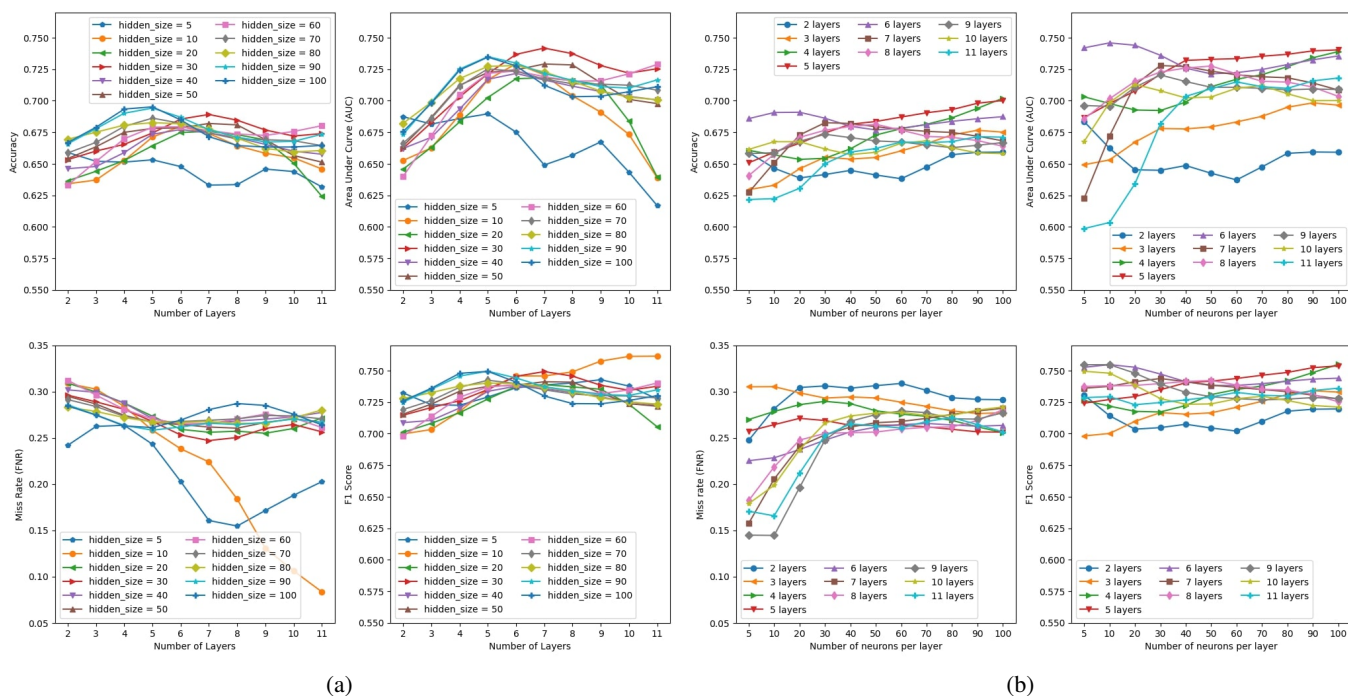


Fig. 5: Performance metrics of our proposed fully-connected neural network architecture in terms of Accuracy, AUC, miss rate, and F1-scores visualized along (a) number of layers, and (b) hidden-size (n_w). We observe that we get a good trade-off for accuracy around 5 layers and a hidden size (n_w) of 30.

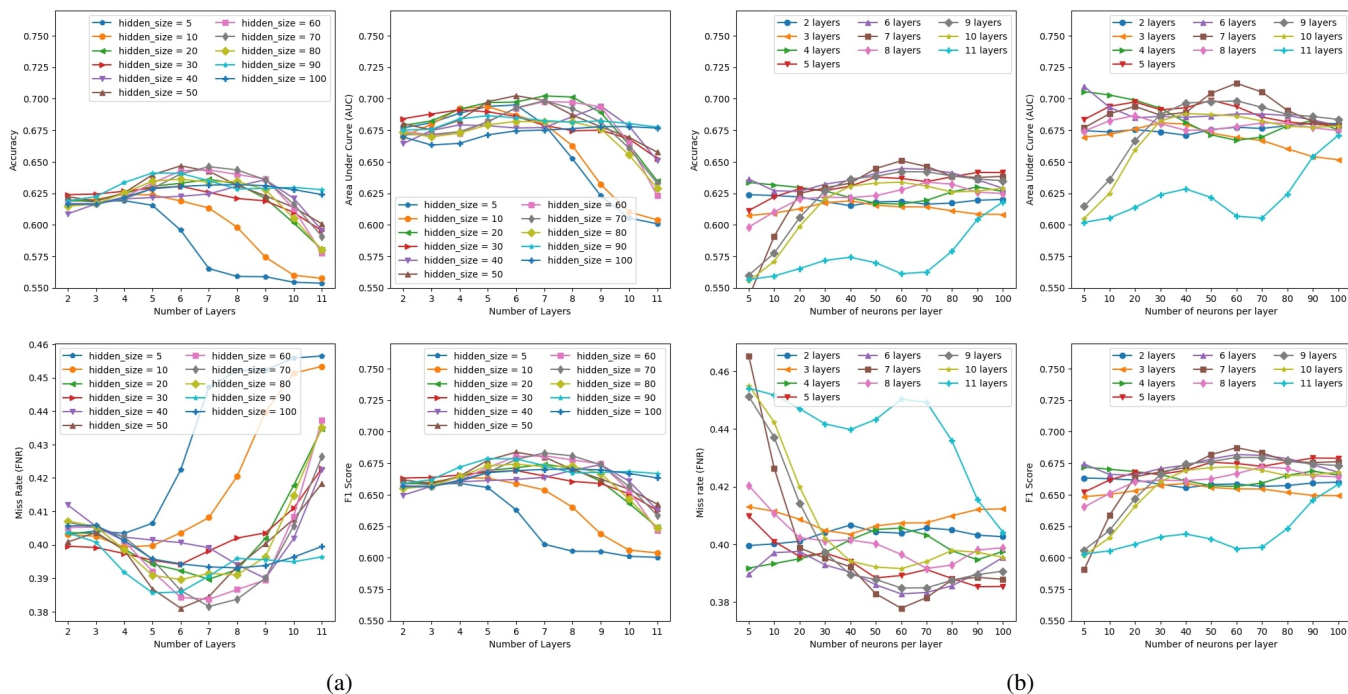


Fig. 6: Performance metrics of our proposed fully-connected neural network on a compressed signal using AJSCC-based [10] 2:1 compression. Results are shown in terms of Accuracy, AUC, miss rate, and F1-scores, visualized along (a) number of layers and (b) hidden size (n_w).

simple feature extraction, achieves a performance accuracy of 66%. The P-QRS CNN [46] employs CNN training specifically designed for P and QRS signals in ECG, resulting in an improved accuracy of 74%. Advanced Bi-LSTM and LSTM

methods [19], [20], when used for feature extraction, achieve an accuracy of over 93%. Our proposed approach, on the other hand, takes into account the various energy considerations that go into real-time in-situ processing on wearable sensors with

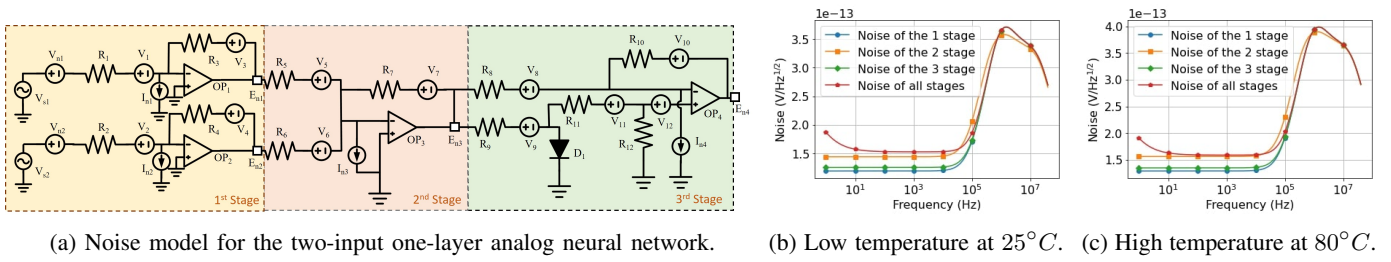


Fig. 7: (a) First stage is the signal amplifier, the second stage is the voltage adder, and the third stage is the activation function

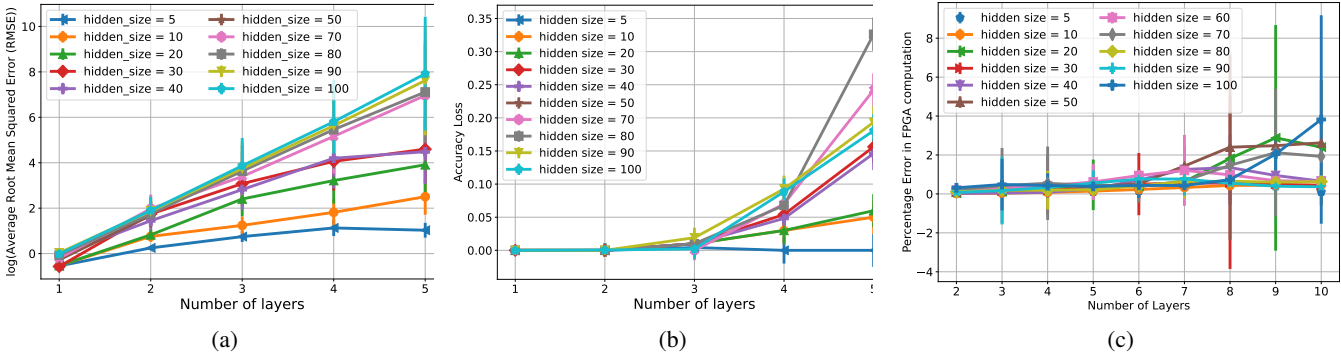


Fig. 8: (a) The natural log of the Root Mean Squared Error (RMSE) as the digitally-trained weights are implemented in analog circuit, simulated via SPICE (ngpsice 36). We observe that a marked increase in error is seen in higher layers as the number of neurons go above 50 neurons per layer; (b) The average accuracy loss due to added noise because of execution on analog circuit. The neural network is resilient to smaller noise levels, leading to only a small accuracy loss in smaller networks. (c) Percentage error in execution when the designed digital network is executed on tinyFPGA with a fixed-point width of 16. The error is more pronounced for a greater number of layers, but tolerable (within 5%) for up to 7 layers of computation.

compatible accuracy. Furthermore, the principal function of our proposed FNN is not to replace digitally implemented signal processing, but rather to act as a pre-filter for reducing power consumption, hence, even a lower—but acceptable—detection performance should suffice. Overall system could be made better by using a more complex digital implementation while relying on analog to filter out most normal signals.

Neural Architecture Analysis: We perform a combinatorial analysis of our proposed architecture based on the parameters of our proposed architecture, namely a number of layers (L) and hidden size (n_w). In a folded neural network, the decision to fold layers does not have a direct impact on the theoretical performance of an unfolded version of the network, as the performance is degraded because of noise introduced during multiple passes due to the reading/writing of voltage signals and leakage currents. Therefore, these simulations can be understood as a feasibility analysis for training a fully-connected neural network to detect if an abnormality exists in a given ECG signal. Fig. 5 shows the performance metrics accuracy, Area Under Curve (AUC), miss-rate, and F1-score for various hidden sizes and several layers. For Fig. 5a, we observe that performance increases for around 5 layers (increasing network capacity) but then stagnates. Similarly, looking at Fig. 5b, we conclude that a hidden-size (n_w) of 30 shows the best performance.

We repeat this combinatorial analysis for compressed signals using AJSCC [10] (2:1 ratio), as shown in Fig. 6, showing that the machine-learning approach is compatible

with compression as well, and can be used to save space & energy during the implementation in the analog domain. We do observe a slight drop in performance ($\sim 5\%$ in terms of accuracy) but gain space-saving in terms of the input layer, where the size of weights-matrix is reduced to $n_w \times 6$ from the original size of $n_w \times 12$, resulting in $2\times$ less space required for the implementation of the input layer.

C. Analog Noise, Space and Energy Analysis

In this sub-section, we present our analysis and discussion of various considerations for noise, space, and energy usage of our design.

Noise Analysis: To gain insights into the robustness of our design against noise, we created a design space using LTSpice software. This involved evaluating the output voltage noise and taking into account all significant noise sources. To validate our calculations, we compared them to the results obtained from simulating the circuit model. The noise energy of a two-input one-layer neural network (divided into three stages) can be expressed as (see Fig. 7a): For the first stage,

$$E_{n1}^2 = I_{n1}^2 (R_3 || R_1)^2 + \frac{R_3^2}{R_1^2} (V_{n1}^2 + V_1^2) + V_3^2. \quad (1)$$

$$E_{n2}^2 = I_{n2}^2 (R_4 || R_2)^2 + \frac{R_4^2}{R_2^2} (V_{n2}^2 + V_2^2) + V_4^2. \quad (2)$$

For the second stage,

$$E_{n3}^2 = I_{n3}^2(R_5||R_6||R_7)^2 + \left[\frac{R_7^2}{R_5^2}(E_{n1}^2 + V_5^2) + \frac{R_7^2}{R_6^2}(E_{n2}^2 + V_6^2) \right] + V_7^2. \quad (3)$$

For the third stage, assuming diode D_1 is forward-biased,

$$E_{n4}^2 = I_{n4}^2(R_8||R_{10})^2 + \frac{R_{10}^2}{R_8^2}(E_{n3}^2 + V_8^2) + V_{10}^2 + \frac{V_9^2}{R_9^2}(R_9||R_{11}||R_{12})^2 + \frac{V_{11}^2 + V_{12}^2}{R_{11}^2}((R_9 + R_{11})||R_{12})^2 + V_{n3}^2. \quad (4)$$

Assuming diode D_1 is reverse-biased,

$$E_{n4}^2 = I_{n4}^2(R_8||R_{10})^2 + \frac{R_{10}^2}{R_8^2}(E_{n3}^2 + V_8^2) + V_{10}^2 - \frac{V_9 + V_{11}}{R_9 + R_{11}}(R_9 + R_{11}||R_{12})^2 + V_{n3}^2. \quad (5)$$

Considering the above-mentioned equations and simulation results as shown in Fig. 7, we have found that the second stage is the most susceptible to noise in the low-frequency bandwidth among the three stages. This is expected as the third stage adds onto the fluctuations it receives from the earlier stages, although there is a difference in the noise analysis depending on whether the diode D_1 is forward-biased or reverse-biased, as derived in (4) and (5), respectively.

Apart from the theoretical noise-model analysis, we also performed circuit simulations via SPICE (ngspice 36) software to evaluate the impact of noise on the analog circuit empirically. Figs. 8a and 8b show the natural log of the Root Mean Squared Error (RMSE) as the proposed circuit is simulated in SPICE for a different number of layers and hidden size, and the associated accuracy loss, respectively. The proposed network yields quite low error for networks with a hidden size smaller than 50, cementing its feasibility for execution in analog. Furthermore, the accuracy loss for networks with 4 layers is within 10% demonstrating the robustness of the associated network. Finally, in Fig. 8c, we also evaluate the errors incurred as the network would be implemented on a small digital node (using FPGA). The associated error is always within 10% for computation with a fixed-point width of 16, meaning that our network is amenable to execution on smaller digital nodes as well, with tolerable error and a very small associated accuracy loss.

Furthermore, the FNN's noise tolerance, when folded, is assessed through a process that involves storing the output in a capacitor array after each fold and then reading it back into the recurrent path. This mechanism introduces a natural capacitor discharge effect as analog signals are stored and retrieved. The effect becomes more pronounced with each fold, leading to a gradual decay of the signals over time, reducing the noise tolerance of the hidden-layer computation. To assess this tolerance, in Fig. 9, we present the signal-to-noise ratio (SNR), space occupation, and power consumption analysis. Fig. 9a shows SNR across multiple folds for four different noise levels. At the output, we can observe that as

we take FNN with one layer per fold ($n_{lpf} = 1$), the noise ratio to the original signal increases with each fold. When a larger capacitance is used to implement signal memory, also known as a lower angular frequency (higher RC time constant), the SNR at the second layer experiences a faster drop after the first fold. However, the rate of dropping slows down during the second fold. Conversely, a smaller capacitor improves noise tolerance during the second fold. For the higher angular frequency, as the number of folds increases, the SNR significantly drops, which is undesirable, and the SNR noise ratio becomes more unstable, as shown in the error bar. On the other hand, when we recurrently add two layers at a time ($n_{lpf} = 2$), as the SNR of each layer shown in Fig. 9b, the SNR remains unaffected between the first and second layers. Between the third and fourth layers, it is notable that the SNR slightly drops compared with the third layer. The SNR only drops significantly during each fold. In this case, a smaller capacitor also results in a lower SNR.

Device mismatch considerations: The analysis of ECG signals (0.05–150 Hz) permits the neglect of device mismatch effects on opamps, NMOS, and PMOS due to low operational frequency. Meanwhile, we did not utilize signal amplification that also effectively reduces the impact of mismatch. To support the statement, the small-signal AC voltage gain of a differential pair in an analog circuit can be expressed as $A_v = \frac{g_m \cdot r_o}{2}$, where g_m is the transconductance of each transistor, and r_o is the output resistance of each transistor [47]. Introducing device mismatch by representing g_m and r_o as random variables, we have $g_m = g_0 \cdot (1 + \Delta_g)$ and $r_o = r_{o0} \cdot (1 + \Delta_{r_o})$, where g_0 is the nominal transconductance, Δ_g is a random variable representing the relative variation in g_m , r_{o0} is the nominal output resistance, and Δ_{r_o} is a random variable representing the relative variation in r_o . Substituting these expressions into the voltage gain equation, we obtain,

$$A_v = A_{v0} \cdot (1 + \Delta_g) \cdot (1 + \Delta_{r_o}), \quad (6)$$

where A_{v0} is the nominal voltage gain. The equation derived shows how device mismatch introduces variations in the voltage gain of the circuit. At low frequencies, the DC operating point of the circuit becomes more dominant. Since device mismatch is often more pronounced in AC or dynamic conditions. The variations are assumed to be small (Δ_g and Δ_{r_o}) in the case, the impact of device mismatch on A_v is relatively minor.

Space and Energy Consumption: In our design, capacitors are the largest devices, with the most important parameter to consider being capacitance density for manufacturing. Murata Manufacturing Co., Ltd. has recently started producing two new multi-layer ceramic capacitors for automotive applications. The first capacitor, NFM15HC105D0G3, is the world's smallest three-terminal low-equivalent series inductance (ESL) multilayer ceramic capacitor, measuring only 0402 inches (1.0×0.5mm). The second capacitor, NFM18HC106D0G3, has the highest capacitance for a three-terminal low-ESL multilayer ceramic capacitor, providing 10μF in the compact size of 0603 inches (1.6×0.8mm). By utilizing Murata's thin-layer technology and high-precision lamination technology, the NFM15HC105D0G3 is 60% smaller in volume com-

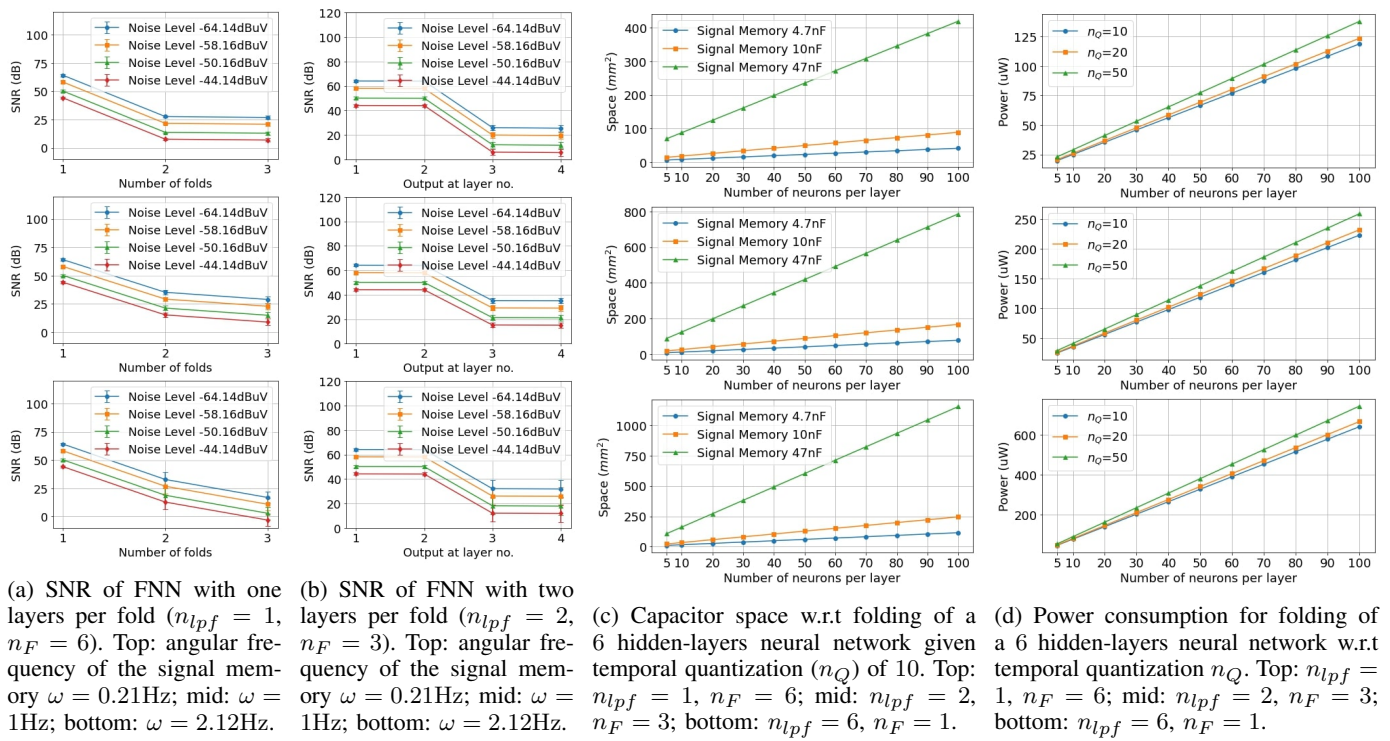


Fig. 9: Signal to noise ratio, space occupation, and power consumption analysis.

pared to their conventional products with the same capacitance. The NFM18HC106D0G3 has a capacitance ten times higher than similar-sized conventional products. The density is $128\text{nF}/\text{mm}^2$, which we use for the following demonstrations. Considering the integration of analog components within the analog chip, it becomes apparent that capacitors dominate in terms of space utilization. In Fig. 9c, the space occupation of a capacitor is illustrated for various sizes of hidden layers (n_w). Observing the results, we find that the space occupation is directly proportional to the number of neurons per layer. The difference in space occupation between the 4.7nF and 10nF capacitors is minor but significantly smaller than that of the 47nF capacitor. This indicates that larger capacitors require more physical space within the circuit. Comparing different n_{lpf} , we can observe that folding can save physical space. The larger number of n_{lpf} , the smaller space occupation for the same computation, albeit at the expense of continual monitoring interval. Moving on to Fig. 9d, we explore the power consumption in relation to the number of neurons per layer and the sampling number n_Q . Higher sampling resolution costs more power. Overall, these findings shed light on the relationship between signal-to-noise ratio, capacitor size, space occupation, and power consumption, providing valuable insights for circuit designers seeking to optimize their designs in terms of space utilization and power efficiency.

Batteryless Operation: As mentioned in Sect. I, the typical power budget of a digital wearable health monitoring sensor is 120 to 600 mW. However, by using the proposed analog pre-filter that requires less than 1 mW of power, we can reduce power consumption by 99% while being able to detect anomalies in ECG signals continuously. The digital part, comprising of screen display, MCU, and flash memory only

has to be woken up when a potential anomaly is detected. Furthermore, display or data transmission is only powered up on demand, enabling feasible operation without a bulky battery, which we explain in detail as follows.

A human movement energy harvester (silicon/quartz) at a frequency 2Hz [48] can have $40\mu\text{W}$ output power energy using a chip size $20\text{mm} \times 45\text{mm}$ (around the size of a wearable watch), with a maximum power density of $0.044\mu\text{W}/\text{mm}^2$. Assuming 16 hours (waking hours) of $40\mu\text{W}$ and 8 hours (sleeping hours) of 0W energy harvesting, our system can spend an average of $26.7\mu\text{W}$. Looking at Fig. 9d (Top), a fully-folded 6-layer network ($n_{lpf} = 1$; $n_F = 6$) with $n_Q = 20$, and a hidden-size (n_w) of 10, can be operated with an average power of around $25\mu\text{W}$. On the other hand, with a duty cycle of 50%, we can execute a fully-folded 6-layer network with a hidden size (n_w) of 30 with an equivalent average of $53\mu\text{W}$, which is one of the best performing neural network architectures as demonstrated in Fig. 5a. This operation is not possible with unfolded network architecture as it consumes more space (38.2mm^2) and more power ($202.15\mu\text{W}$)—as evidenced in Figs. 9c (Bottom), 9d (Bottom). Utilizing a supercapacitor, typically possessing an energy density ranging from $1 - 30\text{mWh/g}$, we can effectively store and deliver power for the circuit's operation. Therefore, our FNN approach reduces power consumption to enable batteryless operation. It can be argued, however, that a similar reduction in average power could be achieved by simply reducing the duty cycle by $6\times$, instead of folding $6\times$ as shown in Fig. 9d (Top). But the point of note here is that our folded approach consumes a steady low power (equal to average power) while decreasing the duty cycle leads to a peaky power consumption pattern (peak-to-average power ratio of 6), albeit with a similar

apparent monitoring interval. A higher peak power, hence, means a bigger supercapacitor, hindering a compact wearable design. Hence, our FNN is not only amenable to batteryless operation but is the only way to save enough space and power for continual monitoring.

D. Operational Speed

When it comes to designing analog/digital models of our proposed network, fine-tuning or training the weights is the most time-consuming task. Offline training as processed on an Nvidia RTX 2080 Ti GPU, takes around 47 seconds per epoch, whereby usually a training of 10–20 epochs is needed to achieve acceptable performance. These times signify the delay in training and designing new weights for updates in the device with new data. However, such updates are infrequent and done offline, meaning that for the real-time operation of the device, only delays relating to the digital and analog execution should be relevant. The analog operation showcases a markedly swifter processing speed in anomaly detection compared to its digital counterpart. By configuring various RC time constants to represent distinct charging/discharging intervals, as illustrated in Fig. 9a and Fig. 9b, a combination of a $4.7\mu F$ capacitor and $100k\Omega$ resistor results in an RC time constant of 2.95 seconds or a 2.12 Hz angular frequency. We observed its ability to encompass information over approximately 2.5 times the RC time constant, equivalent to 7 to 10 heartbeats, contingent on heart rate. The operational mode maintains acceptable SNR conditions. Crucially, this design ensures that the processing time remains at or below T_Q , thereby not affecting T_F and T_P , ensuring real-time signal processing, as evidenced by the prototype depicted in Fig. 4. Analog operation inherently operates in real-time, contrasting with digital processes that involve considerations of computational time.

V. CONCLUSION AND DISCUSSION

We proposed an ultra-low power analog design for physiological signal processing, utilizing an all-analog neural network architecture and a physical folding architecture with an analog oscillator as a timing signal. Our method eliminates the need for a battery and undergoes extensive evaluation using an ECG-based diagnosis dataset. We consider factors like thermal noise, spatial requirements, and power consumption. We also evaluate detection effectiveness, exploring hidden layer sizes and the number of layers. In the broader context of wearable monitoring, our FNN approach demonstrates significant potential beyond its current use for ECG monitoring. It can be expanded to encompass other monitoring applications like EEG monitoring, sleep monitoring, fitness tracking, and more. Additionally, it can be applied to cross-domain scenarios such as continuous computation in Radio-Frequency Identification tags (RFIDs), smart fabrics, implantable tattoos, tiny digital FPGA devices, and others. Overall, the FNN architecture proves beneficial in situations where resources are limited in terms of energy and space while necessitating continuous yet straightforward computation. There is, however, no free lunch,

as folding capability imposes limitations on the network structure, restricting the full utilization of recent advancements in neural network research in the analog domain. Further research is needed to incorporate powerful architectures like CNNs, Transformers, and others into the analog domain. This article represents the first step towards achieving low-powered analog neural network computation. Finally, although our current analog FNN prototype is built using commercially available components, resulting in a large size, future iterations will be designed as analog ICs, leading to a significant reduction in volume. This advancement will also allow for a substantial increase in the number of neurons and the complexity of the FNN.

REFERENCES

- [1] Y.-T. Hsieh, K. Anjum, and D. Pompili, "Ultra-low power analog recurrent neural network design approximation for wireless health monitoring," in *2022 IEEE 19th International Conference on Mobile Ad Hoc and Smart Systems (MASS)*, pp. 211–219, IEEE, 2022.
- [2] M. Saleh and J. A. Ambrose, "Understanding myocardial infarction," *F1000Research*, vol. 7, 2018.
- [3] A. A. Panju, B. R. Hemmelgarn, G. H. Guyatt, and D. L. Simel, "Is this patient having a myocardial infarction?," *Journal of the American Medical Association*, vol. 280, no. 14, pp. 1256–1263, 1998.
- [4] L. C. Cancio, A. I. Batchinsky, J. Salinas, T. Kuusela, V. A. Convertino, C. E. Wade, and J. B. Holcomb, "Heart-rate complexity for prediction of prehospital lifesaving interventions in trauma patients," *Journal of Trauma and Acute Care Surgery*, vol. 65, no. 4, pp. 813–819, 2008.
- [5] L. Chen, T. M. McKenna, A. T. Reisner, A. Gribok, and J. Reifman, "Decision tool for the early diagnosis of trauma patient hypovolemia," *Journal of biomedical informatics*, vol. 41, no. 3, pp. 469–478, 2008.
- [6] L. Chen, A. T. Reisner, T. M. McKenna, A. Gribok, and J. Reifman, "Diagnosis of hemorrhage in a prehospital trauma population using linear and nonlinear multiparameter analysis of vital signs," in *2007 29th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp. 3748–3751, IEEE, 2007.
- [7] V. A. Convertino, K. L. Ryan, C. A. Rickards, J. Salinas, J. G. McManus, W. H. Cooke, and J. B. Holcomb, "Physiological and medical monitoring for en route care of combat casualties," *Journal of Trauma and Acute Care Surgery*, vol. 64, no. 4, pp. S342–S353, 2008.
- [8] B. Chen, D. Pompili, and I. Marsic, "Continuous vital sign monitoring via wireless sensor network," *Proceedings of Malignant Spaghetti—Wireless Technologies in Hospital Healthcare*, 2008.
- [9] Y.-T. Hsieh, K. Anjum, S. Huang, I. Kulkarni, and D. Pompili, "Hybrid analog-digital sensing approach for low-power real-time anomaly detection in drones," in *2021 IEEE 18th International Conference on Mobile Ad Hoc and Smart Systems (MASS)*, pp. 446–454, 2021.
- [10] X. Zhao, V. Sadhu, A. Yang, and D. Pompili, "Improved circuit design of analog joint source channel coding for low-power and low-complexity wireless sensors," *IEEE Sensors Journal*, vol. PP, no. 99, p. 1, 2017.
- [11] R. Lajara, J. J. Pérez-Solano, and J. Pelegrí-Sebastiá, "Predicting the batteries' state of health in wireless sensor networks applications," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 11, pp. 8936–8945, 2018.
- [12] M. Rodriguez Fernandez, E. Zalama Casanova, and I. Gonzalez Alonso, "Review of display technologies focusing on power consumption," *Sustainability*, vol. 7, no. 8, pp. 10854–10875, 2015.
- [13] P. Mayer, M. Magno, and L. Benini, "Smart power unit—mw-to-nw power management and control for self-sustainable iot devices," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5700–5710, 2020.
- [14] S. Benatti, G. Rovere, J. Bösser, F. Montagna, E. Farella, H. Glaser, P. Schönlé, T. Burger, S. Fateh, Q. Huang, and L. Benini, "A sub-10mw real-time implementation for emg hand gesture recognition based on a multi-core biomedical soc," in *2017 7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, pp. 139–144, 2017.
- [15] A. Nikoukar, S. Raza, A. Poole, M. Güneş, and B. Dezfouli, "Low-power wireless for the internet of things: Standards and applications," *IEEE Access*, vol. 6, pp. 67893–67926, 2018.

- [16] Y.-W. Chong, W. Ismail, K. Ko, and C.-Y. Lee, "Energy harvesting for wearable devices: A review," *IEEE Sensors Journal*, vol. 19, no. 20, pp. 9047–9062, 2019.
- [17] M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, *Energy harvesting for self-powered wearable devices*. Springer, 2018.
- [18] Y. Yu, X. Si, C. Hu, and J. Zhang, "A review of recurrent neural networks: Lstm cells and network architectures," *Neural computation*, vol. 31, no. 7, pp. 1235–1270, 2019.
- [19] H. Yoo, J. Moon, J.-H. Kim, and H. J. Joo, "Design and technical validation to generate a synthetic 12-lead electrocardiogram dataset to promote artificial intelligence research," *Health Information Science and Systems*, vol. 11, no. 1, p. 41, 2023.
- [20] T. Mehari and N. Strodthoff, "Advancing the state-of-the-art for ecg analysis through structured state space models," *arXiv preprint arXiv:2211.07579*, 2022.
- [21] P. S. Pandian, K. P. Safeer, P. Gupta, D. T. Shakunthala, B. S. Sundershesu, and V. C. Padaki, "Wireless sensor network for wearable physiological monitoring," *Journal of Networks*, vol. 3, pp. 21–29, May 2008.
- [22] H. Viswanathan, B. Chen, and D. Pompili, "Research challenges in computation, communication, and context awareness for ubiquitous healthcare," *IEEE Communications Magazine*, vol. 50, pp. 92–99, May 2012. Conference Name: IEEE Communications Magazine.
- [23] M. M. Baig, H. Gholamhosseini, and M. J. Connolly, "A comprehensive survey of wearable and wireless ECG monitoring systems for older adults," *Medical & Biological Engineering & Computing*, vol. 51, pp. 485–495, May 2013.
- [24] J. Conway, A. Fernandes, C. J. Coelho, L. Andrade, D. da Silva, and H. Carvalho, "Wearable computer as a multi-parametric monitor for physiological signals," in *Proceedings IEEE International Symposium on Bio-Informatics and Biomedical Engineering*, pp. 236–242, Nov. 2000.
- [25] T. Walls, D. Pompili, and J.-P. Varkey, "Human motion recognition using a wireless sensor-based wearable system," Jan. 2012.
- [26] J. M. Peake, G. Kerr, and J. P. Sullivan, "A critical review of consumer wearables, mobile applications, and equipment for providing biofeedback, monitoring stress, and sleep in physically active populations," *Frontiers in Physiology*, vol. 9, 2018.
- [27] A. Choudhury, S. Vuppu, S. Pratap Singh, M. Kumar, and S. Nakharu Prasad Kumar, "ECG-based heartbeat classification using exponential-polynomial optimizer trained deep learning for arrhythmia detection," *Biomedical Signal Processing and Control*, vol. 84, p. 104816, July 2023.
- [28] M. Andellini, S. Haleem, M. Angelini, M. Ritrovato, R. Schiaffini, E. Iadanza, and L. Pecchia, "Artificial intelligence for non-invasive glycaemic-events detection via ECG in a paediatric population: study protocol," *Health and Technology*, vol. 13, pp. 145–154, Jan. 2023.
- [29] O. Faust, U. R. Acharya, E. Y. K. Ng, and H. Fujita, "A review of ecg-based diagnosis support systems for obstructive sleep apnea," *Journal of Mechanics in Medicine and Biology*, vol. 16, p. 1640004, Feb. 2016. Publisher: World Scientific Publishing Co.
- [30] T. H. Haapaniemi, V. Pursiainen, J. T. Korpelainen, H. V. Huikuri, K. A. Sotaniemi, and V. V. Myllylä, "Ambulatory ecg and analysis of heart rate variability in parkinson's disease," *Journal of Neurology, Neurosurgery & Psychiatry*, vol. 70, no. 3, pp. 305–310, 2001. Publisher: BMJ Publishing Group Ltd. eprint: <https://jnnp.bmj.com/content/70/3/305.full.pdf>.
- [31] M. Sharma, J. S. Rajput, R. S. Tan, and U. R. Acharya, "Automated detection of hypertension using physiological signals: A review," *International Journal of Environmental Research and Public Health*, vol. 18, p. 5838, Jan. 2021. Number: 11 Publisher: Multidisciplinary Digital Publishing Institute.
- [32] T. D. Pham, "Time–frequency time–space LSTM for robust classification of physiological signals," *Scientific Reports*, vol. 11, p. 6936, Dec. 2021.
- [33] M. C. Teich, S. B. Lowen, B. M. Jost, K. Vibe-Rheymer, and C. Heneghan, "Heart rate variability: Measures and models," Tech. Rep. arXiv:physics/0008016, arXiv, Aug. 2000. arXiv:physics/0008016 type: article.
- [34] O. Faust, Y. Hagiwara, T. J. Hong, O. S. Lih, and U. R. Acharya, "Deep learning for healthcare applications based on physiological signals: A review," *Computer Methods and Programs in Biomedicine*, vol. 161, pp. 1–13, July 2018.
- [35] A. Mishra, S. Bhusnur, and S. Mishra, "A neoteric parametric representation and classification of ecg signal," *Circuits, Systems, and Signal Processing*, Apr. 2023.
- [36] W. Zeng, J. Yuan, C. Yuan, Q. Wang, F. Liu, and Y. Wang, "A novel technique for the detection of myocardial dysfunction using ECG signals based on hybrid signal processing and neural networks," *Soft Computing*, vol. 25, pp. 4571–4595, Mar. 2021.
- [37] E. D. Übeyli, "Combining recurrent neural networks with eigenvector methods for classification of ECG beats," *Digital Signal Processing*, vol. 19, pp. 320–329, Mar. 2009.
- [38] Y.-T. Hsieh, K. Anjum, S. Huang, I. Kulkarni, and D. Pompili, "Neural network design via voltage-based resistive processing unit and diode activation function - a new architecture," in *The IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2021.
- [39] T. P. Xiao, C. H. Bennett, B. Feinberg, S. Agarwal, and M. J. Marinella, "Analog architectures for neural network acceleration based on non-volatile memory," *Applied Physics Reviews*, vol. 7, no. 3, p. 031301, 2020.
- [40] O. Krestinskaya, K. N. Salama, and A. P. James, "Learning in memristive neural network architectures using analog backpropagation circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 2, pp. 719–732, 2019.
- [41] K. Smagulova, K. Adam, O. Krestinskaya, and A. P. James, "Design of cmos-memristor circuits for lstm architecture," in *2018 IEEE international conference on electron devices and solid state circuits (EDSSC)*, pp. 1–2, IEEE, 2018.
- [42] T. W. Hughes, I. A. Williamson, M. Minkov, and S. Fan, "Wave physics as an analog recurrent neural network," *Science advances*, vol. 5, no. 12, p. eaay6946, 2019.
- [43] E. A. P. Alday, A. Gu, A. J. Shah, C. Robichaux, A.-K. I. Wong, C. Liu, F. Liu, A. B. Rad, A. Elola, S. Seyedi, et al., "Classification of 12-lead ecgs: the physionet/computing in cardiology challenge 2020," *Physiological measurement*, vol. 41, no. 12, p. 124003, 2020.
- [44] A. Natarajan, Y. Chang, S. Mariani, A. Rahman, G. Boverman, S. Vij, and J. Rubin, "A wide and deep transformer neural network for 12-lead ecg classification," in *2020 Computing in Cardiology*, pp. 1–4, IEEE, 2020.
- [45] P. Aublin, M. B. Ammar, N. Achache, M. Benahmed, A. El Hichami, M. Barret, J. Fix, and J. Oster, "Cardiac abnormality detection based on an ensemble voting of single-lead classifier predictions," in *2021 Computing in Cardiology (CinC)*, vol. 48, pp. 1–4, IEEE, 2021.
- [46] M. Bodini, M. W. Rivolta, and R. Sassi, "Classification of 12-lead ecg with an ensemble machine learning approach," in *2020 Computing in Cardiology*, pp. 1–4, IEEE, 2020.
- [47] S.-C. Huang, M. Ismail, and S. R. Zarabadi, "A wide range differential difference amplifier: A basic block for analog signal processing in mos technology," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 40, no. 5, pp. 289–301, 1993.
- [48] S. Roy, A. W. Azad, S. Baidya, M. K. Alam, and F. Khan, "Powering solutions for biomedical sensors and implants inside the human body: a comprehensive review on energy harvesting units, energy storage, and wireless power transfer techniques," *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12237–12263, 2022.