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Split-Capacitor-Based Isolated Double Step-Down DC-DC Converter

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***Abstract*—This paper introduces an isolated high step-down DC-DC converter with reduced voltage stress of power switches in the primary side. The introduced converter provides zero-voltage-switching turn-on for all power switches and avoids the transformer saturation problem. By using a split-capacitor double step-down structure, the introduced converter also reduces the input capacitance and eliminates the high voltage stress during the start-up process. The introduced converter is ready to be connected to a three-level neutral-point-clamped inverter with self-balanced voltages in two capacitors of the DC link. The theoretical analysis and comparative study of the introduced converter are presented in detail. A 1 kW 400-V/48-V laboratory prototype was implemented to validate the feasibility of the introduced converter.**

***Index Terms*—High step-down, phase-shift full-bridge converter, start-up, soft-switching, low voltage stress.**

I. Introduction

In recent years, the research on green energy and electric vehicles has become more attractive owing to their potential to reduce carbon emissions and global warming impacts. Many studies on new power converter topologies have been focused on improving conversion efficiency and reducing cost. High energy efficiency high-boost DC-DC converters are implemented in many photovoltaic and fuel cell applications [1]–[2]. Also, high-buck DC-DC converters are attractive in uninterruptable power supplies (UPS), light-emitting diode (LED) drivers, data centers, battery chargers, and power supplies for railways [3]–[6], which require low-voltage and high-current capabilities. In addition, AC-DC rectifiers including power factor correction and DC-DC converters with a high step-down capability, e.g., from 400 Vdc to 48 Vdc bus, are commonly used in distributed power systems [7]–[9] and from 400 Vdc to 12 Vdc for electric vehicle auxiliary power modules (APMs) and data centers [10]–[12]. Galvanic isolation is also required in many applications and power distribution units.

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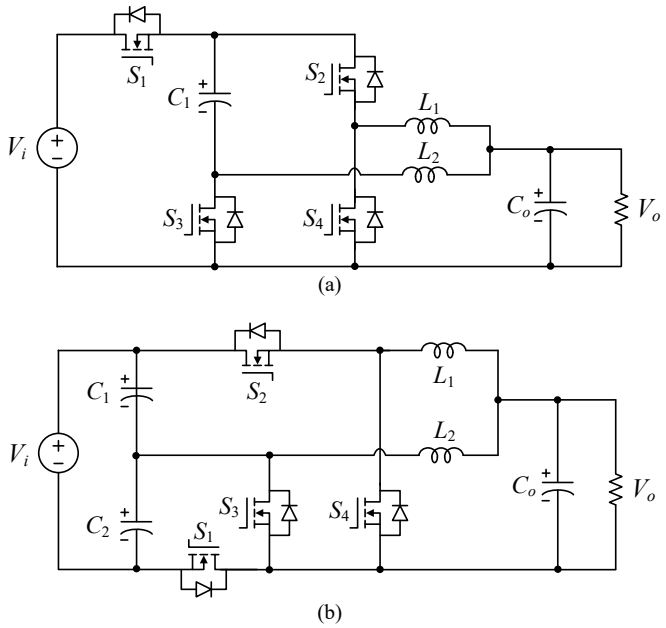

Fig. 1. Nonisolated step-down DC-DC converter. (a) Series-capacitor structure [25], (b) Split-capacitor structure [27].

To realize the isolated DC-DC conversion, an isolated resonant converter [13]–[14] is one of the popular topologies to achieve soft-switching for power switches. Soft-switching operation can be obtained by generating sinusoidal waveforms on the switching devices. Nevertheless, the output voltage of those resonant converters is controlled by implementing a variable switching frequency scheme, which makes it difficult to design magnetic elements. The voltage-fed half-bridge isolated (VFHB) converter [15]–[16] is another candidate topology for industrial applications because it is a simple structure and is easy to control. Nevertheless, the soft-switching condition is limited and there are high voltage stresses on the power switches. Then, the voltage-fed phase-shift full-bridge (PSFB) isolated converter [17]–[22] is shown in Fig. 2(a), which is considered to solve these concerns in VFHB converters and are widely employed due to the characteristics of fixed frequency, simple structure, and soft-switching operation. In a voltage-fed PSFB converter, the soft-switching operation of all power switches is achieved with the phase-shift control method. The first drawback of the PSFB converter is the narrow zero-voltage switching (ZVS) operating range. Therefore, auxiliary components or circuits are used to extend the soft-switching range. For example, increasing the leakage inductance or adding an external series inductance [18]–[19] of the transformer extends the ZVS range of lagging switches.

However, this leads to large leakage inductance of the high-frequency transformer to achieve the full soft-switching of all power switches. The large leakage inductance causes a high circulating current in the circuit, high voltage spikes on the secondary switching devices, and a high electromagnetic interference issue. Additional resonant circuits in [20]–[22] were introduced to maintain the soft-switching condition of the switches with extended ZVS ranges, and to reduce circulating losses of conventional PSFB converters. However, the additional components will increase the complexity and loss of the power converter, the cost, and the current stress of power switches. Several control methods were proposed to avoid the auxiliary circuits. For example, new pulse-width-modulation (PWM) schemes [23]–[24] were introduced to achieve a wide soft-switching range and reduce circulating current. But it causes saturation in the primary side of the transformer. To solve this problem, a blocking capacitor should be connected in series with the primary side of the transformer.

The double step-down structure has been applied to isolated DC-DC converters to improve the voltage conversion ratio and resolve the transformer saturation problem [25]–[29]. Fig. 1(a) presents the high step-down non-isolated DC–DC converter [25]–[26]. By using one extra series capacitor on the input side, this converter has the following advantages: it avoids the current unbalance problem between two output inductors; the voltage stress of the three switches is reduced to half of the input voltage. A high step-down non-isolated DC–DC converter based on a split-capacitor structure [27], shown in Fig. 1(b), was proposed to eliminate the issue of high voltage stress when the converter is started up and also reduce the converter volume of the converter. However, this converter does not retain the common ground feature compared to the series-capacitor-based converter [26]. For the isolation requirement, series-capacitor-based converters have been explored in the isolated topology [28]–[29]. In [28], an isolated double step-down DC-DC converter presented in Fig. 2 was proposed, which has the advantages of the non-isolated type with low voltage stress on three switches and provides a wider ZVS range without transformer saturation problem. Likewise, a high step-down isolated converter with a clamping circuit [29] was proposed to suppress the voltage spike of rectifier diodes and eliminate voltage oscillations. However, the series electrolyte capacitor on the primary side of these converters should be used and the series capacitor current is high, which is more prone to failure and increases the size of the converter. In addition, these converters have an issue of voltage stress on power switches during the start-up process. To eliminate the start-up voltage stress issue, a split-capacitor-based structure was applied to the dual-active bridge (DAB) topology. This converter achieves a low switching loss with reduced voltage stress of six switches and ZVS for all switches, lowering the DC-link split-capacitor. However, the split-capacitor structure was only applied to non-isolated topology [27] and DAB topology [30], which has not been explored in the voltage-fed full-bridge isolated topology. With the aforementioned consideration, a split-capacitor-based isolated double step-down DC-DC converter (SC-IDSDC) is presented in this paper. The proposed SC-IDSDC can provide all the merits of a non-isolated split-capacitor structure, such as

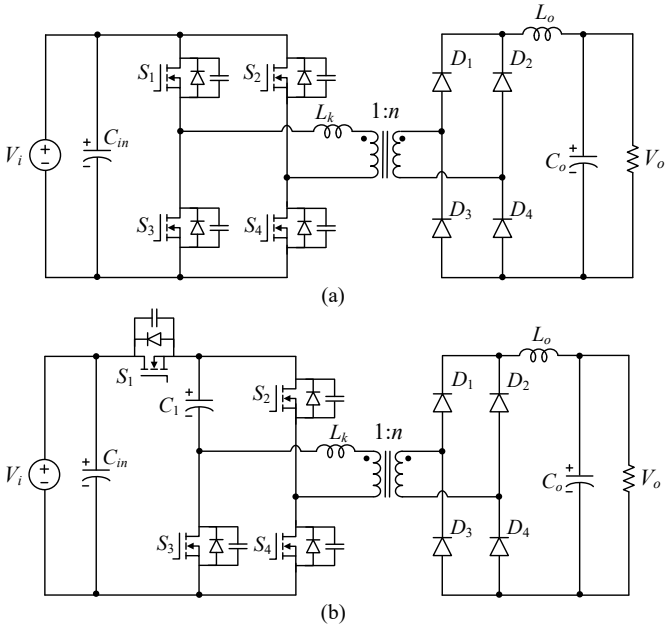

Fig. 2. Conventional series-capacitor-based isolated double step-down DC-DC converter [28].

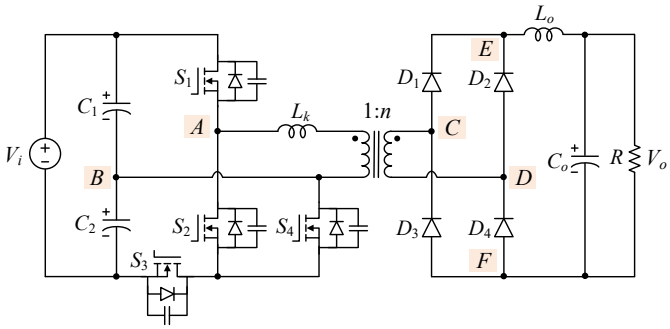

Fig. 3. Proposed split-capacitor-based isolated double step-down DC-DC converter.

low voltage stress on three switches, start-up voltage stress problem elimination, and input capacitance reduction. In addition, the proposed SC-IDSDC also achieves ZVS turn-on for all switches without transformer saturation problems.

The content of this paper is arranged as follows. The structure and operating principle of the proposed SC-IDSDC are presented in Section II. To highlight the performance of the proposed SC-IDSDC, a comparative study is presented in Section III. The effectiveness of the proposed SC-IDSDC is validated by the simulation and experimental results of a 1 kW−400 V/48 V laboratory prototype, given in Section IV. Finally, Section V concludes the paper.

II. Proposed SC-IDSDC

A. Operating Principle of the Proposed SC-IDSDC

As shown in Fig. 3, the proposed converter consists of a double step-down on the primary side with four switches (S_1−S_4), two input capacitors (C_1−C_2), HF transformer, a diode bridge (D_1−D_4), and output inductor filter (L_o) and capacitor (C_o)

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are used for the output filter. Fig. 4 shows the operating waveforms of the proposed SC-IDSDC. In this case, switches S_1 and S_2 are on with a duty cycle of D and phase-shifted 180°; S_3 and S_4 are complementary with S_1 and S_2, respectively. The input capacitors C_1–C_2 are connected in series, and their voltages are equal to $V_i/2$. Fig. 5 shows the operating modes of the proposed SC-IDSDC.

Interval 1-[t_0–t_1, Fig. 5(a)]: S_1 and S_4 are turned on. The input power is transferred to the output. Capacitors C_1 and C_2 are discharged and charged, respectively. Each capacitor voltage is equal to $V_i/2$. The primary voltage of the transformer is positive, and diodes D_1, and D_4 conduct. The leakage inductor current i_{lk} increases linearly and equals

$$v_{AB} = V_i / 2 \tag{1}$$

$$i_{lk}(t) = \frac{(v_{AB} - v_{CD}/n)}{L_{lk}} \times (t - t_0) \tag{2}$$

Interval 2-[t_1–t_2, Figs. 5(b)-(c)]: At t_1, S_1 is turned off and S_4 is still on. The parasitic capacitor C_{S1} is charged, and C_{S2} is discharged by the leakage inductor, as depicted in Fig. 5(b). When the parasitic capacitor of S_2 is fully discharged and the body diode D_{S2} is conducted, then switch S_2 is turned on with ZVS condition, as depicted in Fig. 5(c). The leakage inductor energy has to charge C_{S1} and discharge C_{S2}. Then, half of the leakage inductance energy is required for the ZVS operation of switch S_2. The ZVS operating condition for switch S_2 is determined as

$$\frac{1}{2}C_{S1}V_{S1}^2 + \frac{1}{2}C_{S2}V_{S2}^2 \le L_{lk}i_{lk}^2(t_1)/2, \tag{3}$$

Interval 3-[t_2–t_3, Fig. 5(d)]: Switch S_4 remains on and switch S_2 is turned on. The leakage current i_{lk} circulates through switch S_4 and body diode D_{S2}, and i_{lk} decreases linearly. The transformer primary voltage v_{AB} and rectifier voltage v_{EF} become zero if the voltage drops on D_{S2} and S_4 are neglected.

$$v_{AB} = 0 \tag{4}$$

$$i_{lk}(t) = i_{lk}(t_2) - \frac{v_{CD}/n}{L_{lk}} \times (t - t_2) \tag{5}$$

Interval 4-[t_3–t_4, Figs. 5(e)-(f)]: At t_3, S_2 remains on and S_4 is off. The switch output capacitors C_{S1} and C_{S4} are charged while C_{S3} is discharged by the primary current, as depicted in Fig. 5(e). In this deadtime duration, the leakage current is reduced and the primary voltage and secondary voltage have become zero. When the capacitor C_{S3} is fully discharged, and the body diode D_{S3} conducts, switch S_3 will be turned on under ZVS condition, as shown in Fig. 5(f). The leakage inductor current i_{lk} circulates through capacitor C_2 and body diodes D_{S2} and D_{S3}. The ZVS condition for switch S_3 is given

$$\frac{1}{2}C_{S1}V_{S1}^2 + \frac{1}{2}C_{S3}V_{S3}^2 + \frac{1}{2}C_{S4}V_{S4}^2 \le \frac{1}{2}L_{lk}i_{lk}^2(t_3), \tag{6}$$

Interval 5-[t_4–t_5, Fig. 5(g)]: When S_2 is turned on and S_3 is still on, the primary voltage v_{AB} becomes negative, and diodes

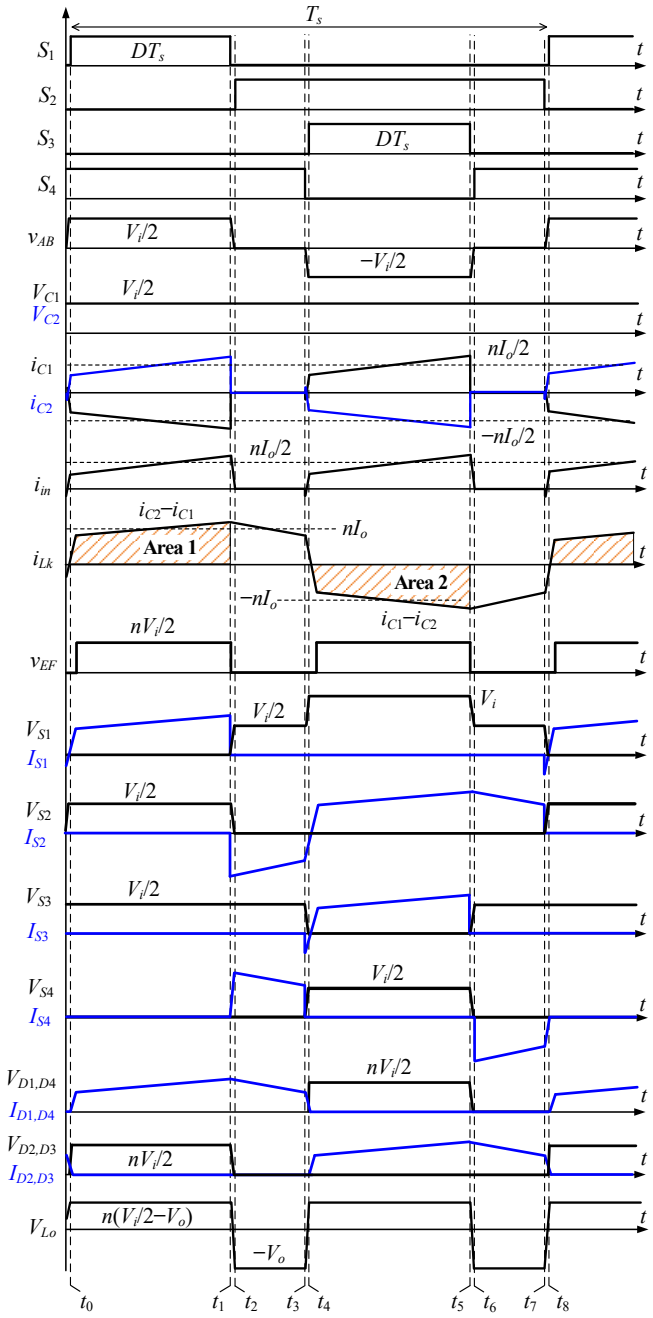

Fig. 4. Typical waveforms of the proposed SC-IDSDC.

D_2 and D_3 conduct. The primary voltage and leakage inductor current are derived as

$$v_{AB} = -\frac{V_i}{2} \tag{7}$$

$$i_{lk}(t) = i_{lk}(t_4) + \frac{(v_{AB} - v_{CD}/n)}{L_{lk}} \times (t - t_4) \tag{8}$$

Interval 6-[t_5–t_6, Figs. 5(h)-(i)]: At t_5, S_3 is turned off and S_2 is still on. From Fig. 5(h), the switch capacitors C_{S1}, and C_{S3}

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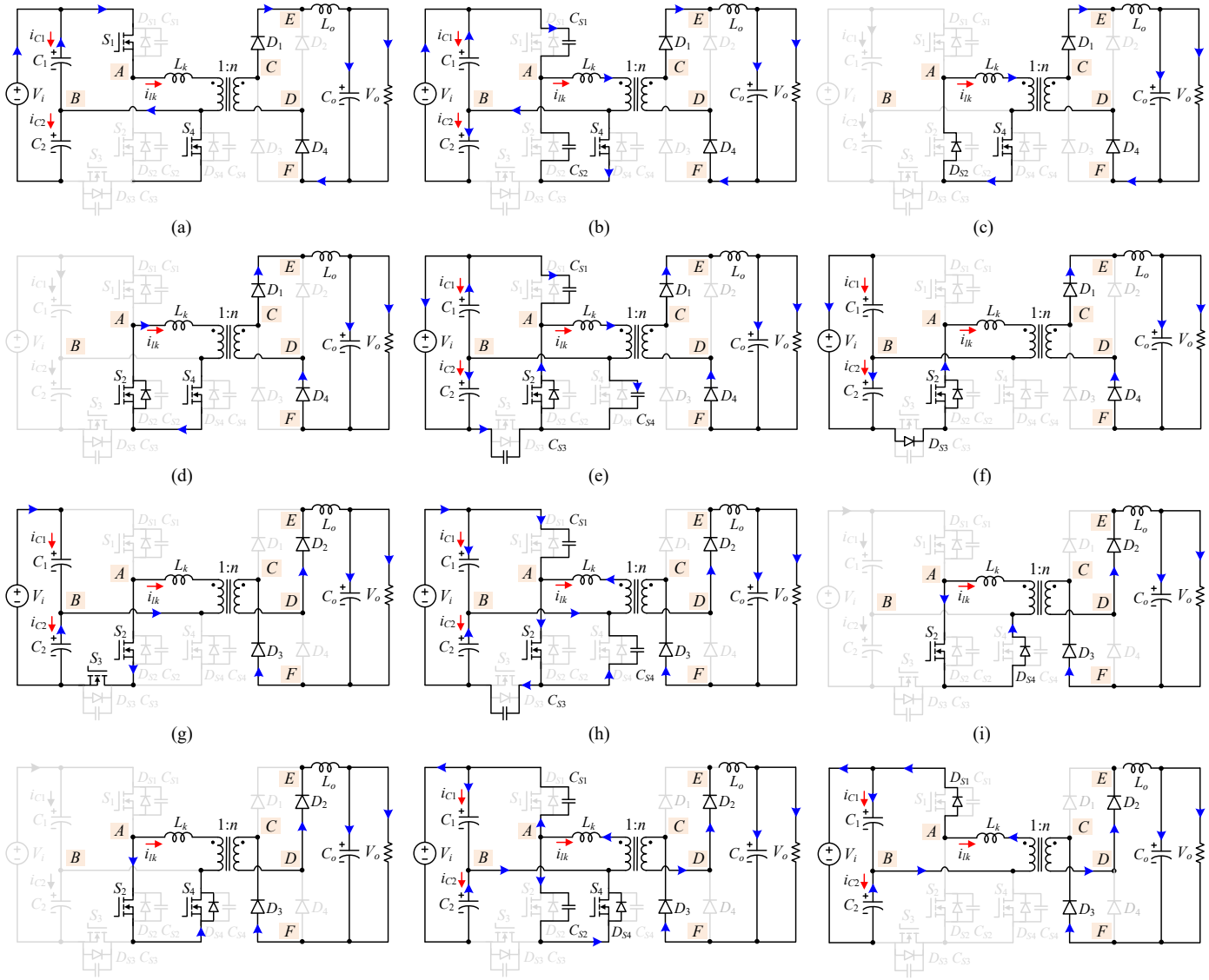

Fig. 5. Equivalent circuits of the proposed SC-IDSDC.

are charged and C_{S4} is discharged by the leakage inductor. When the capacitor C_{S4} is fully discharged and the body diode D_{S4} conducts, switch S_4 is operated with ZVS condition, as shown in Fig. 5(i). The leakage inductor current i_{lk} circulates through switch S_2 and body diodes D_{S4}. The ZVS condition for switch S_4 is given

$$\frac{1}{2}C_{S1}V_{S1}^2+\frac{1}{2}C_{S3}V_{S3}^2+\frac{1}{2}C_{S4}V_{S4}^2\le\frac{1}{2}L_{lk}i_{lk}^2(t_5), \tag{9}$$

Interval 7-[t_6–t_7, Fig. 5(j)]: Switch S_2 remains on and switch S_4 is turned on. The leakage inductor current i_{lk} circulates through switch S_2 and body diode D_{S4}. The leakage inductor current i_{lk} decreases linearly and the primary voltage becomes zero.

$$v_{AB}=0 \tag{10}$$

$$i_{lk}(t)=i_{lk}(t_6)-\frac{v_{CD}/n}{L_{lk}}\times(t-t_6) \tag{11}$$

Interval 8-[t_7–t_8, Figs. 5(k)-(l)]: At t_7, S_2 is turned off and S_4 remains on. As shown in Fig. 5(k), the switch capacitor C_{S1} is discharged, and C_{S2} is charged by the leakage inductor current. When C_{S1} is fully discharged and the body diode D_{S1} conducts, then switch S_1 can be turned on under ZVS, as depicted in Fig. 5(l). The ZVS condition for switch S_1 is given by

$$\frac{1}{2}C_{S1}V_{S1}^2+\frac{1}{2}C_{S2}V_{S2}^2\le\frac{1}{2}L_{lk}i_{lk}^2(t_7), \tag{12}$$

The voltage waveform of output inductor v_{Lo} is shown in Fig. 4. By applying the volt-sec balance condition on the output

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TABLE I: COMPARISON OF THE CONVENTIONAL PSFB CONVERTER, THE CONVENTIONAL SC CONVERTER [28] AND THE PROPOSED SC-IDSDC

	Conventional PSFB converter	Conventional SC converter [28]	Proposed SC-IDSDC
Voltage gain	nD	$nD/2$	$nD/2$
Transformer voltage	V_i	$V_i/2$	$V_i/2$
Transformer saturation	Yes	No	No
ZVS range	Narrow	Wide	Wide
Required ZVS energy	CV_i^2	$\frac{3CV_i^2}{8}$	$\frac{3CV_i^2}{8}$
NPC-type connection	No	No	Yes
Switch current stress	I_o for all switches	$I_o/2$ for S_2~S_4 I_o for S_1	$I_o/2$ for S_2~S_4 I_o for S_1
Start-up voltage stress	V_i for all switches	V_i for all switches	V_i for S_1 $V_i/2$ for S_2~S_4
Steady-state voltage stress		V_i for S_1 $V_i/2$ for S_2~S_4	
Input current stress	I_o	$I_o/2$	$I_o/4$
Additional series capacitor	NA	$\frac{Dk_{Ci}}{2}$	NA

Where $k_{Ci} = nI_o/(f_s.\Delta v_{Ci})$, C is the output capacitor of MOSFET and $C = C_{S1} = C_{S2} = C_{S3} = C_{S4}$.

TABLE II: PARAMETERS FOR SIMULATION AND EXPERIMENT

Parameter	Values
Input voltage	400 V
Output voltage	48 V
Power rating	1 kW
Capacitors	680 µF/100V for C_o 330 µF/400V for C_1 and C_2
Switching frequency	50 kHz
Rectifier diodes	STPS60SM200C
Power switches	IPW60R045CPA for S_1 IRFP4868 for S_2~S_4
Transformer	L_{lk} = 7 µH, n = 26:8

inductor and ignoring the leakage voltage ($V_{lk} = 0$) in this case, the relationship between the input and output voltages can be calculated as

$$V_o = \frac{nD}{2} V_i, \tag{13}$$

Where n and D are the turns ratio and the duty cycle, respectively.

B. Automatic Removal of Transformer Saturation and Start-up Voltage Stress Characteristics

The primary current of the transformer and input capacitors' current waveforms are denoted in Fig. 4. For simplicity in illustration, the dead-time between two complementary switches is ignored in this case. The saturation problem of the transformer is effectively avoided for the following reasons. It can be observed that the leakage inductor current is constituted with a part of input capacitors C_1–C_2 currents in modes 1 (t_0–t_1) and 5 (t_3–t_5), which can be noted as areas 1 and 2 in Fig. 4. Based on the amp-sec balance condition of input capacitors C_1 and C_2, areas 1 and 2 must be equal. Therefore, the average leakage inductor current in the intervals (t_0–t_1) and (t_3–t_5) becomes zero, and the leakage current magnitude values at t_1 and t_5 are equal. From (3) and (7), the average leakage inductor current in the intervals (t_2–t_3) and (t_6–t_7) becomes zero. From the above explanations, the saturation of the transformer is automatically solved while the tolerance values between two capacitors C_1 and C_2 are considered. In addition, it can be observed that the two input capacitors C_1 and C_2 are connected in parallel with the input voltage. Therefore, the input capacitors C_1 and C_2 are pre-charged before start-up and the voltage stresses of all power switches will not change in both the start-up and steady-state operations.

C. Input Capacitor Selection

It can be seen that the input capacitors C_1 and C_2 voltage are similar and equal to $V_i/2$. Considering the interval (t_4-t_5), the input capacitor currents are given as

$$i_{C1} = i_{C2} = C_1 \frac{\mathrm{D}v_{C1}}{DT_s/2} = C_2 \frac{\mathrm{D}v_{C2}}{DT_s/2} = \frac{nI_o}{2}, \tag{14}$$

The values of C_1 and C_2 are derived as

$$C_1 = C_2 = \frac{Dk_C}{2}, \tag{15}$$

Where $k_C = nI_o/(f_s.\Delta v_C)$ is the peak-to-peak ripple of the input capacitor voltage.

III. COMPARATIVE STUDY

Table I provides a detailed comparison of the conventional PSFB converter, the conventional SC converter [28], and the proposed SC-IDSDC. The comparison is taken in terms of different factors including the voltage gain, transformer primary voltage, transformer saturation issue, ZVS range, NPC connection type, voltage and current stresses, input current stress, and additional series capacitor. The conventional SC converter [28] overcomes some issues in the conventional PSFB converters by providing a high step-down ratio, soft-switching range extension, transformer saturation issue elimination, and low switch voltage stress as presented in [28]. In addition, considering the high step-down ratio, the conventional SC converter [28] is the closest to the proposed SC-IDSDC among the conventional high step-down converter. As shown in Figs. 2-3, the proposed SC-IDSDC does not use an additional series capacitor compared with the conventional SC converter when two capacitors C_1 and C_2 are considered as the input capacitors. As can be seen in Table I, the primary transformer voltage, transformer saturation issue, ZVS characteristic, voltage, and current stress on switching devices in the steady state of the conventional SC converter [28] and the proposed SC-IDSDC are similar. For the start-up voltage stress comparison, the proposed SC-IDSDC does not have increased

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voltage stress on power switches. On the contrary, three power switches in the conventional SC converter are subject to increased voltage stress. Therefore, the proposed SC-IDSDC can reduce the switching loss of three power switches with lower voltage stress. When compared with the conventional SC converter, the input current of the proposed SC-IDSDC is half of the input current of the conventional SC converter [28]. Regarding the mentioned characteristics, the proposed SC-IDSDC is a better choice compared with the conventional PSFB converter and the conventional SC converter [28] when high step-down capability and a wide range of ZVS conditions are required.

IV. Simulation And Experimental Verifications

To confirm the correctness and effectiveness of the proposed SC-IDSDC, both simulation and experimental results are carried out.

A. Simulation Verifications

The proposed SC-IDSDC is implemented in the PSIM software to validate the advantages of the proposed SC-IDSDC. In this simulation model, the on-resistance of S_1 and S_2~S_4 are 45 mΩ and 26 mΩ, respectively. The forward voltage and on-resistance of all rectifier diodes are 0.7 V and 60 mΩ, respectively. The output voltage of 48 V is bucked from a 400 V input voltage. Thus, the duty cycle and turn ratio of the transformer are selected at 0.39 and 26:8, respectively. The 50 kHz switching frequency is chosen. The proposed SC-IDSDC is employed with a resistive load of 2 Ω and an LC filter of (100 μH, 680 μF) at the output side. Fig. 6(a) shows the simulation results during start-up operation and the voltage stresses of all switches are not changed from start-up to steady-state condition. The obtained simulation waveforms of all switches match the theoretical analysis in Section II. B, as shown in Fig. 6(b). From the waveforms, all switches are turned on under ZVS conditions. The primary voltage v_{AB} and secondary voltage v_{CD} are positive and negative at ± 200 V and ± 62 V, respectively. Fig. 6(d) shows the simulation waveforms for the leakage inductor current, input current and voltage, and the current stresses of the secondary diodes. The simulation results match the key waveforms in Fig. 4.

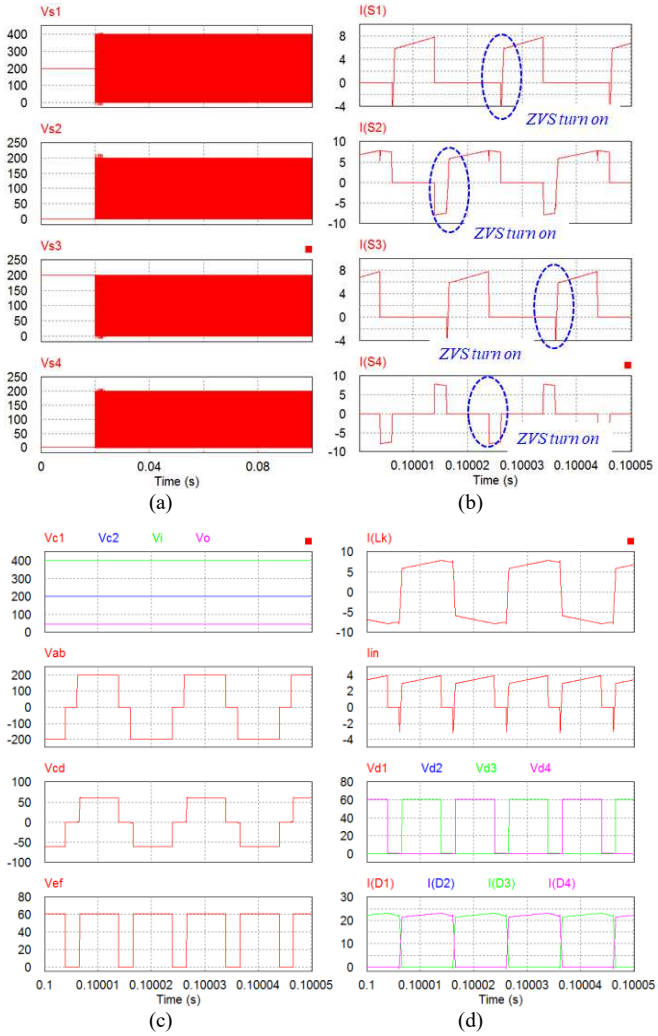

Fig. 6. Simulation results of the proposed SC-IDSDC.

B. Experimental Verifications

A 1 kW prototype of the proposed SC-IDSDC was built in the laboratory. The specifications for the testing prototype are listed in Table II and the prototype picture of the proposed SC-IDSDC is shown in Fig. 7. Herein, MOSFETs IRFP4868PbF (300 V, 70 A, r_{DSon} = 25.5 mΩ) were selected for switches S_2, S_3, and S_4, MOSFETs IPW60R045CPA (600 V, 60 A, r_{DSon} = 45 mΩ) was selected for switches S_1. Four STPS60SM200C Schottky (200 V, 30 A, V_F = 0.64 V) diodes were used for rectifier diodes. Fig. 8(a) depicts the voltage waveforms of power switches during the start-up process. The voltage waveforms of S_2, S_3, and S_4 are maintained at V_i/2, and the voltage stress of S_1 is the input voltage. The output voltage of 46.8 V is obtained from a 400 V input voltage and the duty cycle

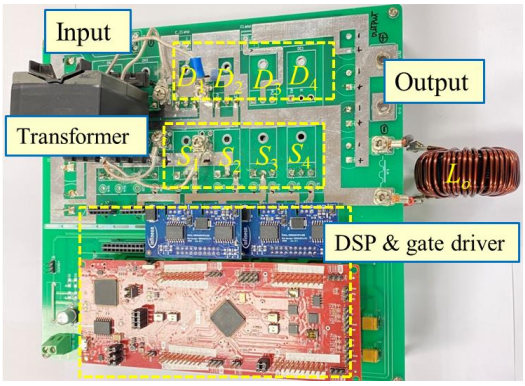

Fig. 7. Prototype of the proposed SC-IDSDC.

is set at 0.39. Two input capacitors C_1 and C_2 voltages are equal to 200 V, as depicted in Fig. 8(b). The primary voltage v_{AB}, secondary voltage v_{CD}, the leakage inductor current, and the rectifier diode-voltage and current stresses are depicted in Figs. 8(c)-(d). The voltage waveforms of the transformer are the AC

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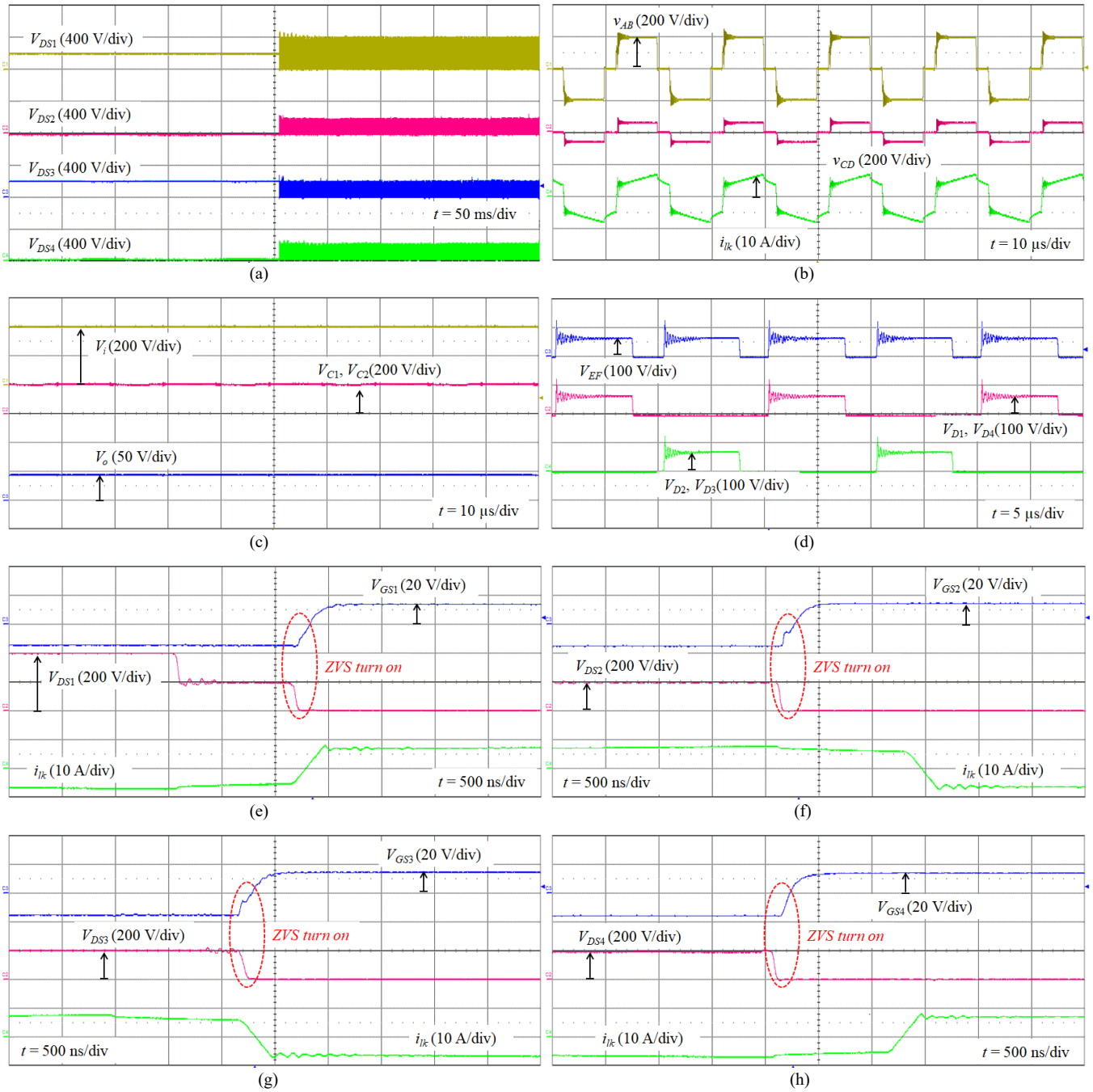

Fig. 8. Experimental waveforms of the proposed SC-IDSDC. (a) Voltage stresses of S_1, S_2, S_3 and S_4 during start-up, (b) Primary and secondary voltage, leakage current, (c) input voltage, capacitors C_1 and C_2 voltage, output voltage, (d) V_{EF} voltage and rectifier diodes voltage, (e)-(h) Gate-source and drain-source voltages of S_1, S_2, S_3 and S_4.

pulse with three levels when the duty cycle is 0.39. Figs. 8(e)-(h) show that drain-source and gate-source waveforms of S_1, S_2, S_3 and S_4 when they are turned on. From Figs. 8(e)-(h), we can see that all power switches are operated under ZVS turn-on conditions. As expected, these experimental results match the simulation results.

Fig. 9 depicts the measured efficiency comparison of the conventional PSFB converter, conventional SC converter [28], and the proposed SC-IDSDC with the same operating condition. Here, the blocking capacitor is added to the conventional PSFB converter to avoid the saturation issue of the transformer. The conventional SC converter [28] and proposed SC-IDSDC have higher efficiency than the conventional PSFB converter at light load conditions. It can be seen that the efficiencies of the conventional PSFB converter, conventional SC converter [28], and the proposed SC-IDSDC are 94.3, 94.1%, and 95.2% at full

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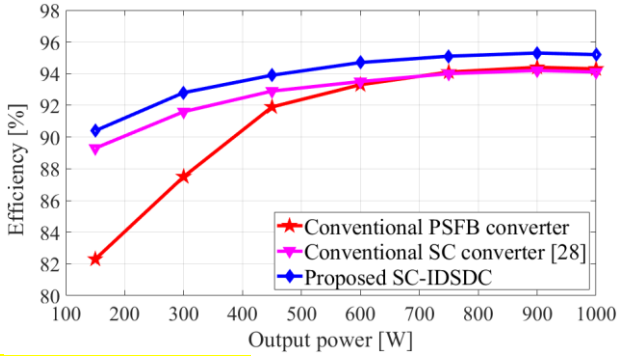

Fig. 9. Efficiency measurement.

load conditions, respectively. Because the drain-to-source on-resistance and turn-off time of the three switches used in the proposed SC-IDSDC can be reduced, the conduction and switching losses of the proposed SC-IDSDC are lower than those of the conventional PSFB converter and conventional SC converter [28].

V. Conclusion

In this paper, the proposed SC-IDSDC with a double step-down ratio was presented. By split-capacitor configuration in the input side, the proposed SC-IDSDC has the following outcomes and characteristics: reduced voltage stresses for three switch voltages with half of the input voltage, ZVS for all power switches; transformer saturation elimination, and mitigation of start-up voltage stress issue. In the switching process of the proposed SC-IDSDC, all switches are switched with a voltage transition equal to half of the input voltage, which decreases significantly the required soft-switching energy. Thus, power switches can achieve high efficiency in light load conditions. Consequently, the proposed SC-IDSDC can improve the efficiency range of the conventional PSFB converter with reduced voltage stress and a wider ZVS range. In addition, the proposed SC-IDSDC has no issue of transformer saturation. Compared to the conventional isolated SC converter, the proposed SC-IDSDC also improves efficiency and reduces the additional series capacitor. The circuit topology and operating principles of the proposed SC-IDSDC are presented. Finally, the simulation and experimental results have been provided to verify the correctness and effectiveness of the proposed SC-IDSDC.

References

[1] M. K. Nguyen, T. D. Duong, Y. C. Lim, and Y. J. Kim, "Isolated boost dc–dc converter with three switches," *IEEE Trans. Power. Electron*., vol. 33, no. 2, pp. 1389–1398, Feb. 2018.

[2] M. K. Nguyen, Y. C. Lim, J. H. Choi and G. B. Cho, "Isolated high step-up DC-DC converter based on quasi-switched boost network," *IEEE Trans. Ind. Electron*., vol. 63, no. 12, pp. 7553–7562, Dec. 2016.

[3] E. Rodriguez-Diaz, J. C. Vasquez and J. M. Guerrero, "Intelligent DC Homes in Future Sustainable Energy Systems: When efficiency and intelligence work together," *IEEE Consumer Electronics Magazine*, vol. 5, no. 1, pp. 74-80, Jan. 2016.

[4] M. Arias, D. G. Lamar, F. F. Linera, D. Balocco, A. A. Diallo, and J. Sebastian, "Design of a soft-switching asymmetrical half-bridge converter as second stage of an LED driver for street lighting application," *IEEE Trans. Power Electron.,* vol. 27, no. 3, pp. 1608–1621, Mar. 2012.

[5] Y. T. Yau, W. Z. Jiang and K. I. Hwu, "Ultrahigh step-down converter with wide input voltage range based on topology exchange," *IEEE Trans. Power Electron*., vol. 32, no. 7, pp. 5341-5364, Jul. 2017.

[6] A. Khaligh and M. D'Antonio, "Global trends in high-power on-board chargers for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3306–3324, Apr. 2019.

[7] J. Khodabakhsh and G. Moschopoulos, "A study of T-type and ZVSPWM full-bridge converters for switch-mode power supplies," *IEEE Trans. Power Electron.,* vol. 35, no. 7, pp. 7145–7159, Jul. 2020.

[8] R. Kathiresan, P. Das, T. Reindl, and S. K. Panda, "A novel ZVS DC–DC full-bridge converter with hold-up time operation," *IEEE Trans. Ind. Electron.,* vol. 64, no. 6, pp. 4491–4500, Jun. 2017.

[9] T. Mishima, K. Akamatsu and M. Nakaoka, "A high frequency-link secondary-side phase-shifted full-range soft-switching PWM DC–DC converter with ZCS active rectifier for EV battery chargers," *IEEE Trans. Power Electron*., vol. 28, no. 12, pp. 5758-5773, Dec. 2013.

[10] G. N. B. Yadav, and N. L. Narasamma, "An active soft switched full bridge DC–DC Converter: Analysis, modeling, design, and implementation," *IEEE Trans. Power Electron*., vol. 29, no. 9, pp. 4538–4550, Sep. 2014.

[11] P. N. Truong, N. A. Dung, Y. C. Liu, and H. J. Liu, "A non-isolated high step-down DC–DC converter with low voltage stress and zero voltage switching," *IEEE Trans. Power Electron*., *early access*, 2022.

[12] S. Kim, H. Cha, and H. G. Kim, "High-efficiency voltage balancer having DC–DC converter function for EV charging station," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 9, no. 1, pp. 812–821, Feb. 2021.

[13] X. Zhao, L. Zhang, R. Born, and J.-S. Lai, "A high-efficiency hybrid resonant converter with wide-input regulation for photovoltaic applications," *IEEE Trans. Ind. Electron*., vol. 64, no. 5, pp. 3684–3695, May 2017.

[14] T. D. Duong, M. K. Nguyen, A. D. Nguyen, C. Wang, Y. C. Lim and J. H. Choi, "Isolated quasi-switched boost series resonant DC-DC converter," *IECON 2021 – 47th annual conference of the IEEE industrial electronics society*, 2021, pp. 1-2.

[15] I. O. Lee, and G. W. Moon, "A new asymmetrical half-bridge converter with zero DC-offset current in transformer," *IEEE Trans. Power Electron*., vol. 28, no. 5, pp. 2297–2306, May. 2013.

[16] H. Li, L. Zhao, C. Xu, and X. Zheng, "A dual half-bridge phase-shifted converter with wide ZVZCS switching range," *IEEE Trans. Power Electron*., vol. 33, no. 4, pp. 2976–2985, Apr. 2018.

[17] C. Y. Lim, Y. Jeong, and G. W. Moon, "Phase-shifted full-bridge DC–DC converter with high efficiency and high power density using center-tapped clamp circuit for battery charging in electric vehicles," *IEEE Trans. Power Electron*., vol. 34, no. 11, pp. 10945–10959, Nov. 2019.

[18] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage switched PWM converter," *in Proc. Appl. Power Electron. Conf.*, 1990, pp. 275–284.

[19] R. Redl, N. O. Sokal, and L. Balogh, "A novel soft-switching full-bridge DC/DC converter: Analysis, design considerations, and experimental results at 1.5 kW, 100 kHz," *IEEE Trans. Power Electron*., vol. 6, no. 3, pp. 408–418, Jul. 1991.

[20] Z. Guo, D. Sha, and X. Liao, "Input-series-output-parallel phase shift full bridge derived DC-DC converters with auxiliary LC networks to achieve wide zero voltage switching range," *IEEE Trans. Power Electron*., vol. 29, no. 10, pp. 5081–5086, Oct. 2014.

[21] Y. Lo, C. Lin, M. Hsieh, and C. Lin, "Phase-shifted full-bridge series resonant DC-DC converters for wide load variations," *IEEE Trans. Ind. Electron*., vol. 58, no. 6, pp. 2572–2575, Jun. 2011.

[22] A. Safaee, P. Jain, and A. Bakhshai, "A ZVS pulse width modulation full-bridge converter with a low-RMS-current resonant auxiliary circuit," *IEEE Trans. Power Electron*., vol. 31, no. 6, pp. 4031–4047, Jun. 2016.

[23] B. Gu, J. S. Lai, N. Kees, and C. Zheng, "Hybrid-switching full-bridge DC–DC converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers," *IEEE Trans. Power Electron*., vol. 28, no. 3, pp. 1132–1144, Mar. 2013.

[24] V. R. K. Kanamarlapudi, B. Wang, N. K. Kandasamy, and P. L. So, “A new ZVS full-bridge DC–DC converter for battery charging with reduced losses over full-load range,” *IEEE Trans. Ind. Appl*., vol. 54, no. 1, pp. 571–579, Jan. 2018.

[25] K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, “Analysis of double step-down two-phase buck converter for VRM,” *in Proc. 27th Int. Telecommun. Conf*., Sep. 2005, pp. 497–502.

[26] D. V. Bui, H. Cha, and V. C. Nguyen, "Asymmetrical PWM series capacitor high-conversion-ratio DC-DC converter," *IEEE Trans. Power Electron*., vol. 36, no. 8, pp. 8628-8633, Aug. 2021.

[27] K. Kim, H. Cha, S. Park, and I. O. Lee, “A modified series-capacitor high conversion ratio DC–DC converter eliminating start-up voltage stress problem,” *IEEE Trans. Power Electron*., vol. 33, no. 1, pp. 8–12, Jan. 2018.

[28] S. Kim, H. Cha, H. Ahmed, and H. Kim, “Isolated double step-down DC–DC converter with improved ZVS range and no transformer saturation problem,” *IEEE Trans. Power Electron*., vol. 32, no. 3, pp. 1792–1804, Mar. 2017.

[29] Z. Chen, Y. Chen, and Q. Chen, “Isolated series-capacitor-based full-bridge converter with reduced circulating losses and wide soft switching range,” *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 7, no. 2, pp. 1272–1285, Jun. 2019.

[30] K. Kim and H. Cha, “Split-capacitor dual-active-bridge converter,” *IEEE Trans. Ind. Electron*., vol. 68, no. 2, pp. 1445–1453, Feb. 2021.