Strained-topological-insulator spin-orbit-torque random-access-memory bit cell for energy-efficient processing in memory

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We present a design of a strained-topological-insulator spin-orbit-torque random-access-memory (STI SOTRAM) bit cell comprising a piezoelectric/magnet (gating)/topological insulator (TI)/magnet (storage) heterostructure that leverages the TI's high charge-to-spin conversion efficiency coupled with the piezo-induced strain-based gating mechanism for low-power in-memory computing. The piezo-induced strain effectively modulates the conductivity of the topological surface state by altering the gating magnet's magnetization from out of to in plane, facilitating the storage magnet's spin-orbit-torque (SOT) switching. Through comprehensive coupled stochastic Landau-Lifshitz-Gilbert simulations, we explore the device dynamics, anisotropy-stress phase space for switching, and write conditions and demonstrate a significant reduction in energy dissipation compared to conventional heavy-metal-based SOT switching. Additionally, we project the energy consumption for in-memory Boolean operations (AND and OR). Our findings suggest the promise of the STI SOTRAM for low-power, high-performance edge computing.

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I. INTRODUCTION

Electronics in the edge computing era poses unique challenges that may need heterogeneous combinations of materials with diverse attributes, and devices and circuits that capitalize on those attributes [1,2]. Along this path, the intersection of magnetism, topology, and strain offers a highly complementary suite of symmetries and tunable properties that could play off of each other strategically. For instance, strain can alter the energy landscape [3] of a magnet and rotate it by 90° [4]. Rotating a magnet out of plane can modulate spin conductivity of a three-dimensional (3D) topological insulator (TI) by breaking time-reversal symmetry and gapping its topological surface states (TSS) [5–7]. Conversely, a TI can act on the magnet when its spin-momentum-locked TSS write spin information onto the free layer of a magnetic tunnel junction (MTJ) with a current driven spin-orbit torque (SOT), its spin Hall angle (SHA) exceeding unity [8–11]. Integrating these properties into a single stack may allow us to naturally integrate multiple functionalities into a compact, vertical monolithic structure.

In this paper, we will discuss an example stack, a multifunctional device composed out of a four-layer piezo/magnet/TI/magnet structure (Fig. 1), which exploits the above attributes to achieve both logic and memory functions in a single bit cell. Here strain actuates a bottom magnet in and out of the TI plane with a voltage-gated piezo, which modulates the TSS and drives a top storage magnet into a write mode, a read mode, or a logic mode using a sense amplifier. Since selector and storage magnets are co-located in a vertical geometry, the structure is scalable and naturally suited for a processing-in-memory (PIM) architecture. In contrast to traditional Von Neumann architecture (separate memory and logic cores with data-transfer latency) [12,13], key processing tasks are performed locally within a PIM [14–17], allowing the preprocessed data to be transferred to the primary processing unit with reduced latency [18]. The individual memory cells in a PIM architecture (bit cells) are often organized in a crossbar layout. Selectors control each row and column of the crossbar grid, enabling the bit cells for read or write operations. Utilizing sense amplifiers, the entire row

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of the crossbar can be read by comparing the state of the bit cells with a known reference voltage or current to perform logic operations within the memory [19–21].

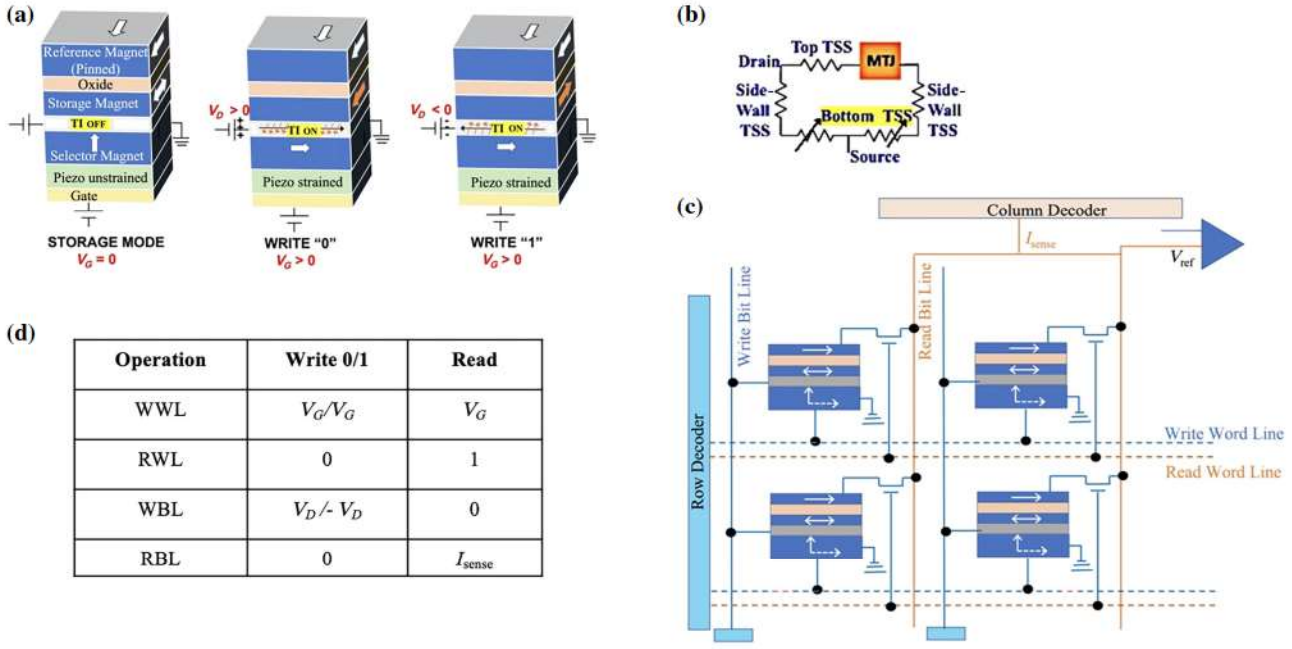
The specific design of the stack depends on the convenience of fabrication (e.g., here we assume the thick piezo layer sits at the bottom, the bottom magnet on it to share the strain, then the TI to feel its proximal magnetization, and finally, the top magnet to get a write operation on it). Other lateral or flipped structures may well serve as better designs, if only for ease of fabrication. The core functionality, however, is employing SOT from a single-channel material, in this case, the TI delivers both high SHA and simultaneously gate tunability. Let us now discuss these two features separately.

Magnetic random access memory (MRAM) is a leading contender for a PIM bit cell due to its nonvolatility, high-speed, low-power consumption, high endurance, scalability, and excellent compatibility with complementary metal-oxide-semiconductor (CMOS) process technology [17,22,23]. The fundamental building block for MRAM devices is an MTJ, which consists of a thin insulator sandwiched between two magnetic layers—a "pinned layer" whose magnetization is fixed and a "free layer" whose magnetization can be reoriented by a spin current. Conventional MRAM uses current in the overhead to apply a magnetic field to write data on the MTJ free layer. Recently, a current-induced SOT mechanism, resulting from either the spin Hall effect [24,25] or the Rashba effect [26], has emerged as a promising approach for energy-efficient switching of the MTJ's free layer. SOT-based switching addresses several limitations of its already commercialized counterpart, spin-transfer torque- (STT) based switching, such as the need for high write voltages, shared read-write paths creating read disturbs, and degradation of the insulating layer [27–29]. SOT-based MRAM (SOTRAM) is a three-terminal device featuring a decoupled read-write path and in-plane charge-current flow in the nonmagnetic layer underneath the MTJ free layer with a high charge-to-spin conversion efficiency, yielding a low write current and infinite endurance [24,25]. SOTRAM is attractive as a high-density last-level-embedded cache [30,31], with distinct advantages for PIM-like edge-based motion detection and cross-modality object recognition [23,32]. They do suffer from the higher footprint associated with the third terminal, a higher charge current needed to supply the spin current orthogonal to it, and the need for a field assist when the free-layer spin stagnates onto a symmetry direction in the magnet/heavy metal (HM) interfacial plane. Consequently, achieving a significantly high charge-to-spin conversion efficiency (large SHA) is essential to bypass these challenges for energy-efficient applications.

Traditional SOT devices typically utilize HMs such as Pt [25,33], Ta [24], and W [34] as spin current injectors; however, these HMs exhibit low SHA (Pt, 0.08; Ta, 0.15; W, 0.4 [35]), leading to low charge-to-spin conversion efficiency [11]. Recently, TIs have garnered attention as an attractive spin source for SOT switching [8–10,36,37]. TIs are characterized by their spin-momentum-locked TSS, insulating bulk states, and SHA greater than unity [38–40]. The conducting TSS arise from band inversion at the surface, mediated by strong spin-orbit coupling, and are topologically protected by time-reversal symmetry [41–43]. More encouragingly, sputtered TIs such as Bi_2Se_3 show very high (> 10) SHAs, primarily because of the reduction in bulk conductivity that would otherwise shunt current away from the TSS, as well as better defect control that suppresses unwanted surface scattering. These attributes make TIs highly efficient spin-current injectors for SOT switching, facilitating energy-efficient information writing [44].

Conversely, a magnet's ability to modulate the spin conductivity of the TSS of a TI, when in proximity with the TI, based on its magnetization direction, offers a pathway for an intrinsic gating mechanism to control the TI surface current [5,45]. Switching the magnet (gating magnet hereafter) from in-plane to out-of-plane orientations, gaps in the TSS can be opened, thereby modulating the spin conductivity [6,7]. This 90° switching of the gating magnet can be achieved through various mechanisms, such as strain [46–49], voltage-control magnetic anisotropy [50], and changing the anisotropy by an applied voltage [5,51]. Nonetheless, strain-induced 90° switching of magnets is very energy efficient [3,48,49,52], where a piezoelectric material induces electrical strain in response to an applied gate voltage to facilitate switching from in plane to out of plane and vice versa.

In this paper, we model the aforementioned potentially compact and energy-efficient four-layer piezoelectric/magnet/TI/magnet (MTJ) stack, which we refer to as a strained-topological-insulator spin-orbit-torque random access memory (STI SOTRAM). We argue that this structure is naturally suited as a compact bit cell in an in-memory computing architecture. We employ stochastic Landau-Lifshitz-Gilbert (LLG) simulation to analyze the device dynamics. We present the device's functionality, the required phase space for stress generated by the piezo-induced strain and the gating magnet's anisotropy, and the writing condition's phase space (writing voltage vs time or delay) of the MTJ. We estimate the energy cost for gating and writing mechanisms and find that energy dissipation is significantly reduced compared to HM-based SOT switching, which indicates the benefits of utilizing TI as a spin source and an intrinsic gating mechanism as opposed to an access transistor traditionally used. Furthermore, we project the energy cost for 2-bit AND and OR operations, which shows lower-energy costs than traditional SOT switching. Finally, we show the impact of various material parameters on the device metric.



(d)

Operation	Write 0/1	Read
WWL	V_G/V_G	V_G
RWL	0	1
WBL	$V_D/\text{-}\ V_D$	0
RBL	0	I_{sense}

FIG. 1. (a) Schematic of a compact, low-power STI SOTRAM. An out-of-plane gating (selector) magnet gaps the bottom surface states of the TI and places the upper magnet in storage mode (left). The strain generated by the piezoelectric rotates the selector magnet from out of plane to in plane, restoring the bottom-layer surface states and activating the TI. The drain polarity V_D sets the storage bit with m_{2y} (bit "0") or $-m_{2y}$ (bit "1") using high SHA SOT (middle and right, respectively). The fixed layer of the MTJ reads the state as "0" (parallel) or "1" (antiparallel). (b) Equivalent resistance model of the TI. An out-of-plane gating magnet breaks the current path in the bottom TSS. (c) Schematic of a PIM crossbar architecture where each activated stack (bit cell) can be selected by activating the row column. Two selected bit cells can feed to a sense amplifier that processes the local inputs by comparing with a reference voltage or current and performing Boolean logic operations (e.g., AND, OR, etc.), thereby processing local data from the magnetic memory. (d) Biasing condition for read-write operations. WWL, write word line; RWL, read word line; WBL, write bit line; RBL, read bit line.

II. STI SOTRAM BIT-CELL DESIGN FOR PIM

Figure 1(a) depicts the schematic of the compact four-layer structure of the device comprising a piezoelectric/gating magnet/TI/MTJ stack in the vertical direction. The device contains a gating (selector) magnet at the bottom whose magnetization can be switched in and out of the plane of the TI in nanoseconds with a voltage-gated piezoelectric at a low-energy cost (approximately 10 aJ) [4,52,53]. An out-of-plane selector magnet gaps the bottom surface states of the TI, leading to breaking the current path [Fig. 1(b)] and places the upper MTJ free layer in storage mode [Fig. 1(a), left]. Activating the TI bottom surface with applied voltage restores the current path and drives the top MTJ free layer into one of three modes—(i) altering its magnetization with drain bias for data writing [Fig. 1(a), middle and right], (ii) discharging its stored magnetization state for data reading, the output set by its low (parallel) or high (antiparallel) resistance relative to the MTJ pinned layer; (iii) or execute a logic operation (e.g., bitwise AND, OR, etc.) using a sense amplifier [Fig. 1(c)]. Two selected bit cells can feed their voltage or current to a sense amplifier that processes the local inputs by comparing them with a reference voltage or current and performing Boolean logic operations. For example, for current-based sensing, if the current of the bit cells is I_c, AND and OR operations can be performed by selecting a reference current of $1.5I_c$ and $0.5I_c$, respectively. Similarly, we can choose different reference voltages for a voltage-based sensing scheme (discussed later). Since selector and storage magnets are co-located in a vertical geometry, the structure is scalable and naturally suited for a PIM architecture that preprocesses stored data locally, all with the same vertically integrated, compact bit cell as shown in Fig. 1(c). Figure 1(d) shows the biasing condition for various operations.

From Mars rovers to mine robots, edge computing avoids cloud access that is either unavailable or unreliable. Energy and latency are its main concerns. Our device gating energy is low because the strain is remarkably energy efficient, while our write energy is low because TIs offer a very high SHA. Our results (Fig. 5) show that at the individual bit-cell level, our device requires much lower energy (approximately 2–6×) than 45-nm dynamic and static random access memory (DRAM, SRAM) and HM-based SOTRAM with a lower or comparable speed (2 ns), further improvable with larger band-gap TIs. Moreover, at a PIM architecture level, we significantly outperform DRAM on both nonvolatility and energy cost

by rolling memory and logic into a single unit, reducing data-transit latency from approximately mm-cm data-bus lengths between separate memory-logic cores to just approximately μm-mm array dimensions, as the sense amplifier processes suitably segmented data from locally accessed storage magnets. At data-transfer rates of approximately Mbps-Gbps, this enables a 2–3× speedup over traditional Von Neumann architecture, in addition to the energy gain. Our device exploits the TI as a unique semiconducting channel that delivers high SOT without field assist for low-energy write and voltage gating with strain for low-power row-column select in PIM architecture.

III. METHODS

To characterize the magnetization dynamics in our device, we solve a coupled stochastic LLG equation in the macrospin limit using the fourth-order Runge-Kutta method. As explained in detail in Sec. II, the device consists of a piezoelectric/gating magnet/TI/MTJ heterostructure. We simultaneously solve the magnetization dynamics of the gating magnet and the MTJ free layer. In the case of the gating magnet, the LLG equation is described as

$$\frac{1+\alpha_1^2}{\gamma}\cdot\frac{\partial \mathbf{m_1}}{\partial t} = -\mu_0\cdot(\mathbf{m_1}\times\mathbf{H_{eff1}}) - \alpha_1\mu_0\cdot\mathbf{m_1}\times(\mathbf{m_1}\times\mathbf{H_{eff1}}), \quad (1)$$

where $\mathbf{m_1} = \mathbf{M_1}/M_{s1}$ is the normalized magnetization and M_{s1} is the saturation magnetization of the gating magnet. α_1, μ_0, and γ are magnetic damping coefficient, permeability of free space, and gyromagnetic ratio, respectively. We consider $\mathbf{H_{eff1}} = \mathbf{H}_{k1} + \mathbf{H_{stress}} + \mathbf{H_{th}}$, where $\mathbf{H}_{k1}$ and $\mathbf{H_{stress}}$ are the effective anisotropy field and stress field of the gating magnet, respectively [54,55]. $H_{k1} = (2K_{u1})/(\mu_0 M_{s1}) - M_{s1}$ (K_{u1} is the uniaxial anisotropy of the gating magnet). $H_{\text{stress}} = (3\lambda_s\sigma_s)/(\mu_0 M_{s1})$ (λ_s is the magnetostriction coefficient of the gating magnet, and σ_s is the stress generated by the electrical strain induced by the piezoelectric).

For the MTJ free layer, the switching is facilitated by the SOT arising from the TI, and the LLG equation takes the form:

$$\frac{1+\alpha_2^2}{\gamma}\cdot\frac{\partial \mathbf{m_2}}{\partial t} = -\mu_0\cdot(\mathbf{m_2}\times\mathbf{H_{eff2}}) - \alpha_2\mu_0\cdot\mathbf{m_2}\times(\mathbf{m_2}\times\mathbf{H_{eff2}}) - \frac{\hbar}{2e}\cdot\frac{\theta_{sh}^{\text{eff}}J}{M_{s2}t_{f2}}\cdot\mathbf{m_2}\times(\mathbf{m_2}\times\boldsymbol{\sigma}_\mathbf{p}), \quad (2)$$

where e is the elementary charge, $\hbar$ is the reduced Plank constant, θ_{sh}^{eff} is the effective SHA of the TI, t_{f2} is the thickness of the MTJ free layer, J is the surface current density of the TI, and $\boldsymbol{\sigma}_p$ is the unit vector along the spin-polarization direction. The other variables and constants have the same meaning as defined in Eq. (1), and a subscript of 2 represents the parameter for the MTJ free layer. $\theta_{sh}^{\text{eff}} = \theta_{sh}(1 - \text{sech}(t_{\text{TI}}/\lambda))$, where θ_{sh}, t_{TI}, and λ are the SHA, thickness, and spin diffusion length of the TI. In Eq. (2), $\mathbf{H_{eff2}} = \mathbf{H}_d + \mathbf{H_{th}}$. $\mathbf{H}_d$ is the demagnetization field of the in-plane MTJ free layer and expressed as $H_d = -M_{s2}[N_{dx}\ N_{dy}\ N_{dz}]$, where N_{dx}, N_{dy}, N_{dz} are the demagnetization factors of the free layer along x, y, z axis, respectively.

In both Eqs. (1) and (2), $\mathbf{H_{th}}$ is a random thermal field with zero mean ($\mu = 0$) and standard deviation

$$\text{SD} = \sqrt{\frac{2\alpha k_B T}{\mu_0^2\gamma M_s V\Delta t}}, \quad (3)$$

where α, M_s, and V are the damping coefficient, saturation magnetization, and volume of the respective magnets. Δt is the simulation time step, which is taken to be 10^{-12} for all the simulations. μ_0, γ, k_B, and T have their usual meanings.

Throughout our study, we use TbCo as both the gating magnet and the MTJ free-layer magnet, Bi_2Se_3 as the TI, and $Pb(Zr, Ti)O_3$ (PZT) as the piezoelectric materials unless otherwise specified. The used parameters are listed in Table I.

The modulation of the surface current density J of the TI by the gating magnet is modeled separately with an empirical function, described next.

TABLE I. Material parameters.

Dimension		
Length	L	20 nm
Width	W	40 nm
Gating magnet: TbCo		
Thickness	t_{f1}	2.5 nm
Saturation magnetization	M_{s1}	200×10^3 A/m [66,69]
Damping	α_1	0.4
Uniaxial anisotropy	K_{u1}	64×10^3 J/m^3 [10,66]
Magnetostrictive coefficient	λ_s	400×10^{-6} [65]
Young's modulus	Y	100×10^9 Pa [64]
MTJ-free layer: TbCo		
Thickness	t_{f2}	12.5 nm
Saturation magnetization	M_{s2}	400×10^3 A/m [69,75]
Damping	α_2	0.01
Topological insulator: Bi_2Se_3		
Thickness	t_{TI}	8 nm [10,36]
Spin Hall angle	θ_{sh}	3.5 [35]
Spin-diffusion length	λ	6.2 nm [76]
Conductivity	σ_c	$5.7\times10^4\ \Omega^{-1}$m^{-1} [35]
Piezoelctric: PZT		
Thickness	t_{piezo}	100 nm
Piezoelectric constant	d_{31}	1.8×10^{-10} m/V [3]
Max. strain	ϵ	1000 ppm (0.1%) [52]
Relative dielectric constant	ϵ_r	1000 [3]

IV. RESULTS AND DISCUSSION

The first functional block of the entire stack is the piezoelectric/gating magnet heterostructure. Applying a voltage to the piezoelectric (PZT), electrical strain is generated and transferred to the adjacent gating magnet (TbCo) via the magnetostriction effect. This strain is then converted into stress via the elastic modulus of the gating magnet, which counteracts the uniaxial anisotropy of the gating magnet. When the stress is sufficient, it can switch the gating magnet from out of plane to in plane with minuscule energy consumption in the order of approximately 10 aJ [4,52,53] (energy cost estimation for our device is shown later). The strain-induced switching of the gating magnet facilitates the opening and closing of the band gap in the TSS of the TI (Bi_2Se_3), depending on the out-of-plane and in-plane magnetization orientation of the gating magnet, respectively.

Figure 2(a) shows the magnetization dynamics of the gating magnet under the influence of the stress induced by the piezoelectric strain. We started with an out-of-plane magnetization ($m_{1z} = +1$) for the gating magnet, which corresponds to the OFF state of the device as it opens a band gap in the TSS and, hence, no current flow. Under the influence of stress, it takes a very short time, approximately 1 ns for the 90° switching ($m_{1z} = 0$) of the gating magnet for a stress $\sigma_s = 100$ MPa. The switching delay depends on the strength of σ_s and the material parameters of the gating magnet. The out-of-plane magnetization component (m_{1z}) is fed to the next block (TI) dynamically, which modulates the band gap in the TSS and, hence, the surface current. We consider a Dirac Hamiltonian form to model the surface state of the TI. In the presence of a magnet in proximity to the TI, the Hamiltonian can be expressed as $H = \hbar v_F(\boldsymbol{\sigma} \times \mathbf{k}) \cdot \hat{z} + M_0 \mathbf{M_1} \cdot \boldsymbol{\sigma}$ [5,56], where v_F is the Fermi velocity, $\mathbf{k}$ is the wave vector, $\boldsymbol{\sigma}$ is the Pauli spin matrices, M_0 is the exchange strength between the gating magnet and TI, and $\mathbf{M_1}$ is magnetization of the gating magnet. From simple algebra, for the case of an out-of-plane magnetization orientation of the gating magnet, we can show the energy dispersion takes the form $E = \pm\sqrt{\hbar^2 v_F^2 |k|^2 + (M_0 m_{1z})^2}$, where $|k| = \sqrt{k_x^2 + k_y^2}$. This gives rise to a band gap $E_{\text{gap}} = \sqrt{(2M_0 m_{1z})^2}$ at $k = 0$. The band gap will modulate the surface current of the TI as $I_{\text{surf}} = I_{0,\text{surf}} e^{-E_{\text{gap}}/k_B T}$, where $I_{0,\text{surf}}$ represents the surface current needed to switch the MTJ free layer for a specific switching delay. Figure 2(b) shows the evolution of the E_{gap} and the I_{surf} with time in response to the magnetization dynamics of the gating magnet [Fig. 2(a)]. Initially, when $m_{1z} = +1$, a band gap of $2M_0$ opened, and we get vanishing surface current. As the gating magnet switches ($m_{1z} = 0$) by the stress, the conductivity of the TSS is restored since the band gap is closed. We use $M_0 = 0.1$ eV, a typical value for Bi_2Se_3 [5,45]. Note that we cannot open an infinite band gap as it is limited by the bulk band gap of the TI (0.3 eV for Bi_2Se_3 [57,58]). We use $I_{0,\text{surf}} = 6I_{c,\text{surf}}$ while generating Fig. 2(b), where $I_{c,\text{surf}}$ is the critical surface current needed to switch the MTJ free layer.

We utilize an in-plane magnet-based MTJ for our device for primarily two reasons: (i) SOT can provide deterministic switching without an external field assist only for an in-plane magnet because of in-plane spin polarization (orthogonal to the charge current) [8,24,59], and (ii) we are limited by the interaction between the TI and the MTJ free layer as such an out-of-plane free layer will open the gap in the TSS and hence no current conduction [5–7]. While utilizing an in-plane magnet occupies more area than a perpendicular magnetic anisotropy (PMA) magnet, our design integrates the gating and storage magnets within the same stack. This configuration offers both area and energy-efficiency advantages, along with the added benefit of field-free switching. Extensive research is underway for field-free switching of PMA magnets. However, these require a graded structure or an added magnet that provides the symmetry-breaking field and adds structural complexity [60,61]. We use an in-plane magnet of "type y" (easy axis in y direction). The critical current density for switching J_c for this type of MTJ is expressed as [59,62,63]

$$J_c = \frac{2e\alpha_2 \mu_0 M_{s2} t_{f\,2}}{\hbar \theta_{sh}^{\text{eff}}} \left(H_{\text{in}} + \frac{H_{\text{out}}}{2} \right). \tag{4}$$

H_{in} is the in-plane shape anisotropy of the free layer, and H_{out} is the out-of-plane demagnetization component. The other variables and constants have the same meaning defined in Sec. III. Using the parameters listed in Table I, we find $J_c = 1.88 \times 10^{10}$ A/m^2, which is at least one order of magnitude less than conventional HM-based SOT switching [35,59] and laid the foundation of energy-efficient switching. This amount of critical current density needs to be supplied by the top surface states of TI for the switching of MTJ free layer, from which we can estimate the critical surface current $I_{c,\text{surf}} = J_c W t_{\text{surf}} = 0.75$ μA (W is the device width, $t_{\text{surf}} = 1$ nm is the thickness of the TI top surface [36]).

Figure 2(c) shows the magnetization dynamics of the MTJ free layer in response to the SOT generated by the TI surface current. We can clearly see the magnetization switching ($m_{2y} = +1$ to $m_{2y} = -1$) with a switching delay of approximately 4 ns for a surface current of $6I_{c,\text{surf}}$. Note that Figs. 2(a)–2(c) are generated in the absence of a thermal field. Figures 2(d) and 2(e) show the magnetization dynamics of the gating magnet and the MTJ free layer, respectively, under the influence of the thermal field for 50 simulation runs for the same current as without the thermal case, and we can see the stochastic behavior of the magnetization dynamics. Figure 2(f) shows the histogram from 1000 simulations runs, and we find a switching time of 10.75 ns, calculated by $t_{\text{sw}} = \mu + 6\text{SD}$, corresponding to

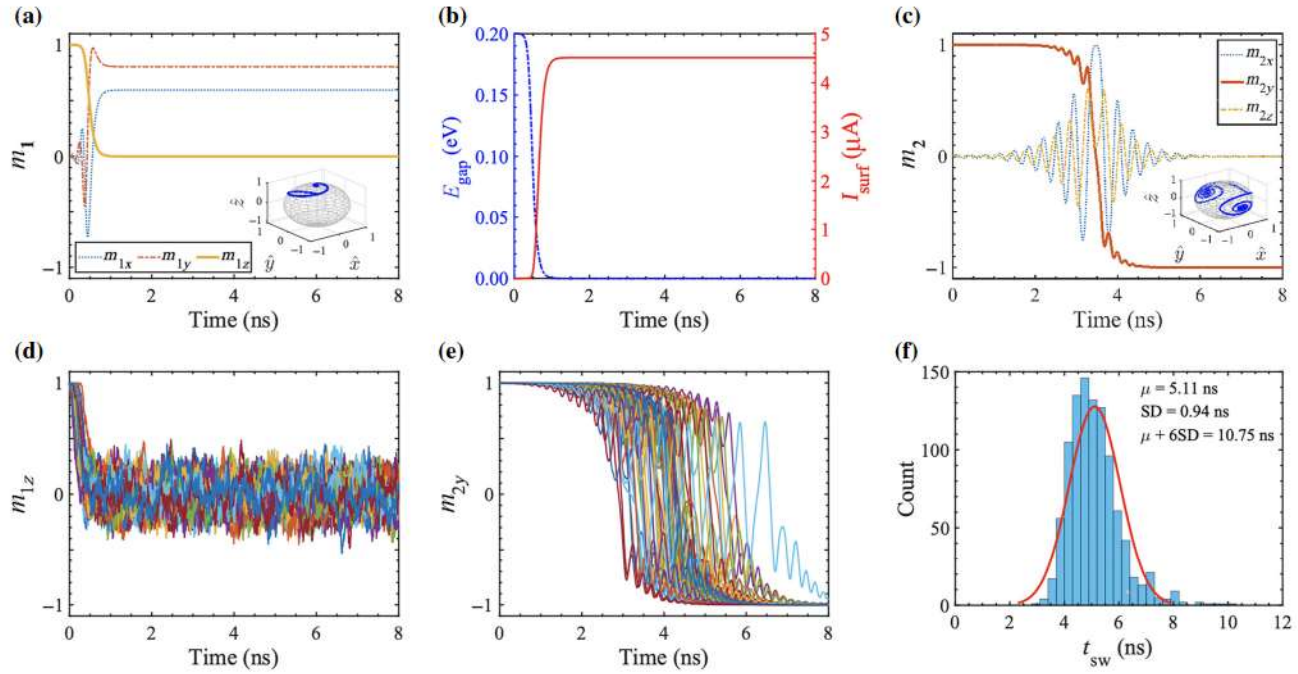


FIG. 2. Coupled LLG simulations showing gating magnet switching with strain (a), turning ON TSS (closing band gap) and hence delivering surface current (b), and switching the MTJ free layer with SOT (c) without the thermal field. (d),(e) Magnetization dynamics for the gating magnet and the MTJ free layer, respectively, influenced by the stochastic thermal field (50 simulations). (f) Histogram of switching time from 1000 stochastic simulations to estimate the switching time corresponding to WER $= 10^{-9}$. The switching time is calculated as $t_{sw} = \mu + 6$ SD from the histogram. The red curve is the Gaussian fit. The results are generated using $I_{0,surf} = 6I_{c,surf}$.

a write error rate WER $= 10^{-9}$, which is the industry standard for memory applications [28]. In the subsequent part of the paper, we calculate t_{sw} similarly unless otherwise specified.

Figure 2 demonstrates the functionality of the device. We will now delve into the details and constraints of the individual blocks. Beginning from the bottom to up, the piezoelectric-gating magnet stack enables the strain-driven out-of-plane to in-plane switching. As discussed earlier, the switching is governed by the competition between the uniaxial anisotropy energy and the stress energy induced by the strain. PZT typically can generate an electrical strain of $0.05\% - 0.1\%$ $(500 - 1000$ ppm) in response to an applied voltage [52], which sets the achievable stress-energy limit to counteract the anisotropy energy. The relation between the applied voltage and strain is $V_G/t_{piezo} = \epsilon/d_{31}$ [3,52], where V_G, t_{piezo}, ϵ, d_{31} are the applied gate voltage, thickness of piezoelectric, strain, and piezoelectric constant, respectively. The typical d_{31} constant for PZT is 1.8×10^{-10} [3]. TbCo has Young's modulus of 100 GPa [64] and $\lambda_s = 400 \times 10^{-6}$ [65], which gives a range of stress σ_s from 50 to 100 MPa. Figure 3(a) shows the gate voltage required for generating the strain (stress) for a 100-nm-thick PZT. The critical question is whether this stress is sufficient to overcome the anisotropy barrier. TbCo has a low uniaxial anisotropy K_{u1} of 64 kJ/m^3 [10,66]. Considering the demagnetization effect, the effecting anisotropy becomes 38.9 kJ/m^3 ($K_{eff} = K_{u1} - \frac{1}{2}\mu_0 M_{s1}^2$). Conversely, the stress energy $E_{stress} = \frac{3}{2}\lambda_s\sigma_s$ [54,55] ranges from 30 to 60 kJ/m^3 depending on the amount of strain (stress) shown in Fig. 3(a). Figure 3(b) presents the phase space for anisotropy and stress for the switching probability of the MTJ-free layer (colormap). The P_{sw} is calculated from 10^5 stochastic LLG runs [67] for 10 ns with a surface current of $6I_{c,surf}$. The figure illustrates the reciprocal relation between the K_{u1} and σ_s, and the range of K_{u1} and σ_s for a working device. This phase space is relevant because K_{u1} can be tuned by adjusting the composition of TbCo and alloying [68,69], while σ_s is adjustable through applied gate voltage.

Next, we consider the voltage requirement for the MTJ write operation (switching the MTJ free layer). For the write operation, three key quantities are the switching time, switching current or voltage, and WER. We calculate the switching voltage vs switching time for various stress values in Fig. 4, showing the typical reciprocal relation for spin-torque switching [70–72]. The switching voltage shown in Fig. 4(a) corresponds to WER $= 10^{-9}$. As σ_s increases, the out-to-in-plane switching time of the gating magnet is reduced, and it requires less time for the band gap to close, which is attributed to the lower overall switching time of the device. We vary the surface

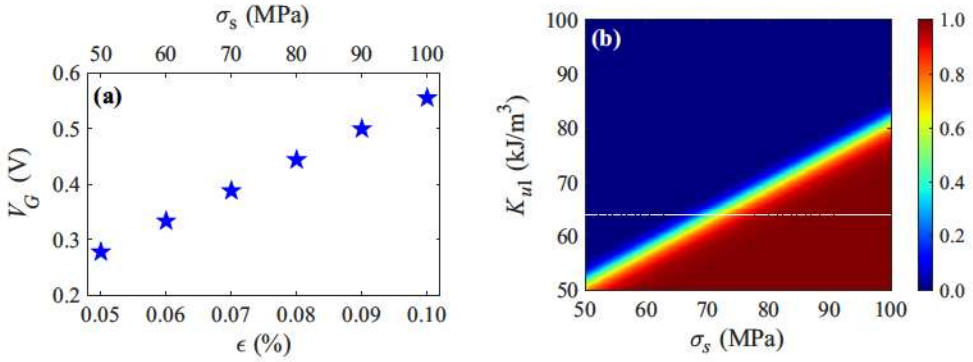


FIG. 3. (a) Gate-voltage requirement in the PZT to generate electrical strain (stress). The capacity to generate strain in the PZT limits the maximum achievable stress. (b) Gating magnet's uniaxial anisotropy vs stress phase space for the switching probability (colorplot) of the MTJ free layer. The probability of switching is calculated from 10^5 stochastic simulations. The dash-dotted line represents the TbCo uniaxial anisotropy ($K_{u1} = 64$ kJ/m^3).

current from 3.5 to 20 times the critical surface current and let the magnetization evolve until it reaches 95% of its final value ($m_{2y} = -0.95$) [73]. We denote the time as the switching time for the individual switching event, and from the switching-time distribution of 1000 simulations, we calculate the t_{sw} corresponding to WER $= 10^{-9}$. While calculating the total current requirement for the required surface current, we consider a $I_{surf}/I_{tot} = 15\%$ (see more discussion later).

Furthermore, we estimate the energy consumption for the switching process. The energy has two components: the gating energy and the switching energy. The energy associated with the gating mechanism comes from the applied voltage in the piezoelectric and can be estimated as $E_{piezo} = \frac{1}{2} C_p V_G^2$ [3,52], where C_p is the capacitance of the PZT, and V_G is the applied gate voltage. For the case of 0.1% strain, we get $V_G = 0.56$ V and $C_p = \epsilon_r \epsilon_0 WL/t_{piezo} = 0.071 \times 10^{-15}$ F (L is the length of the device, ϵ_0 and $\epsilon_r = 1000$ [3] are the permittivity of free space and the relative permittivity of PZT, respectively). We obtain $E_{piezo} = 11.13$ aJ, which is minuscule and

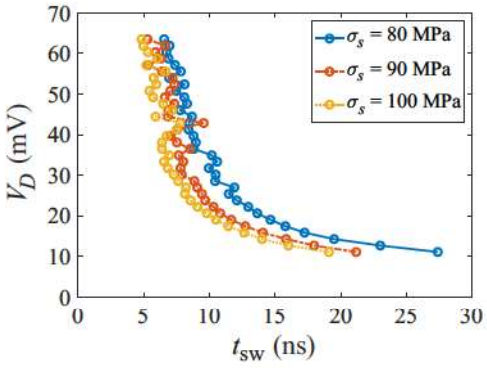


FIG. 4. Supplied drain voltage to the TI for write operation. We use $I_{surf}/I_{tot} = 15\%$.

consistent with previous studies [4,52,53]. The other part of the energy is the I^2R loss in the TI. TI is typically modeled as parallel surface and bulk channels (bulk channel accounts for the shunting through the bulk states) [36, 58]. The bulk resistance is $R_{bulk} = L/\sigma_c W t_{bulk} = 1.46$ kΩ, where σ_c is the average conductivity of the TI ($\sigma_c = 5.7 \times 10^4\ \Omega^{-1}\ \text{m}^{-1}$ for Bi_2Se_3 [35]), and t_{bulk} is the thickness of the bulk state of TI. We use $t_{bulk} = 6$ nm since the TI is 8 nm thick and the thickness of the top and the bottom surface is 1 nm each [36]. We estimate R_{surf} based on the current distribution in the top surface channel, which is found to be 30% of the total current as previously reported in both theory [58] and experiments [36]. This makes $R_{surf} = 1.94$ kΩ. Nonetheless, the bottom surface needs to be grounded through the gating magnet for the gating mechanism to work for our vertical structure [Fig. 1(b)]. Therefore, we divide the bottom surface resistance equally with a ground in the middle and estimate the equivalent resistance $R_{eq} = 633.5\ \Omega$, and eventually, we achieve 15% current through the top surface channel of the TI for the resistance configuration shown in Fig. 1(b). Shunting through the bulk in TI is an open question, and it requires materials with a higher band gap to get more current in the surface [58]. For high-speed applications, we want the switching time in single-digit nanoseconds [28,31,74]. We estimate the energy used in this operation regime. Figure 5(a) shows the voltage requirement for t_{sw} for 2–10 ns (WER $= 10^{-9}$), while Fig. 5(b) shows the energy consumption for the writing operation for a range of I_{surf}/I_{tot}. I_{surf}/I_{tot} can be varied by tuning the conductivity, bulk band gap, and thickness of the TI [36]. Our analysis suggests energy consumption in the TI is in the order of < 100 fJ, even with a low current ratio of 15% in the top surface, which is energy efficient compared to HM-based SOT switching [Fig. 5(c)], consistent with previous studies [10,35]. If we increase the top surface current, the energy consumption will be decreased further. Figure 5(c) shows

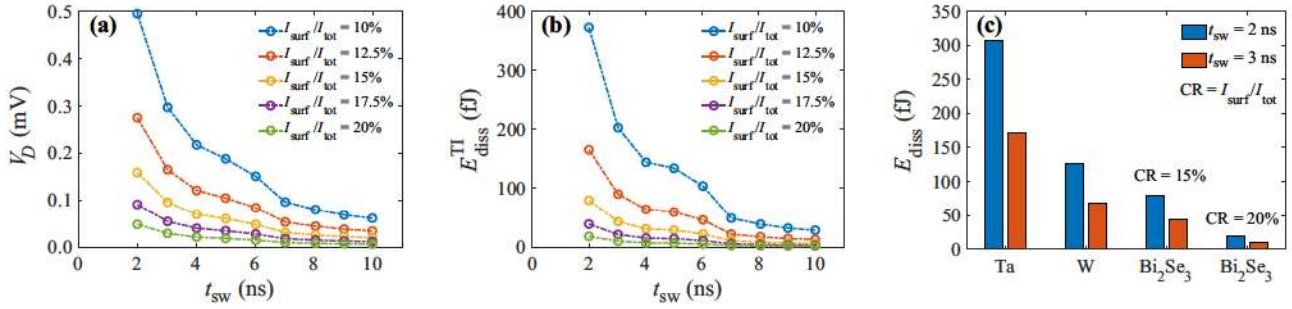


FIG. 5. (a) Drain-voltage requirement for high-speed switching (2–10 ns). (b) Energy dissipation in the TI during the writing process. (c) Comparison of energy dissipation between traditional HM- and TI-based SOT mechanism. TI consumes orders of magnitude less energy than the HM.

the energy-consumption comparison between HM- and TI-based switching, which shows an order-of-magnitude reduction in energy consumption for TI. Although the conductivity of HM is very high, the current dictates the I^2R loss, and TI requires a significantly low current because of its higher SHA [35].

The total energy consumption for writing operation $E_{\text{write}} = E_{\text{piezo}} + E_{\text{TI}}$, which is dominated by the E_{TI} because of the minuscule energy in the gating mechanism. This suggests the advantage of the stain-based intrinsic gating mechanism because it eliminates the need for an access transistor for the write operation, costs negligible energy, and has a reduced footprint compared to a CMOS access transistor. The energy consumption in TI will be much lower if we incorporate other TIs with higher SHAs. For example, for BiSb (SHA = 10 and $\sigma_c = 1.5 \times 10^5\ \Omega^{-1}\ \text{m}^{-1}$ [35]), the energy consumption is approximately 0.9 fJ and approximately 0.2 fJ for a current ratio of 15% and 20%, respectively, which is approximately 100× lower than Bi_2Se_3 and approximately 1000× lower than traditional HM.

The above-estimated write energy is at the bit-cell level. Now, we project the energy cost for a PIM array from the bit-cell energy. In particular, we show the projection for a 2-bit Boolean AND and OR operation using the PIM crossbar array [Fig. 1(c)]. Before doing the projection, we need to estimate the read energy cost. For reading operation, we use a small sense current $I_{\text{sense}} = 1\ \mu\text{A}$, significantly less than the write current, eliminating the risk of an accidental switch. We assume a resistance area product for the MTJ $R_PA = 2\ \Omega\mu\text{m}^2$ and a TMR = 100% [77], which makes $R_P = 2.5\ \text{k}\Omega$ and $R_{AP} = 5\ \text{k}\Omega$, respectively ($R_P$ and R_{AP} are the resistance of MTJ in parallel and antiparallel state, respectively). We consider a 16-nm PTM HP model for the read access transistor with a $R_{\text{ON}} = 5\ \text{k}\Omega$. We need to keep the gate voltage ON for the read operation so that the TI surface state is conductive, adding the gating energy during the read operation. Considering this, we found a read energy E_{read} of approximately 45 aJ and approximately 55 aJ for parallel (bit "0") and antiparallel (bit "1") states at a read speed of 4 ns [78]. For in-memory 2-bit AND and OR operations, we need to select two bit cells simultaneously, and the PIM operation is done by comparing the sense voltage from the bit cells with a reference voltage V_{ref} through a sense amplifier [see Fig. 1(b)], where V_{ref} is set to a value depending on the operation we want to perform. For two bit cells, we will have $\{R_{AP}, R_{AP}\}$, $\{R_{AP}, R_P\}$, $\{R_P, R_{AP}\}$, $\{R_P, R_P\}$ combinations in the resistance states of the MTJ, corresponding to sense voltages $\{V_{AP}, V_{AP}\}$, $\{V_{AP}, V_P\}$, $\{V_P, V_{AP}\}$, $\{V_P, V_P\}$. Setting a $V_{\text{ref}} = (V_{AP,AP} + V_{AP,P})/2$ ensures the sense amplifier will produce a logic "1" output only when both the bit cells are in the antiparallel state (logic AND). Similarly, for logic OR, $V_{\text{ref}} = (V_{AP,P} + V_{P,P})/2$ will serve the purpose. For the resistance and sense current used in our study, we get $V_{AP,AP} = 5$ mV, $V_{AP,P} = 4.29$ mV, $V_{P,AP} = 4.29$ mV, $V_{P,P} = 3.75$ mV, which give $V_{\text{ref, AND}} = 4.65$ mV; $V_{\text{ref, OR}} = 4.02$ mV. We can set the reference voltage by tuning the reference resistance of the sense amplifier, and therefore, we can perform reconfigurable in-memory computing by tuning the reference voltage. The energy components for a full-cycle (write-read) in-memory Boolean computing are summarized in Fig. 6, which shows that E_{write} is the dominant contribution. This suggests the energy efficiency of the STI SOTRAM bit cell for in-memory computing because the write energy of STI SOTRAM is much smaller than that of a conventional HM-based device, as shown in Fig. 5 (see the comparison with other emerging technology in Table II). Note that we assume a symmetric write operation [79] for both bits "0" and "1", and the energy associated with the sense amplifier is estimated as $\frac{1}{2}C\Delta V^2$, where C is the capacitance of the sense amplifier (typically 1 pF [80,81]) and ΔV is the difference between the sense voltage and the reference voltage. The estimated total area for the Boolean operation is 6720 nm^2, which includes the area of the bit cells and the read-access transistor ($W/L = 10/1$).

Finally, we present the effect of various key parameters on device switching time or delay t_{sw}. We show the effect of the thermal stability factor Δ_1 and damping coefficient

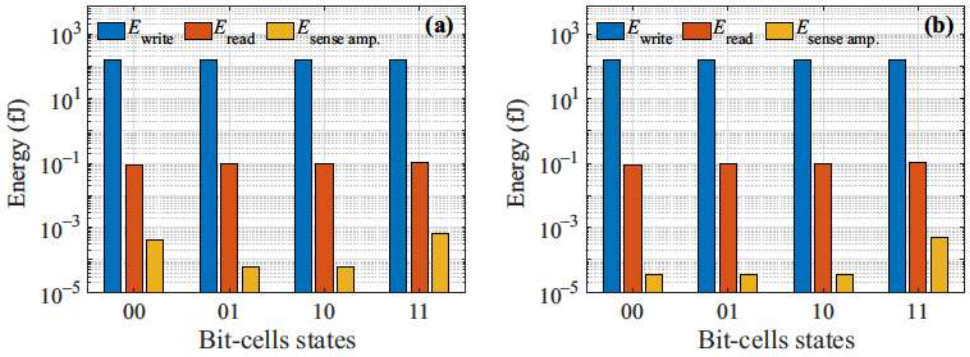


FIG. 6. Energy consumption for in-memory (a) AND and (b) OR operations. E_{write} and E_{read} are the combined energy for both the bit cells, while $E_{sense\ amp}$ represents the energy associated with a single sense amplifier.

α_1 of the gating magnet and the exchange constant between the TI and the gating magnet M_0 on t_{sw} for various σ_s values. In Fig. 7, the top panel shows the t_{sw} while the bottom panel shows the histogram of t_{sw} from 1000 simulations. For the case of varying Δ_1, as it increases, the switching time of the gating magnet will increase for a specific σ_s, which increases the overall switching time of the device. While for a higher α_1, t_{sw} reduces as the gating magnet switching time reduces with a large damping coefficient because the gating magnet dynamics is governed by precessional and damping torques. We note that the switching dynamics of the free-layer magnet are influenced by its damping coefficient (α_2), which directly impacts the t_{sw}. In the case of SOT-driven switching, particularly for an in-plane magnet, an increase in the damping coefficient increases the critical current density required for switching [see Eq. (4)], as damping acts as a resistive force opposing the switching process [59,72]. Consequently, a higher α_2 increases t_{sw}, while a lower α_2 reduces it for a given current density. Lastly, if we increase M_0, t_{sw} increases because the gap opening is larger, and it takes longer to provide sufficient surface-state current in the TI. Note that even if we get a large M_0, the TSS band gap cannot be infinitely large as we are limited by the bulk band gap of the TI. In contrast, we need a larger value of M_0 for a high ON-OFF ratio, which suggests the need for a TI with larger bulk band gap [45].

V. CHALLENGES AND OPPORTUNITIES

The above results show excellent promise for utilizing the STI SOTRAM for an energy-efficient bit-storage device. However, it is worth discussing the challenges associated with implementing STI SOTRAM devices. We will separate these discussions into two categories—material issues vs device issues.

A. Material challenges

Material issues exist [85] since we need three separate interfacial processes with input-output isolation—(a) strain

TABLE II. Stoplight chart for existing vs emerging memory technology [17,31,74,82–84]. Our device uses nonvolatile magnetic SOT technology, albeit with a superior TI underlayer with both a large SHA (> 10) for low-power write and a gate-tunable band gap for energy-efficient (approximately 10s of aJ) row-column select. The resulting vertical structure of the selector-storage stack (Fig. 1) is well suited for compact, low-latency in-memory edge computing.

	SRAM (45 nm)	DRAM	Flash (NAND)	Flash (NOR)	FeRAM	ReRAM	PCRAM	STTRAM	SOTRAM	STI SOTRAM
Memory type	Charge	Charge	Charge	Charge	FE capacitor	Oxide charge	VO_2, GST Bi_2O_2Se	Tunnel junction	Tunnel junction	Tunnel junction
Endurance	10^{16}	10^{16}	10^{4}	10^{6}	10^{10}	$10^{5}-10^{8}$	$10^{4}-10^{9}$	$>10^{15}$	$>10^{15}$	$>10^{6}$
Read time	1–100 ns	30 ns	~1 μs	~50 ns	<10 ns	<10 ns	<10 ns	<10 ns	<10 ns	<10 ns
Write time	1–100 ns	50 ns	0.1–1 ms	1 – 10 μs	~30 ns	<10 ns	~50 ns	<10 ns	<10 ns	<10 ns
Erase time		50 ns	0.1 ms	10 ms						
Write energy	~ fJ	~10 fJ	~10 fJ	~100 pJ	~100 fJ	0.1–1 pJ	10 pJ	~100 fJ	<100 fJ	1–100 fJ
Size F^2	50–120	6–10	10	5	15–34	6–10	4–10	6–20	6–20	15–25
Standby	Current Leakage	Refresh current	None	None	None	None	None	None	Field assist	No assist
High voltage	No	2 V	10 V	<10 V	<3 V	<3 V	<3 V	3 V	<1.5 V	<1V
Nonvolatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

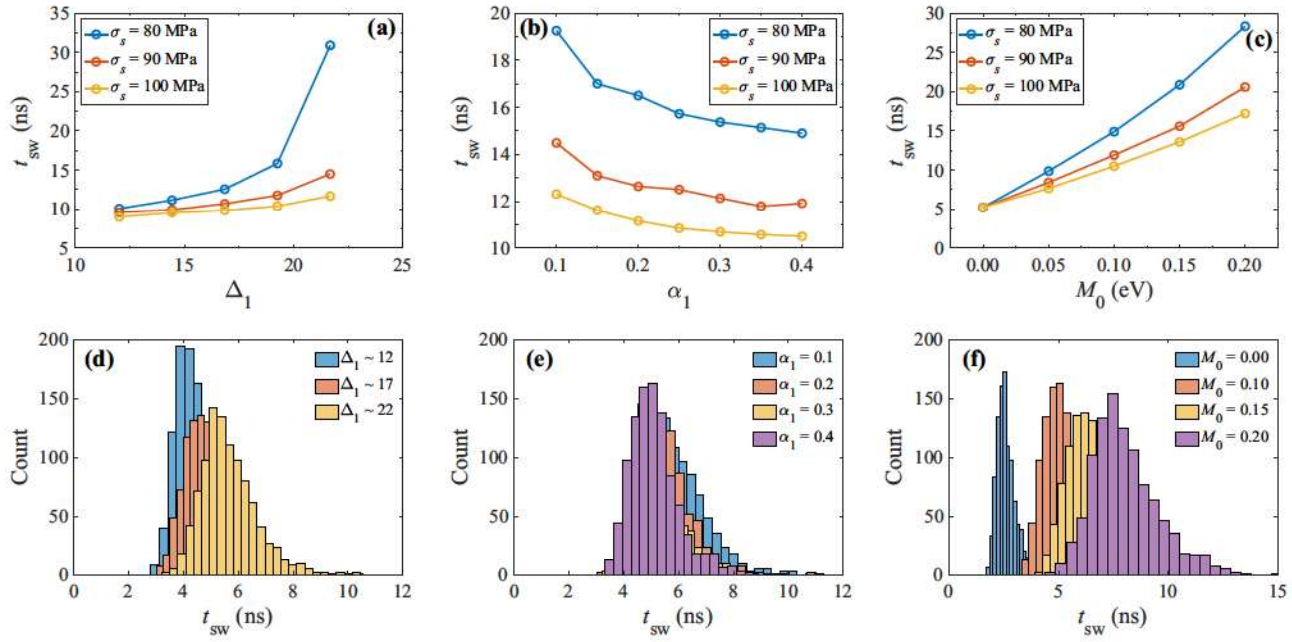


FIG. 7. Variation in switching time with respect to (a) the thermal stability factor of the gating magnet, (b) the damping coefficient of the gating magnet, and (c) the exchange strength between the TI and the gating magnet. (d)–(f) Histograms of the switching time from 1000 stochastic LLG simulations corresponding to (a)–(c), respectively. We use $I_{0,\mathrm{surf}} = 6I_{c,\mathrm{surf}}$ while calculating the t_{sw}.

rotating the bottom selector magnet, (b) modulating the TSS with such rotation, and (c) TSS writing information onto the top storage magnet. Let us discuss these three processes one by one.

(a) Can strain switch a magnet by 90°? The magnetocrystalline anisotropy density K_u is often larger than stress energy. We will need to compositionally tune sputtered magnets like amorphous TbCo [68,69,86], or tailor film thickness of epitaxially grown CoFe to approach a small K_u near the out-of-plane to in-plane crossover [87]. The resulting low K_u can be overcome with stress, while being large enough to avoid spontaneous thermal fluctuations. The condition for switching is $(3/2)\lambda_s\sigma_s > K_u$, where σ_s is the uniaxial stress. The magnets referenced above have magnetostriction coefficient $\lambda_s \sim 200\text{–}400 \times 10^{-6}$ [65,88] with elastic moduli approximately 100 GPa [64] and strain approximately 0.1%, which gives $(3/2)\lambda_s\sigma_s \sim 30 - 60$ kJ/m^3 and suggests successful switching of the magnetization if we can keep K_u lower.

(b) Can a rotated magnet kill the TSS? Theory [7] and experiments [6] show that an interfacing out-of-plane magnet opens a TSS band gap, leaving only chiral quantum anomalous edge states with significantly diminished spin-surface current. A 3D tight-binding-based study suggests the same, even accounting for bands along the patterned TI side walls [45]. Critically, the magnet must adjoin the TI, providing at least 50 mV exchange coupling. The g factor for the Zeeman gap is highly material dependent (approximately 18 for Bi_2Se_3, approximately 6 for Sb_2Te_2Se [89]), while that depends on bulk band gap due to the magnetic proximity effect (approximately 20 meV for EuS/Bi_2Se_3 [90], approximately 100 meV for $MnBi_2Se_4/Bi_2Se_3$ [91]).

(c) Can an activated TI write efficiently on the top magnet, accounting for small TI band gap and current shunting? SHA, even in sputtered TI, can be large (approximately 10–20, about 100× greater than conventional HMs, e.g., Pt), switching magnets very efficiently [35,92]. TIs have small bulk band gaps approximately 100–300 meV that shunt current into the bulk and sidewalls. However, previous studies suggest that even for a modest band-gap TI, an ON-OFF ratio of approximately 10 might be able to flip spins of a magnet with a low WER [45]. This self-correction happens through internal anisotropy fields [93], an increased band gap with thin-film quantization [35,94], and reduced charge current with gap opening. To avoid current shunting into the storage magnet, a thin layer of insulating NiO [95] or MgO [96] can be grown that transmits magnon torque between the magnet and TI, or else use an insulating $BaFe_{12}O_{19}$ as the storage magnet [97].

(d) Can we separate conductive bulk states from surface states in a TI? Critical to the success of our device is the ability to clearly isolate TI surface states from its conductive bulk states, and reliably place the Fermi energy roughly midgap. This is an ongoing topic of research where there has been considerable activity

but no consensus mechanism or widely accepted solution as of now, especially since typical TIs have small band gaps [98,99]. Specifically for Bi_2Se_3, the culprit can be unintentional vacancies and dopants, oxidation, and substrate-induced strain or charge transfer [100–103]. To avoid these effects, we need careful synthesis with precise control of stoichiometry [104,105], high purity Bi and Se precursors [106,107], Se-rich growth conditions [108] followed by postgrowth annealing and controlled cooling (quenching) to avoid vacancies [109,110], and a chemically inert or lattice-matched substrate [111]. Keeping the sample encapsulated (e.g., in *h*-BN) or in a vacuum or inert-gas environment would minimize exposure to air or oxidation [112–114]. Characterization tools such as x-ray phoelectron spectroscopy (XPS) can reveal the purity of the chemical composition [115], while angle-resolved photoelectron spectroscopy (ARPES) can provide information about the Fermi energy relative to the band edges [102,116,117]. A low carrier density ($< 10^{18}$ cm^3) measured in the Hall effect [118] and temperature-dependent resistivity measurements can distinguish between metallic and semiconducting states [36,99,103]. A subsequent reliable measurement of high SOT, as mentioned earlier in subsection (c), will likely be attributable unequivocally to dominant spin-polarized surface states [119,120]. Compensatory doping can be used to counterbalance unintentional doping [103,121,122], while resonant doping and proximity effects from magnetic layers can help further move and pin the Fermi energy towards midgap or the Dirac point [123,124].

(e) Can we grow and pattern the heterogeneous stack? To grow the stack with compatible processing temperatures, we will need to sputter the Bi_2Se_3 directly onto a magnet on a piezo, such as $Pb(Zr,Ti)O_3$(PZT)/$Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ (PMNT). Previous experiments show that amorphous TI retains band gap, topological protection, and high SHA [35,125,126], even after patterning with wet etching [127]. Besides mechanical decoupling, the stacks are also electrically decoupled, as the strains on a common piezo substrate stay localized around the contacts [4,128].

B. Device-circuit-architecture issues

Table II shows projected performance metrics for our device vs competing memory technology, especially for PIM and embedded applications.

(a) Key application space. Our device is similar to a DRAM crossbar, complementary to nonvolatile memory in the low-power and embedded space, and competitive in NAND space with similar trade benefits as MRAM and SOTRAM. It capitalizes on SOT technology, which is attractive as the last-level-embedded cache for digital AI and stand-alone off-chip cache for analog AI. The device uses a superior TI channel that is both spin selective with high SOT efficiency and gate tunable with low-power strain gating. For in-memory computing in embedded applications (image processing, combinatorial optimization) for edge intelligence, error tolerance and retention needs are low while energy and latency are premium. Our energy budget is low with write voltage < 100 mV for thin film (approximately 1 μm on conducting substrate)/2D monolayer piezos. Our device projects excellent metrics with approximately 2–3× improvement over DRAM in energy-delay products.

(b) Critical current and voltage. Our projected current density approximately 10^5–10^6 A/cm^2 is typical of STTRAMs and can be further reduced with higher SHA. Since the TSS are metallic in ON state (conductivity of BiSe approximately 8000–60 000 $\Omega^{-1}m^{-1}$), our room-temperature write voltage is projected to be < 100 mV.

(c) Back-end-of-the-line (BEOL) integration. TIs can be sputtered and wet etched while retaining high SHA, so usual BEOL metallization steps should work. Both TI and magnets should survive 85 °–100 °C processing temperatures. Thermal degradation of TI does not usually occur below 300 °C.

(d) Endurance, stability, and device-to-device variations. While HM-based SOTRAM endurance is approximately 10^{15}, piezo fatigue and TI endurance limit our STI SOTRAM device to approximately 5×10^6 cycles [129,130]. While this is significantly lower endurance, we believe this would suffice for hyperdense, nonvolatile persistent cells in PIM applications, where the probability of data overwrite per cell is very low (approximately 10^{-3}, easily error corrected [131]).

(e) Data retention, read disturb tolerance and scalability. The lower selector magnet needs small out-of-plane anisotropy for strain gating, while the upper storage magnet needs a higher barrier consistent with SOTRAM technology with 10-year retention. Like SOT, we avoid read disturbs with separate read-write paths (unlike SOT, we do not need field assist to circumvent stagnation, as our TI spins and storage magnet are in plane). The top MTJ requires ion milling and mesa etching, which the TSS are known to survive.

(f) Density. Our device footprint is similar to three-terminal SOT, slightly bigger than STTRAM, DRAM, and flash. We compete on density (and latency) by rolling storage and processing into one bit cell, along with nonvolatile magnetic storage and ultralow energy field-free write using strain gating (approximately 10 aJ), and high SHA (approximately 10), key metrics for embedded applications and edge intelligence.

VI. CONCLUSION

In summary, we demonstrated a four-layer piezoelectric/magnet/TI/MTJ bit-cell design with reduced energy cost and footprint for in-memory computing. Eliminating

an access transistor with a built-in strain-based gating mechanism has proved energy efficient, yielding an overall reduced energy cost. High-speed operation is achieved with significantly less energy than the traditional SOT metals at the device and array level. Our results suggest this heterogeneous stack may provide a compact and energy-efficient design for low-power, high-speed *in situ* applications.

The challenges at this time are the yet-to-be-demonstrated ability to fabricate the entire stack, the lower endurance associated with TIs (which is a lesser issue with PIM as the data overwrite per cell is low), ensuring the bulk-insulating properties of the TI itself, and the established challenges with SOT, such as higher footprint (again, PIM saves at the circuit level by rolling memory and logic into one unit), and higher current (but lower voltage since the HM has lower resistance). The in-plane spins help with field assist but hurt with scaling. Out-of-plane field-free switching has been demonstrated with SOTs and with Weyl semimetals [132–134].

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