A Low-Power Highly Reconfigurable Analog FIR Filter With 11-Bit Charge-Domain DAC for Narrowband Receivers

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***Abstract*—An innovative, highly reconfigurable charge-domain analog finite-impulse-response (AFIR) filter for high-channel selectivity receivers is presented. This filter demonstrates excellent reconfigurability to different bandwidths and desired stopband rejection and realizes the coefficients in the charge-domain with time-varying pulse widths controlling the on-time of the transconductor. The charge-domain finite impulse response (FIR) principle is derived step by step in this letter. The proposed filter, manufactured in 28-nm CMOS process, occupies a compact area of 0.05 mm^2, and its bandwidth can be reconfigured from 0.37 to 4.6 MHz. The filter can achieve −70-dB stopband rejection with a sharp transition ($-f_{-60\,\mathrm{dB}}/f_{-3\,\mathrm{dB}} = 4.5$) and low-power consumption of 0.356 mW.**

***Index Terms*—Analog filter, analog finite impulse response (AFIR), baseband analog circuits, channel selection filter, DTC, low power, low-pass filter (LPF), reconfigurable filter, ring-DTC, software-defined radio.**

I. Introduction

Programmable receivers have gained attention as the demand to support various wireless standards increases. The pivotal component is a reconfigurable baseband filter, which efficiently provides the bandwidth and rejection changes. For multichannel narrowband applications, these systems require high-channel selectivity, narrow bandwidth with tunability, low-power consumption, and good linearity. Fig. 1 shows a typical zero-IF receiver signal chain. The baseband circuits commonly utilize one gain stage followed by a high selectivity low-pass filter (LPF). Typically, this LPF is at least a first-order LPF to remove out-of-band (OOB) high-frequency signals. If the LPF stage utilizes an analog finite-impulse-response (AFIR) filter, it is also responsible for filtering out clock aliasing frequencies as they are otherwise only suppressed by the embedded sinc function rejection, which is typically much lower than the average AFIR rejection. Therefore, the AFIR filter primarily contributes to the OOB frequency rejection range within the first aliasing clock frequency. Moreover, since the AFIR filter is typically located in the last stage of the receiver chain before the analog-to-digital converter (ADC), the input-referred noise is substantially suppressed by the total receiver gain, making the noise requirement less of an issue. Therefore, the focus of AFIR filtering is to provide maximum flexibility of bandwidth and stopband rejection while maintaining good linearity and low-power consumption.

Various high-selectivity LPF techniques have recently been proposed [1], [2], [3], [4], [5], [6], [7]. This includes a gm-C-based coupled source-follower [1], charge-sharing infinite-impulse-response (CS-IIR) techniques [2], [3], [4], and a full-rate cascaded-AFIR filter [5]. Filtering-by-aliasing [6] and low-power AFIR filtering [7] are based on similar principles. They use either a time-varying resistor $R(t)$ or a transconductor $G_m(t)$ to generate finite impulse response (FIR) coefficients and integrate the signal in the integrator. However, [6] requires significant power consumption, making it impractical for low-power applications. Additionally, varying the resistor value generates significant kickback signals to the previous stage. Reference [7] achieves low-power consumption but suffers from significant parasitic caps and finite-impedance charge leakage due to the large transconductor implemented as a digital-to-analog converter (DAC).

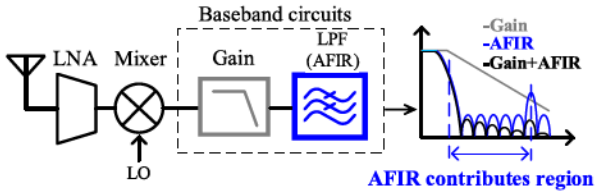

Fig. 1. High-channel selectivity receiver with AFIR.

This letter is an extension of [8], where we proposed a highly reconfigurable AFIR filter with a hybrid charge-domain DAC. A detailed derivation of the AFIR working principle and transfer function as well as additional measurement results are shown in this letter.

II. Charge-Domain FIR Approximation

The proposed AFIR structure leverages principles similar to those used in [6] and [7]. Fig. 2(a) illustrates the operation principle. The analog input signal X is first multiplied by the predetermined discrete time-varying coefficient h and accumulated within the integrator. Then, the output Y samples the accumulated signal at every N sample, where N is the number of FIR coefficients. The coefficient h represents the FIR impulse response and is transmitted at the f_{clk} rate, while the output samples the accumulated signal at the downsample f_{clk}/N rate. However, downsampling can lead to high-frequency signal aliasing to the in-band region, resulting in the distortion of the in-band signal. This issue can be mitigated by ensuring the FIR response sufficiently suppresses the aliasing signals, making them much lower than the in-band signals after folding to the in-band region.

High OOB rejection requires a high-resolution 11-bit DAC for quantizing the FIR coefficients. We propose a *hybrid* gm- and time-domain DAC to realize a combined 11-bit charge-domain DAC resolution with a small area and low-power consumption, as shown

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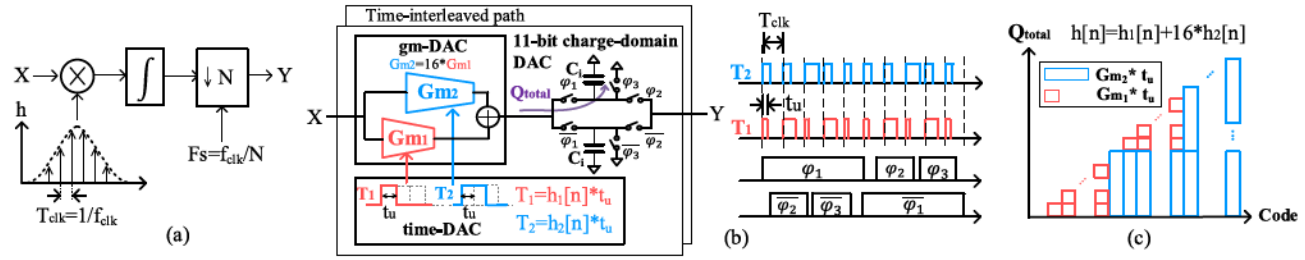

Fig. 2. (a) Hardware-efficient FIR. (b) Proposed AFIR filter with 11-bit charge-domain DAC and timing waveform. (c) Q_{total} versus code.

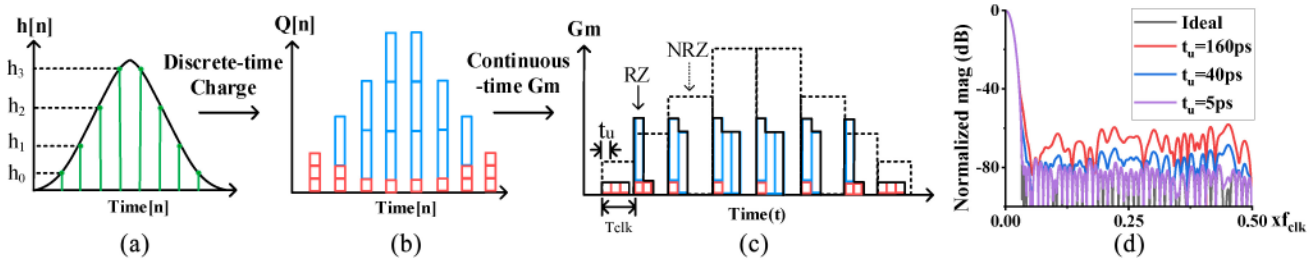

Fig. 3. (a) 8-tap FIR. (b) Q discrete-time mapping. (c) G_m continuous-time mapping. (d) Frequency response with different length of t_u.

in Fig. 2(b). The 11-bit resolution is divided into a fine-grain 4-bit DAC and a coarse 7-bit DAC using two paths (G_{m1} and G_{m2}) whose currents are summed together and integrated on capacitor C_i with total charge Q_{total}. Each path consists of a pulse-modulated Gm stage, where the coarse G_{m2} stage is 16 times larger than the fine-grain G_{m1} stage. Each stage is modulated by a pulse (T_1/T_2 with pulse width $h_1[n]/h_2[n]$). The pulse widths encode the nth coefficient code $h[n]$, where $h[n] = h_1[n]+16*h_2[n]$. T_1 and T_2 have maximum pulse widths of up to 15 and 127 time units (t_u) within one clock cycle T_{clk} for the 4-bit and 7-bit time-DAC, respectively. This dual-path implementation balances the gm/time dimensions, enabling higher bit-resolution implementation. Fig. 2(c) shows how the fine-grain and coarse DACs combine to form a single 11-bit DAC. During each clock period T_{clk}, both T_1 and T_2 fire their preprogrammed pulse widths. The charge on C_i is integrated across multiple clock cycles, representing the number of taps. Charge integration is performed during φ_1 ($\overline{\varphi_1}$), and the resulting value is then sampled at the output during φ_2 ($\overline{\varphi_2}$). The capacitor C_i is reset during φ_3 ($\overline{\varphi_3}$). Time interleaving allows the output to be sampled continuously, avoiding dead time during the reset phase.

Fig. 3(a) and (b) shows an example of simple 8-tap FIR coefficient mapping with the proposed charge-domain DAC. Each tap is implemented with discrete-time charge accumulation through the two paths. Fig. 3(c) illustrates the time-varying G_m value resulting from the differing on-times of the two Gm stages. The pulse-modulated approach yields in a "return-to-zero" (RZ) transconductance waveform [solid-black RZ line in Fig. 3(c)]. The Gm value returns to zero at the end of every clock cycle when both Gm stages finish the clock cycle in their off states. This contrasts with the conventional approach where the transconductance *strength* is modulated but the Gm stage remains on continuously [dashed-black NRZ line in Fig. 3(c)]. The proposed approach activates the gm-DACs only when necessary, resulting in power savings for the transconductor. Additionally, this approach mitigates excessive charge accumulation on the integrator, leading to a reduction in the capacitor area.

The general transfer function of the proposed charge-domain DAC can be written as

$$H(f) = \frac{g_m}{C_i}\sum_{n=0}^{M-1}\begin{pmatrix} M \times h_2[n]\text{sinc}(h_2[n]t_u f)\ e^{-2\pi f h_2[n]t_u} \\ +h_1[n]\text{sinc}(h_1[n]t_u f)\ e^{-2\pi f h_1[n]t_u}\end{pmatrix} \times e^{-2\pi f n T_{\text{clk}}} \quad (1)$$

where g_m is the transconductance of the fine-grain stage (G_{m1}), M is the ratio of G_{m2} to G_{m1}, and C_i is the integrator capacitance. There are two major differences compared to the conventional FIR transfer function [9]. First, the sinc function contains the time-varying coefficients $h_1[n]$ and $h_2[n]$. Second, there are two paths [G_{m2} and G_{m1} in Fig. 2(b)], each characterized by distinct complex values in the frequency domain. Improper handling of these two complex values may result in a nonideal overall FIR frequency response. However, if t_u is much shorter than T_{clk} and focuses on the low frequency, the sinc function can be simplified to

$$\text{sinc}(h_k[n]t_u f) \sim 1 \quad (2)$$

where $h_k[n]$ is the coefficient of either $h_1[n]$ or $h_2[n]$. Combining (1) and (2), the transfer function with a short t_u at low frequency can be approximated to

$$H(f) = \frac{g_m}{C_i}\sum_{n=0}^{M-1}(M \times h_2[n] + h_1[n])\ e^{-2\pi f n T_{\text{clk}}} = \frac{g_m}{C_i}\sum_{n=0}^{M-1} h[n]e^{-2\pi f n T_{\text{clk}}}. \quad (3)$$

This result is similar to the low-frequency approximation of the FIR frequency response reported in [9]. Fig. 3(d) shows the filter's frequency response simulation for the 96-tap/11-bit configuration with different lengths of t_u. As expected from the derivations in (1)–(3), narrowing t_u brings the filter response close to the ideal 11-bit quantization response [black line in Fig. 3(d)].

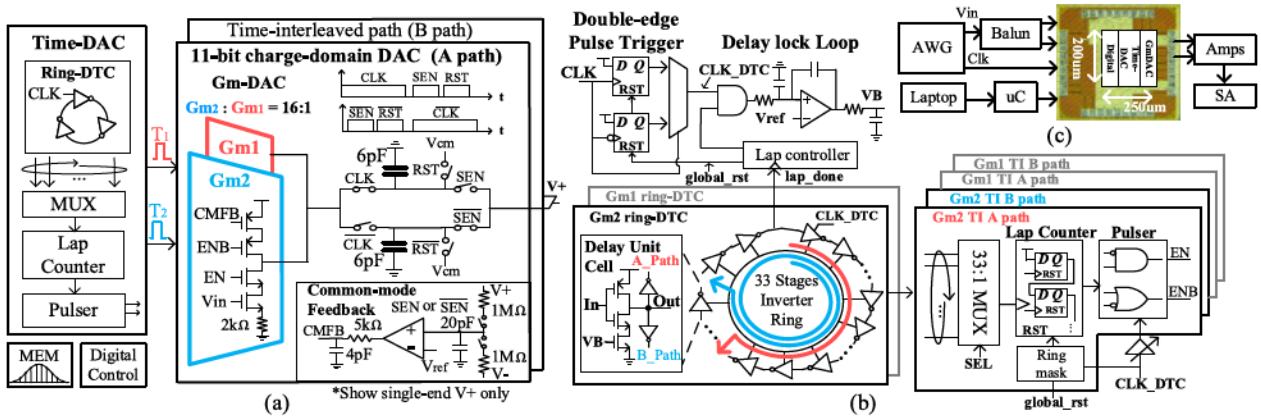

Fig. 4. (a) AFIR with 11-bit charge-domain DAC circuit architecture. (b) 7-bit time-DAC implementation. (c) Measurement setup.

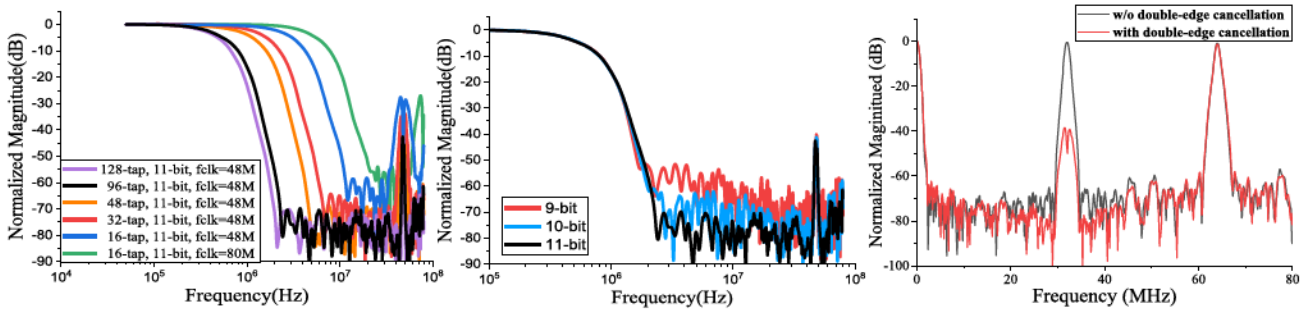

Fig. 5. (a) Measured bandwidth reconfigurability. (b) Measured OOB rejection reconfigurability. (c) Measured double-edge f_{clk} cancelation.

III. Circuit Implementation

Fig. 4(a) shows the proposed AFIR circuit architecture, featuring an 11-bit charge-domain DAC consisting of a gm-DAC and a time-DAC. The gm-DAC physically uses only 16 (G_{m2}) + 1 (G_{m1}) g_m units to generate the current to the integration capacitors, significantly reducing parasitic caps and charge leakage due to finite output impedance. For G_{m2}, transistors M_{0-2} are 6.4u/120n, while M_3 is 10u/120n. To enhance the g_m device linearity, the resistors are placed on the source side. The equal size of M_1 and M_2 balances the charge pushing from the p/nMOS switch parasitic caps to the output. Moreover, a differential structure is implemented to cancel out the residue charge pushing on both the V_+ and V_- sides. The ping-pong structure of the integration capacitors in the A path hides the reset delay and allows sampling at SEN ($\overline{\text{SEN}}$) duration. Hence, the sampling rate is already equal to the clock rate with one path, and with two paths (A/B path), it would double. Each path is equipped with dedicated common-mode feedback circuits to set individual path output common-mode voltages. The output common-mode signal is sampled with a ~10-kHz RC network (1 MΩ/15 pF).

Fig. 4(b) shows the time-interleaved time-DAC implemented with a ring-DTC structure, including a 33-stage inverter ring, a 33-to-1 mux, a 3-bit lap counter, and a pulser. The time-interleaved paths share the same ring-DTC to minimize path mismatch. The mux selects an output inverter stage and sends the rising edge to the lap counter, which tracks the number of laps completed by the ring and outputs the delay edge. The final pulse is generated by the pulser using the time difference between the reference edge and the delay edge. The digital controller controls the mux and lap counter to generate different pulse widths representing the FIR coefficients. Another lap counter with a fixed lap setting determines the maximum laps of the time-DAC, allowing programmability between 5 and 7 bits. The lap counter's output edge is sent to the delay lock loop (DLL), which controls the total delay between the reference edge and the delay edge by adjusting the inverter's bias voltage (VB). The time-DAC's unit pulse width is adjusted to around 60 ps to accommodate the rise and fall settling time of the g_m unit, and the DLL regulates the unit pulse width variation over PVT between 49 and 68 ps. The time-DAC achieves DNL/INL <0.15/0.3LSB over 200 Monte Carlo simulations. Finally, double-edge pulses are generated at both the rising and falling edge of the clock for odd-order aliasing clock frequency cancellation.

The simulation shows the filter response is slightly affected by the unit pulse width variations over PVT (min. stopband rejection variation <1.9 dB). However, the stopband rejection is sensitive to the gm- and time-DAC's mismatch. As a result, fine-tuning FIR coefficients are required to address the 11-bit DAC's mismatch during the measurement process.

IV. Measurement Result

The prototype of the proposed AFIR filter was fabricated in 28-nm CMOS process with a compact area of 0.05 mm^2. The measurement setup for the test chip is illustrated in Fig. 4(c). An arbitrary waveform generator provides synchronous single-end input and clock signals. An onboard balun converts the single-end input signal to differential signals and sets the common-mode voltage. The AFIR output signals are connected to the on-chip buffer, which isolates internal sampling nodes and drives the external amplifier connected to the spectrum analyzer. An internal bypass path is implemented to calibrate the frequency response and noise of the on-chip buffer to the spectrum analyzer path. In frequency response calibration, the bypass path's measured response is normalized and inversely applied to compensate for the main path result. Similarly, for the noise calibration, the bypass path's noise is first measured and subtracted from the main path's noise.

TABLE I
STATE-OF-THE-ART COMPARISON

	This work		JSSC'20[7]	JSSC'13[5]	JSSC'18[6]	JSSC'14[2]	TCAS'18[3]	JSSC'22[4]
Topology	CD-AFIR		AFIR	Cascade-AFIR	FA	CS-IIR	CS-IIR	CS-IIR
Reconfigurability[#]	9/10/11-bit + 16~128-tap		10-bit + 16[†]~128-tap	3-bit delay D_T	13-bit with varying Ts	0.25~64pF C_H + 0.4~2.2pF C_S	1~68.5pF C_H + 0.5~4pF C_S	1~19pF C_H + 0.5~4pF C_S + 1~6pF C_{IH}
Technology	28nm CMOS		22nm FDSOI	65nm CMOS	65nm CMOS	65nm CMOS	180nm CMOS	28nm CMOS
Supply (V)	0.8		0.7	1.2	1.2	1.2	1.8	0.9
Tunable BW (MHz)	0.37-4.6		0.06-3.4	5-26	1.25-20[+]	0.4-30	0.49-13	1-9.9
Min.Stopband Rejection (dB)	Low power (32-tap/ 10-bit)	Max rejection (96-tap/ 11-bit)	-60 (128-tap/ 10-bit)	-65.3	-70	-83[†]	-90[†]	-98[†]
	-60*	-70						
f_{-60dB}/f_{-3dB}	4.15*	4.5	3.8	1.5	3.3[†]	7.8[†]	7.5[†]	14[†]
Power(mW)	0.09*	0.356	0.092	8.4	75~99	1.98	4.3	0.92
IB OIP3[‡] (dBm)	25		-	13	31	31	28.7	32.4
OB OIP3[‡] (dBm)	43.7		28	-	44	21	32.63	41.3
OB OIP2[‡] (dBm)	60.5		-	-	87	69.3	73.48	-
Gain (dB)	23.5		31.5	41	23	9.3	17.6	14.7
IRN (nV/√Hz)	26[§]		12	12.3	-	4.57	6.54	3.5
Area (mm^2)	0.05		0.09	0.52	2.3	0.42	2.9	0.192

[#]Fix clock frequency; *fclk=16MHz; [†]Estimate from figure; [§]Integrated over 50k-460kHz; [+]Baseband BW; [‡]OIPn=IIPn+Gain;

In Fig. 5(a), the filter response demonstrates the bandwidth reconfigurability, which can be adjusted from 0.37 to 4.6 MHz [8]. This is achieved through a combination of 16–128 taps and clock frequencies of 48–80 MHz. Fig. 5(b) shows the OOB rejection reconfigurability with 96 taps and a clock frequency of 48 MHz. The charge-domain DAC allows reconfiguration from 9 to 11 bits, achieving rejection levels of −50 to −70 dBc [8]. Fig. 5(c) shows the double-edge cancellation for odd-order aliasing clock frequencies. The double-edge cancellation achieves −40-dBc rejection at the first aliasing clock frequency, complemented by around 10-dB rejection close to the clock frequency.

Table I summarizes the chip performance measured under an 800-mV supply voltage. All measurements were conducted at the 48-MHz clock frequency with the 96-tap/11-bit configuration unless specified otherwise. The proposed AFIR demonstrates two FIR coefficient configurations [8]: 1) high stopband rejection of −70 dB with a sharp transition (f_{-60dB}/f_{-3dB} ratio of 4.5) and 2) low-power consumption of 90 uW with −60-dB rejection at the 16-MHz clock frequency and the 32-tap/10-bit configuration. Compared with similar FIR works [5], [6], [7], this work demonstrates an improved OIP3 of 43.7 dBm, aided by the linearized g_m device. Compared with analog-IIR structures [2], [3], [4], this work utilizes a smaller area to demonstrate high reconfigurability without needing a large tuning capacitor area. The noise performance of the filter is affected by the small size of the g_m device and the accumulation clock jitter from the ring-DTC, especially for long pulse widths.

V. CONCLUSION

This work presents a highly reconfigurable AFIR filter featuring a novel 11-bit charge-domain DAC implementation. The proposed charge-domain DAC utilizes a low number of gm-DAC units with a highly programmable time-DAC, achieving −70-dB rejection with a sharp transition and low-power consumption of 356 uW in a CMOS process.

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