A Digitally Reconfigurable Low-Noise Amplifier with Robust Input Impedance for Machine Learning-Based Receiver Optimizations

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***Abstract*—The surge in demand for wireless connectivity has strongly incentivized advancements in reconfigurable radio frequency (RF) circuits. Although these circuits offer promising opportunities for machine learning (ML)-based optimization when devices are operating in the field, there is still an increasing need to adjust performance and power consumption over wider ranges, especially to dynamically minimize receiver power consumption when possible. In this paper, we present a novel low-noise amplifier (LNA) topology to dynamically scale power and performance to facilitate the realization of real-time ML methods for receiver optimization. This LNA is designed to avoid any significant input impedance matching degradation despite of a wide bias current tuning range to scale the gain, noise figure (NF) and input third-order intermodulation intercept point (IIP3). Simulations of the 2.4 GHz LNA design in 65 nm CMOS technology show its digitally-programmable gain from 17.07 dB to 28.15 dB, NF from 2.56 dB 5.18 dB, and IIP3 from -14.98 dBm to -9.85 dBm, while maintaining consistent input impedance matching with S_{11} < -13 dB.**

***Index Terms*—Tunable low-noise amplifier, RF front-end, machine learning-based receiver optimization.**

I. Introduction

The growing demand for wireless connectivity, coupled with the dynamic nature of communication environments due to mobility and interference, is increasingly straining the RF front-ends of receivers. This has spurred the development of RF circuits and devices with improved resilience to interference. Past researches on reconfigurable LNAs resulted in effective approaches to increase the capability of wireless receivers to operate under a wide variety of conditions. For instance, the adjustment of S_{11} allows to compensate for variations of the antenna interface or the CMOS fabrication process [1]–[4]. On the other hand, programmable gain can be implemented to dynamically adjust to changes of the received signal power and noise levels [5]–[8]. Furthermore, frequency tuning (including bandwidth and center frequency adjustment) is also becoming more important as a tool to mitigate channel congestion [9]–[12]. In addition, IIP3 tunability for LNAs has also been introduced for linearity enhancement in low-power RF front-ends [13]. To alleviate the impacts of process variations, circuit-level tunability is typically integrated into existing test and calibration methods to assure performance [14]–[16].

System-level wireless research has shown that combining ML and reconfigurable RF circuits can optimize the trade-offs between power efficiency and performance of the RF front-end [17]. For example, [18] has indicated that a deep reinforcement learning (DRL)-based framework can be utilized for training and real-time optimizations on embedded wireless Internet of Things (IoT) devices. Similarly, [19] presents a deep learning-driven receiver capable of real-time reconfiguration based on inferred waveform parameters. Building on these concepts, an envisioned ML-based reconfigurable receiver is visualized in Fig. 1, where a field programmable gate arrays (FPGA) or another digital processor will be employed to calculate output waveform parameters such as bit error rate (BER) and error vector magnitude (EVM) in addition to performing the standard baseband signal processing tasks. The processor, aided by an accelerator, can continuously execute lightweight ML models [20], e.g., DRL-based algorithms or tiny machine learning (TinyML), such that the power consumption is dynamically minimized depending on the ongoing channel conditions. One critical requirement to realize this framework is the design of tunable analog front-end circuits with a wide range to dynamically scale system-level performance and power consumption, while allowing digital control as indicated in Fig. 1. Modern tunable LNAs with calibration or reconfigurable operation are typically designed for optimal performance according to worst-case conditions specified in communication standards, which is not suitable for this framework where the goal is to minimize power consumption during times of operations based on the existing received signal and interference conditions. For example, it is desirable to dynamically reduce the power by a factor of 5-10 when the wireless system performance after demodulation is satisfactory, which is typically not supported by LNAs but is a capability of the proposed LNA topology. Note that the development of a ML-based real-time optimization framework also involves system-level challenges such as system modeling, algorithms development, performance metrics calculation, etc. These challenges are addressed through separate collaborative efforts and the scope of this paper is focused on the circuit-level aspects.

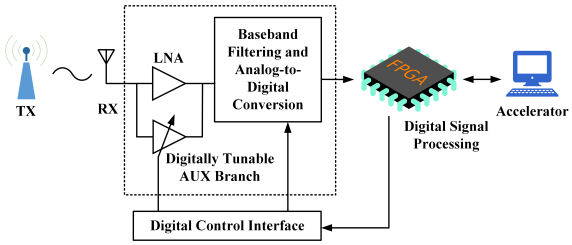

Fig. 1. Envisioned ML-based adaptive receiver with digitally-reconfigurable analog frond-end circuits.

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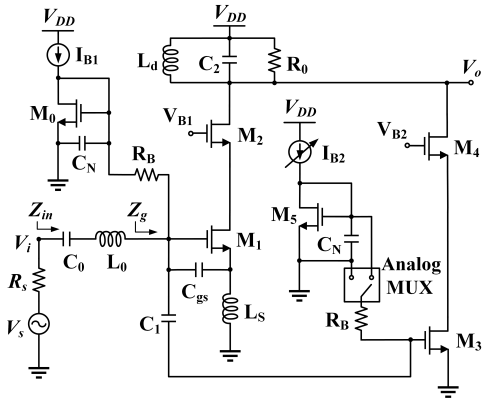

Fig. 2. Reconfigurable inductively-degenerated common-source LNA with an auxiliary branch for performance tuning.

In contrast to prior work, we have specifically designed a common-source LNA with inductive degeneration and inductor-capacitor (LC) tank load to accommodate a wide search space for ML algorithms with a wide range of performance tuning – and correspondingly a wide range to scale the power consumption through adjustment of the bias current. Normally, bias current tuning affects S_{11} significantly because of the corresponding transistor transconductance changes. In this paper, an auxiliary (AUX) branch is introduced to avoid this dilemma; allowing to tune gain, NF, and IIP3 with minimal impact on the S_{11} parameter.

II. Proposed LNA Topology

The LNA topology was designed with two branches, a main branch that continuously maintains input impedance matching, and an auxiliary branch for tunable gain, NF and IIP3. As depicted in Fig. 2, transistor M_1 in the main branch is biased with a static current source and transistor M_3 is biased with a digitally-programmable current. Both branches incorporate cascode devices (M_2 and M_4) to facilitate high gain, low noise and high reverse isolation. Here, L_0 (13.2 nH) and C_0 (1 pF) are assumed to be off-chip passive components as part of the impedance matching network, whereas L_d (5.7 nH; 283 μm x 288 μm and L_s (14 nH; 287 μm x 290 μm) are on-chip ultra thick metal (UTM) inductors with models from the process design kit (PDK). R_B (40 kΩ) and R_0 (5.9 kΩ) are on-chip poly resistors with salicide. C_N (5 pF), C_{gs} (80 fF) and C_2 (650 fF) are Metal-Insulator-Metal (MIM) capacitors, where C_N is for noise bypassing and C_2 for DC-blocking. R_s models the resistance of the input voltage source (i.e., antenna). An analog Multiplexer (MUX) is utilized to activate/deactivate the auxiliary branch based on performance requirements. When the analog MUX switch is connecting the gate of M_3 to ground, then the auxiliary branch is turned off, resulting in a low-power setting with 70 μA bias current (I_{B1}) in main branch. On the other hand, when the analog MUX switch closes the path to the gate of M_5, the auxiliary branch is activated and the bias current source I_{B2} supplies digitally-controlled current. In this prototype design, eight I_{B2} settings from 0 μA to 490 μA were implemented to demonstrate the design concept using the programmable current mirror described in Section II-D. This bias current range was selected as part of exploratory system-level receiver front-end simulations, which are outside of the scope of this paper. In practice, the number of settings can be changed depending on the ML algorithm. Note that the bias current I_{B1} in the main branch remains constant (70 μA) with stable transconductance of M_1 to avoid changing the real part of the input impedance generated under impact of the source degeneration inductor (L_s). The bias current in auxiliary branch will control the transconductance of M_3, leading to tunable performance with minimal impact on S_{11} because the source terminal of M_3 is connected to ground. Note that this topology avoids activating/deactivating multiple parallel segments of M_3 to circumvent parasitics and noise from switches directly in the signal path.

A. Input Impedance Analysis

The transfer function of the input impedance (Z_{in}) can be derived as in equation (1), where the key input impedance terms from the main branch are derived from the analysis of the conventional common-source cascode LNA with source degeneration [21]. The additional impact from the auxiliary branch in Fig. 2 is captured by the effective capacitance C_{AUX} from the gate of M_1 to the ground. In equation (1), C_{AUX} is in parallel with the impedance seen when looking into the gate of M_1. With proper design based on the equations following in this section and with careful layout of both branches in close proximity to minimize parasitics, C_{AUX} can be sufficiently low to ensure only negligible S_{11} variation during performance tuning.

$$Z_{in} = \left(sL_s + \frac{1 + sg_{m1}L_s}{sC_{gs1}}\right) // \left(\frac{1}{sC_{AUX}}\right) + \left(sL_0 + \frac{1}{sC_0}\right), \quad (1)$$

where $s = j\omega$, g_{m1} is the transconductance of M_1, C_{gs1} is the sum of M_1's parasitic capacitance and the MIM capacitor (C_{gs}) between gate and source of M_1.

To minimize the input impedance impact of the auxiliary branch during the design process, it is insightful to estimate the effective capacitance C_{AUX} in equation (1). Although the parasitic gate-to-drain capacitance (C_{gd3}) of M_3 has a tendency to be relatively small, it is worthwhile to consider its Miller effect because the gain from the gate to the drain of M_3 as well as the value of C_{gd3} vary during the bias current tuning in the auxiliary branch. In contrast, since the Miller gain in the main branch is constant with the fixed bias condition of M_1, its Miller capacitance is nullified through the resonance of the input impedance network during the selection of the design parameters in equation (1). As a result, the Miller effect's impact on S_{11} is negligible and normally neglected in the analysis of the inductively-generated common-source LNA (i.e., the main branch). Equation (2) allows the estimation of C_{AUX}, which depends on the bias current in the auxiliary branch that affects the transconductances of M_3 and M_4.

$$C_{AUX} = C_{gs3} + C_{Miller} = C_{gs3} + C_{gd3}A_{v,Miller} = C_{gs3} + C_{gd3}\left(1 + \frac{g_{m3}}{g_{m4}}\right), \quad (2)$$

where the g_{m3} and g_{m4} are the transconductance of M_3 and M_4 respectively; and C_{gs3} and C_{gd3} are the parasitic gate-to-source and gate-to-drain capacitances of M_3.

B. Gain Analysis

The input network of the LNA in Fig. 2 was designed to resonate at the frequency of interest, $f_0 = \omega_0/(2\pi) = 2.4$ GHz. Thus, the gain analysis can be made with the assumptions that the input impedance is matched at resonance ($Z_{in} = R_s$), and that $g_{m1}/C_{gs1} \approx \omega_T$ [21]. Furthermore, the value of the coupling capacitor C_0 is normally selected such that its impedance at f_0 can be ignored. The impacts of the cascode devices M_2 and M_4 were omitted during this gain derivation because the channel resistances of these transistors are significantly lower compared to their parasitic drain-to-source resistances and compared to R_0 [21]. The gain (A_v) from V_s to V_o can be estimated with equations (3) and (4), which were derived using the aforementioned assumptions. The gain increases when the auxiliary branch is activated, which is captured by the term with g_{m3}. When C_{AUX} is relatively small, then Z_g (the impedance seen at the gate of M_1) is predominantly determined by the passive matching network components and the constant transconductance of M_1. As a result, gain tuning can be achieved through the transconductance of M_3 with programmable bias current. Note that $sL_0 + 1/(sC_0) = Z_{in} - Z_g$. Therefore,

$$A_v = \frac{V_o}{V_s} = \left(g_{m1}Q_{in} + \frac{V_i}{V_s}\cdot\frac{V_g}{V_i}g_{m3}\right)R_{out} = g_{m1}Q_{in}R_0 + \frac{Z_{in}}{Rs + Z_{in}}\cdot\frac{Z_g}{Z_g + (Z_{in} - Z_g)}g_{m3}R_0 = \frac{g_{m1}R_0}{\omega_0 C_{gs1}(R_s + \omega_T L_s)} + \frac{Z_g}{2R_s}g_{m3}R_0, \quad (3)$$

$$Z_g = \left(sL_s + \frac{1 + sg_{m1}L_s}{sC_{gs1}}\right) // \left(\frac{1}{sC_{AUX}}\right), \quad (4)$$

where $Q_{in} = g_{m1}R_0/\left[\omega_0 C_{gs1}(R_s + \omega_T L_s)\right]$ is the quality factor of the input matching network [22], Z_g is the impedance looking into the gate of M_1, and Z_{in} is the impedance in (1).

C. Noise Analysis

The noise factor (F) of the proposed LNA can be estimated with equation (5), which captures the main thermal noise contributors and neglects the relatively small noise impacts of the cascode devices (M_2 and M_4). In addition to the noise from the main branch (derived in [21]), the auxiliary branch introduces noise mainly from M_3 but also increases the effective transconductance (G_m), where higher G_m reduces the input-referred noise as can be seen in equation (5).

$$F = 1 + \frac{g_{m1}\gamma}{4R_s G_m^2} + \frac{1}{R_s R_0 G_m^2} + \frac{g_{m3}\gamma}{R_s G_m^2} \quad (5)$$

$$G_m = \frac{g_{m1}}{\omega_0 C_{gs1}(\omega_T L_s + R_s)} + \frac{Z_g g_{m3}}{2R_s} \quad (6)$$

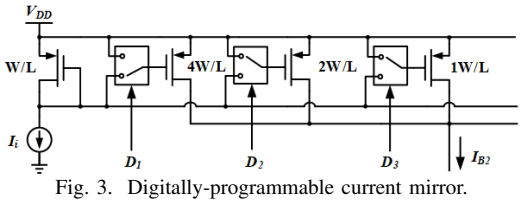

Fig. 3. Digitally-programmable current mirror.

where γ is the noise coefficient, and G_m is the effective transconductance of the LNA.

D. Digitally Programmable Current Mirror

To control I_{B2} in the auxiliary branch, the bias current is generated with a digitally controllable current mirror to validate the performance reconfigurability over a large tuning range. The programmable current mirror was designed for binary-coded CMOS logic levels. As depicted in Fig. 3, I_i is the static reference current, which has a value of 70 μA in this example design. I_{B2} is the tunable bias current for the auxiliary branch, ranging from 0 μA to 490 μA. The analog MUXs are controlled by a binary code word ($D_1D_2D_3$) to activate certain current sources that are summed together for the generation of I_{B2}. The layout design for the current mirror should also incorporate device matching techniques to ensure accurate bias current generation. In the discussed example, the maximum and minimum bias current values occur with $D_1D_2D_3 = [111]$ and $[000]$ respectively, where a "1" indicates that the gate of the corresponding transistor connects to the gate of the diode-connected reference transistor, and a "0" designates that the gate is connected to V_{DD}. The DC current ratios between the output branches and reference current are approximately equal to the ratios of the labelled widths and the reference transistor. For example, a code of $D_1D_2D_3 = [001]$ results in an output current of 70 μA.

III. Simulation Results

Schematic simulations were carried out using Cadence Spectre and foundry-supplied device models from TSMC 65 nm CMOS technology. The effects of package (C_{pack}), bonding wires(L_{bond}) and pad parasitics were modeled with 250 fF, 1 nH with 50 mΩ, and a standard TSMC RF low-capacitance pad model, respectively. The LNA in Fig. 2 was designed with 1.0 V supply with a 2.4 GHz center frequency as a proof-of-concept. The analog MUXs were all implemented with standard transistors used as switches. The bias current in the auxiliary branch has eight settings between 0 μA to 490 μA with a step size of 70 μA, while the bias current in main branch is constant at 70 μA. Hence, the total LNA current ($I_{B1} + I_{B2}$) ranges from 70 μA to 560 μA. In the future, we anticipate to add more steps for ML-assisted tuning.

Fig. 4 shows the frequency responses of gain (S_{21}), NF and S_{11} for the total of six different total bias currents. The IIP3 simulations were completed using periodic steady-state (PSS) analysis with tones at 2.400 GHz and 2.401 GHz. Although the tuned parameters do not follow straight curves vs. the controlling bias current, the characteristics still enable effective ML-based optimization [23]. The convergence of ML algorithms depends more on the tuning range and monotonicity

TABLE I
COMPARISON WITH OTHER RECONFIGURABLE/TUNABLE LNAS

Metric	This work**	JSSC 2018 [24]*	RFIC 2017 [25]*	TCASII 2020 [26]*	ISCAS 2017 [27]*	JSSC 2020 [28]*
Gain [dB]	17.07 ∼ 28.15	17.4	13.9 ∼ 26.3	4 ∼ 10	14.8	11
NF [dB]	2.56 ∼ 5.18	2.8	5.5 ∼ 8.9	4	3.7	6.8
IIP3 [dBm]	-14.98 ∼ -9.85	-10.7	-24 ∼ -13	0	-3.7	-2.2
Technology [nm]	65	65	65	180	110	65
P_{DC} [mW]	0.07 ∼ 0.56	0.475	0.064 ∼ 0.069	0.6	0.336	0.174
Center Frequency [GHz]	2.4	2.4	2.4	2.8	1.8	2.4
V_{DD} [V]	1	1	0.6	0.6	1	0.5
FoM [dB]	32.41 ∼ 34.11	28.8	28.16 ∼ 32.58	28.21	31.58	30.2

*Measurement Results **Simulation results

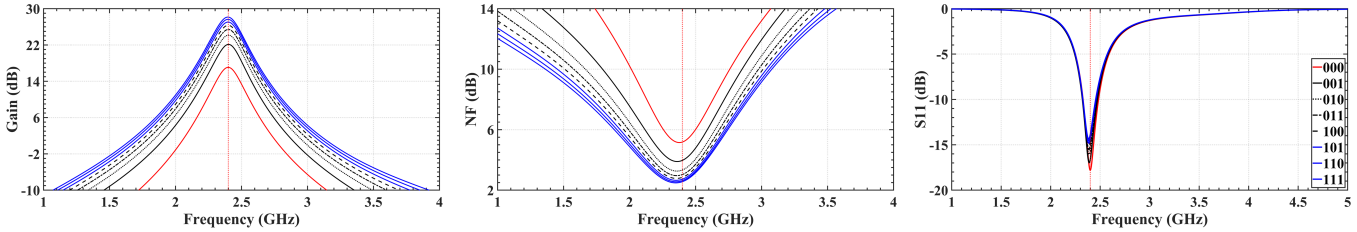

Fig. 4. Frequency responses of key parameters for the six bias current settings.

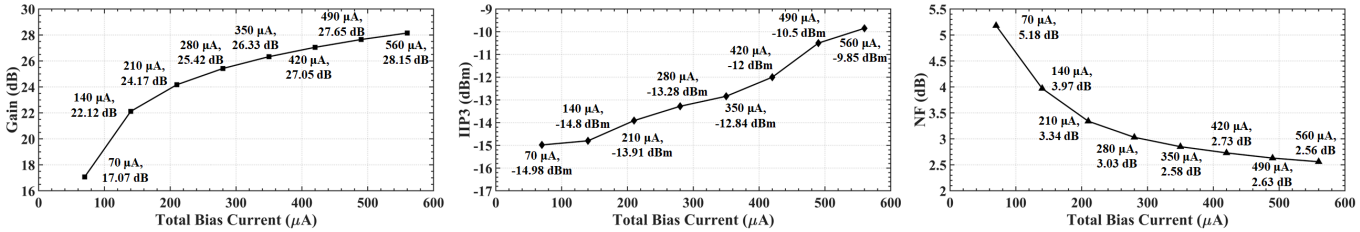

Fig. 5. LNA performance parameters at 2.4 GHz vs. total bias current.

than on linearity. A large tuning range will compensate for the nonlinear characteristics. The simulation results show that the gain and S_{11} remain centered at 2.4 GHz despite of the varying bias current in the auxiliary branch. Normally, when tuning the bias current in the conventional LNA topology, the optimal point of S_{11} shifts away from 2.4 GHz because of the changes of the transconductance and thereby the input impedance. Based on simulations of a conventional common-source LNA with source degeneration, the S_{11} of the reference design varied by 20 dB at the center frequency when tuning the bias current over the same range as the proposed design. As can be seen in the Fig. 4, the impact of the auxiliary branch on S_{11} is minor thanks to the design characteristics explained in Section II. Fig. 5 shows the changes of gain, NF and IIP3 vs. total bias current. As the total bias current increases, the gain increases from 17.07 dB to 28.15 dB, and the NF decreases from 5.18 dB to 2.56 dB. The IIP3 improves by 5 dB from the lowest to highest current setting.

Table I compares the presented LNA design with other LNAs from the literature, which were selected based on their performance reconfigurability/tunability and low power consumption during narrowband operation with similar center frequencies. It can be observed that the LNA from this work offers relatively wide performance tuning with large associated range of power scaling. This large tuning range increases the search space of ML-based RF front-end optimizations by providing more possible solutions to converge to under different conditions and variations. With signal and interference changes in the communication channel, a larger tuning range will also provide enhanced system level performance to balance between power consumption and receiver performance. The figure of merit (FoM) calculations in Table I are based on the following equation from [24]:

$$FOM(dB) = 10log(\frac{10^{Gain/20} \cdot 10^{(IIP_3-10)/20}}{10^{NF/10} P_{DC} \cdot 10^{-3}}), \quad (7)$$

where Gain, NF is in decibel, IIP_3 is in dBm, and P_{DC} is in milliwatts. Both, the low-power and high-power modes, have high FoM-based performance compared to other reconfigurable low-power LNAs.

IV. CONCLUSION

This paper introduced a new digitally tunable LNA topology for reconfigurable RF receiver front-ends enabling ML-based optimizations to scale power based on momentary performance needs. Based on simulations, the LNA was able to achieve adjustable gain from 17.07 dB to 28.15 dB, NF from 5.18 dB to 2.56 dB, and IIP3 from -9.85 dBm to -14.98 dBm. The simulation results show that the input impedance matching conditions are preserved during the reconfiguration. The consistent S_{11} performance allows more flexibility to adjust key performance parameters and power consumption over wider ranges for future real-time ML-based optimizations.

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