Reduce-Order Analysis and Circuit-Level Cost Function for the Numerical Optimization of Power Electronics Modules

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***Abstract*—Energy innovation trends such as sustainable grids, and the electrification of the consumer transportation market are accelerating the adoption of medium-voltage (MV) silicon-carbide (SiC) technology. The fast switching times and higher operating temperatures enabled by MV SiC have forced package designers to employ innovative technologies to improve power densities, lower stray parasitics, and increase cooling capability. These new technologies ultimately require new simulation tools to allow for fast, efficient, and accurate computation of the multi-physics phenomena that govern package performance. To that end, this work proposes a multi-physics optimization workflow that utilizes reduced-order 3D package models and behavior circuit models to efficiently quantify the effects of the package on converter performance. A cost function is proposed which utilizes the information to optimize for converter performance, rather than individual package parameters.**

***Index Terms*—silicon carbide, double-sided cooling, high density, finite element analysis, thermomechanical stress**

I. Introduction

With the electrification of transportation, the growing need for renewable and sustainable energy sources, and the miniaturization trends in modern power electronics, SiC has emerged as an alternative to silicon technology due to its faster switching times and reduced on-state losses [1]. To fully utilize the advantages of MV SiC devices, innovative packaging solutions are required to support the higher voltage and temperature of these devices, reducing stray parasitics and thermal impedances, and offer protection from environmental hazards such as moisture and corrosion [2]. This new generation of advanced packages utilize new materials, processes, and test procedures, which result in tightly coupled systems where thermal, mechanical, and electrical performance are interdependent [3]. Design areas such as electrical performance, reliability, cooling systems, and manufacturing which could once be designed by separate teams, must now be designed in the same room, and in some cases, the same equation [4].

Historically, modeling the mechanical, thermal, and electrical in a coupled (i.e., multi-physics) environment is a challenge, even with modern simulation tools such as ANSYS and STAR-CCM+ [5], [6]. Typically, several versions of the model must be built in several different simulation suites, which are then linked together with extensive scripting. Once the physical phenomenon is simulated, some form of lumped circuit model is usually exported for use in a circuit simulation suite. Shortcomings of this approach include the cost of the software packages, complexity of the integration, lack of automation, and the single-point lumped circuit models [7]. The single-point circuit model is a disadvantage because it models the package at a single operating point (e.g., at a single temperature or operating frequency). In order to analyze the circuit at a different operating point, the physical phenomenon must be re-simulated, and a new lumped circuit model must be exported [5].

This work seeks to improve the multi-physics design workflow in two ways. First, circuit and physical phenomenon simulation is integrated into a single tool by means of an accelerated, reduced-order electro-thermal model as implemented in [8]. This removes the need for the "simulate-export-simulate" workflow across multiple simulation suites and allows for a fully automated workflow, including model generation, simulation, and post processing. Second, a cost function is proposed which utilizes the coupled physics solutions from the lumped-component analysis to calculate circuit- and converter-level parameters from which to optimize the package. The advantage of this technique is the package is optimized from the standpoint of how it performs in a converter rather than abstract package-level parameters such as stray inductance, which, while related to converter performance, are not as insightful. The result is a workflow that offers reduced design cycle time, improved simulation capability, and more optimal package designs.

II. Theory

A. Electromagnetic Simulation

The reduced-order analysis uses a unified model structure as shown in Figure 1, where each set of physics (thermal, electromagnetic, etc.) is driven by the same parametric model. The analysis uses the Finite Difference Method (FDM) and Partial Element Equivalent Circuit method (PEEC) to generate

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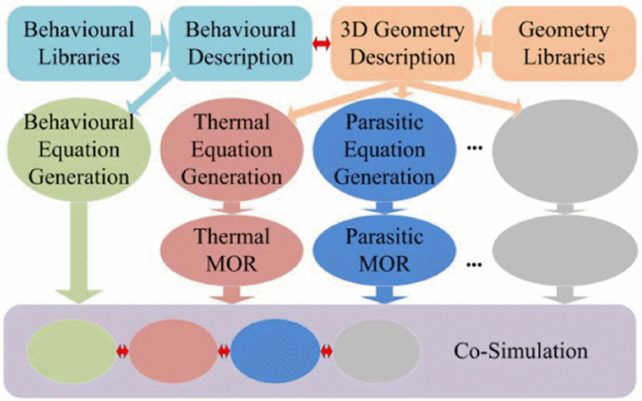

Fig. 1. Structure and data flow of reduced order multi-physics simulation software package.

3D thermal and electromagnetic models respectively [9]. The geometry for each design iteration is automatically meshed in both thermal and electromagnetic domains before a Model Order Reduction (MOR) technique based on Krylov subspace projection is applied to both models [10], which greatly improves the speed of the time domain simulation by up to 100x when compared to commercially available FEM and FDM solvers [8].

One of the primary advantages of this modeling approach is it allows for co-simulation of the thermal and electromagnetic properties of the package with behavioral circuit models, similar to those used in SPICE. This allows the designer to simulate how a semiconductor device would perform in a circuit, while considering the electrical and thermal properties of the package. Given the time-domain switching behavior of the semiconductor devices, a cost function can be constructed that utilizes this information to optimize device performance in a converter.

B. Objective Function

In this work, a cost function is proposed which utilizes the time-domain results from the PEEC simulation to quantify the effect of the package on converter performance. The cost function is formulated as shown in Eq. 1 as the sum of three components: 1) a device lifetime term f_T which quantifies the peak junction temperature, 2) an efficiency term f_E which quantifies device and packages losses, and 3) a noise term f_N which attempts to quantify all undesirable impedances within the package over a broad frequency spectrum.

$$f = f_T + f_E + f_N \tag{1}$$

Of the three terms in the objective function, the noise term f_N is the new contribution of this work. It replaces the more conventional impedance term with one that represents all of the stray impedances in the package, the coupling between them, and the variation over spectrum, as opposed to conventional impedance optimizations that use a single reactance (typically commutation inductance) at a single frequency.

This term is calculated by first running a baseline circuit simulation as shown in Figure 2 where the device model is setup for continuous switching at a frequency of $f_{sw} = 1/T$. In this simulation, no 3D geometry or package parasitics are taken into account, only the device model and the required external components, such as the external gate resistance R_{gext}, and the ideal source voltage V_{bus} and load current I_{nom}. The baseline power of the noise spectrum on the gate P_{go}, the jumping node P_{ao}, and the dc bus P_{bo} are then calculated as follows

$$\begin{aligned} P_{go} &= \int_{f_{LB}}^{f_{UB}} |\mathcal{F}\{i_{go}\}| df \\ P_{ao} &= \int_{f_{LB}}^{f_{UB}} |\mathcal{F}\{v_{ao}\}| df \\ P_{vo} &= \int_{f_{LB}}^{f_{UB}} |\mathcal{F}\{i_{bo}\}| df \end{aligned} \tag{2}$$

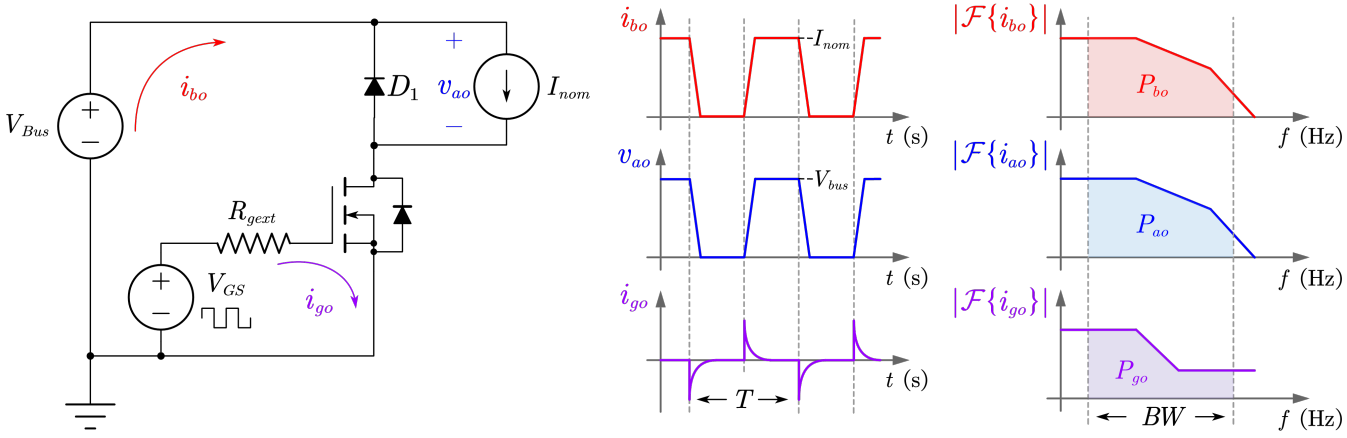

Fig. 2. Calculation of the baseline noise spectrum by simulating the device model in a continuous switching test without any effects of the package, capturing the bus current ripple, output voltage ripple, and gate current ripple, and integrating the spectrum with respect to frequency over a specified bandwidth (BW).

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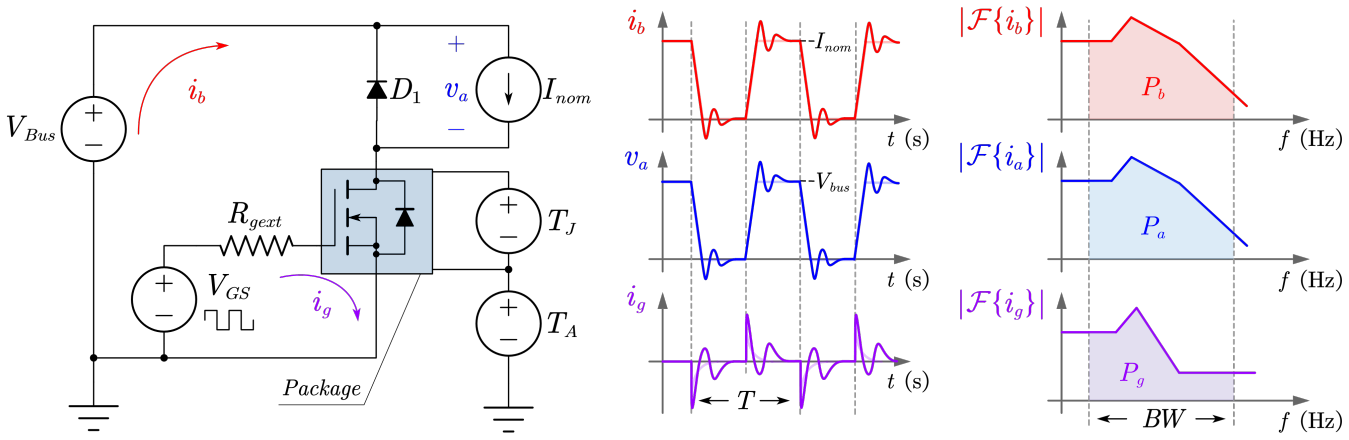

Fig. 3. Calculation of the noise spectrum during the optimization iterations where the device model is simulated in a continuous switching test with all of the 3D effects of the package (both thermal and electromagnetic).

where $|\mathcal{F}\{\cdot\}|$ represents the magnitude of the single-sided spectrum of the signal, and f_{LB} and f_{UB} represent the lower and upper bounds of the frequency band. After computing the baseline power spectrum, the same calculations are repeated at each evaluation of the cost function; however, this time, all of the effects of the package are included in the simulation as shown in Figure 3. The noise term f_N can then be calculated as the sum of the ratios of the spectrum power to the baseline spectrum power as in Eq. 3.

$$f_N = \frac{P_{go}}{P_g} + \frac{P_a}{P_{ao}} + \frac{P_{bo}}{P_b} \tag{3}$$

There are two important points to be made regarding this formulation. First, the summation of the terms in Eq. 3 are summed only to allow for a single-objective cost function. The same can be said for Eq. 1. In practice, these terms could be separated, weighted, or removed for different applications or to use a multi-objective optimization routine. For instance, in applications for motor drivers, high-frequency harmonics on the output node are less important and thus the P_a/P_{ao} term could be eliminated.

Second, the formulation in Eq. 3 serves as an analogue to minimization of impedance. For instance, in the case of P_{go}/P_g, the gate current i_g is inversely proportional to the impedance of the gate loop Z_g when the gate voltage remains constant and thus the power spectrum P_g can be taken to be inversely proportional to Z_g.

$$V_g = i_g Z_g \rightarrow i_g \propto \frac{1}{Z_g} \rightarrow P_g \propto \frac{1}{Z_g} \tag{4}$$

Given Eq. 4, the ratio P_{go}/P_g can be expressed as proportional to the ratio of impedances Z_g and Z_{go}

$$\frac{P_{go}}{P_g} \propto \frac{1/Z_{go}}{1/Z_g} = \frac{Z_g}{Z_{go}} \approx \frac{Z_{go} + Z_{package}}{Z_{go}} \tag{5}$$

where Z_g can be approximately expressed as the sum of the baseline impedances (R_{gext}, R_{gint}, C_{iss}, etc.) and the package stray impedances $Z_{package}$. In this way, minimizing the ratio P_{go}/P_g is analogous to minimizing the package impedance. The difference is that this technique accounts for all of the package impedances across the entire frequency band and quantifies them in a single scalar value.

III. Methodology

A. Software Implementation

The reduced-order, lumped-component simulation tool, parametric 3D modeling, and data post-processing are implemented in C code [8] while the optimization is implemented in MATLAB, as indicated in Figure 4. MATLAB is selected

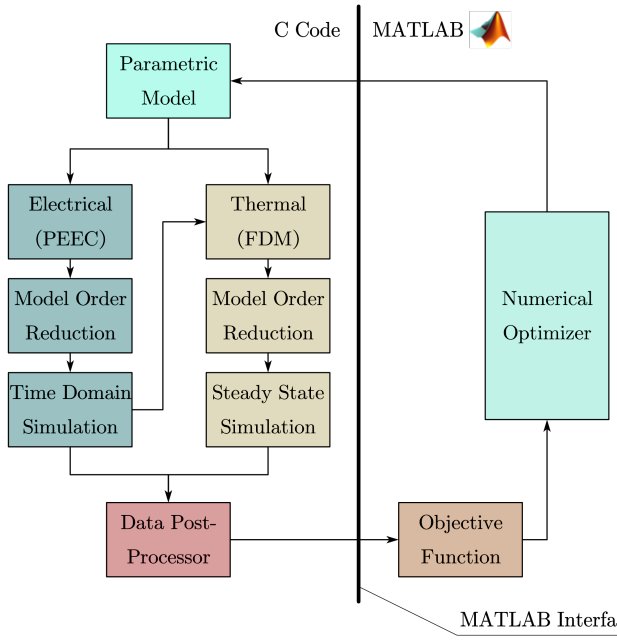

Fig. 4. Software implementation showing the majority of the simulation and modeling components built in C while the optimization components are built in MATLAB.

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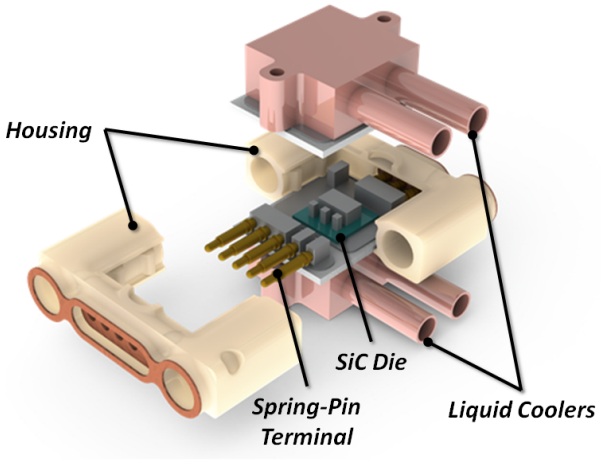

Fig. 5. Discrete 10 kV SiC MOSFET package with double-sided cooling enabled by a wirebond-less molybdenum interconnect and a lateral spring-pin termination.

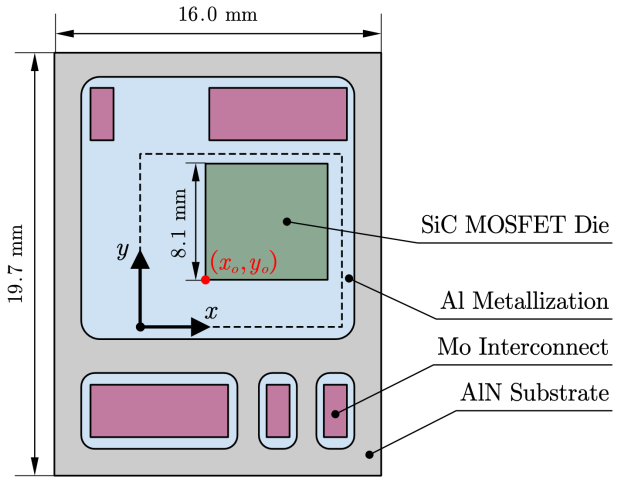

Fig. 7. The optimizable variables (x, y). The black dashed lines indicate the feasible limit for die location and the bound of the optimizable region.

for the optimization component solely because it allows for a rapid-prototyping platform where the cost functions and optimization algorithms can be quickly implemented and modified using builtin tool sets without the time overhead of scratch implementation in C. In practice, all of the cost function and optimization code utilized here could be integrated into the C code base.

B. Package Structure

For the purpose of demonstrating the optimization workflow, the die location of a discrete SiC MOSFET package (Figure 5) was optimized. The module contains a single 3^{rd} generation 10 kV, 25 A SiC MOSFET die and utilizes two aluminum-nitride substrates and a wirebond-less molybdenum interconnect to enable double sided cooling. Figure 6 shows the package during assembly with the upper substrate removed to showcase the wirebond-less interconnects mounted both to the substrate and to the surface of the die.

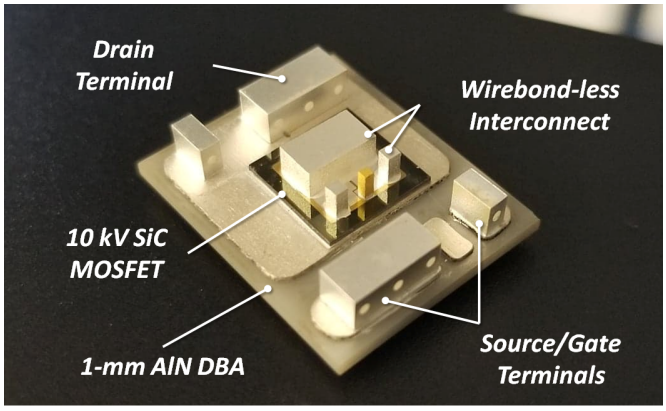

Fig. 6. Package with upper substrate removed to showcase internal geometry and wirebond-less interconnects. Substrate measures 16 x 19.7 mm^2.

For the optimization, there are two degrees of freedom: the lateral X-position and the longitudinal Y-position of the die on the substrate. Figure 7 shows a top-down view of the module with the die location and the coordinate reference frame. The two optimizable variables are x_o and y_o. The total range of the die placement is indicated by the black dashed region. This range of variability in the design provides variation in the both the thermal and electrical performance of the die. As the die moves closer to the edge of the aluminum metallization (large x_o and small y_o), the amount of heat spreading lessons, adversely affecting thermal performance. As the die moves closer to the drain terminal (large y_o) the length of the gate and kelvin traces are adversely affected while the length of the drain and source traces are reduced.

C. Optimization Procedure

For the optimization procedure, a Bayesian optimization technique is selected due to its ability to handle minor noise and non-convexities as a result of variations in the mesh with changes in the geometry [4]. Given the formulation of the cost function and the selected optimization technique, the die location is optimized as shown in Algorithm 1.

IV. Results

To understand the range of variation in performance that occurs over the design range as defined in Figure 7, several studies were conducted. Figure 8 shows the drain-source voltage V_{ds} across the device as the die changes location in the package. Note the device is switched at a bus voltage of 600V, which is significantly lower than the 10 kV rating of the device. Due to the lack of availability of 10 kV device models, a 1.2 kV device model was used in place, requiring the bus voltage to be limited. Four die locations are selected as the four extremes of the design region to understand the extent which the performance varies. The V_{ds} is compared to the baseline waveform (calculated as shown in Figure 3)

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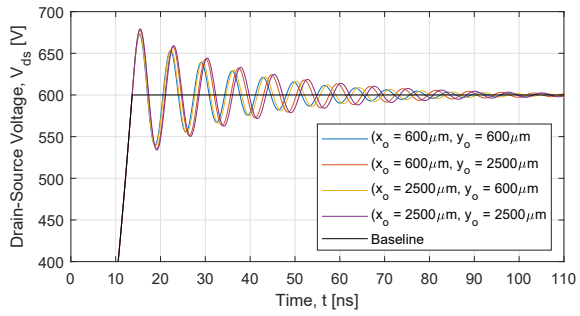
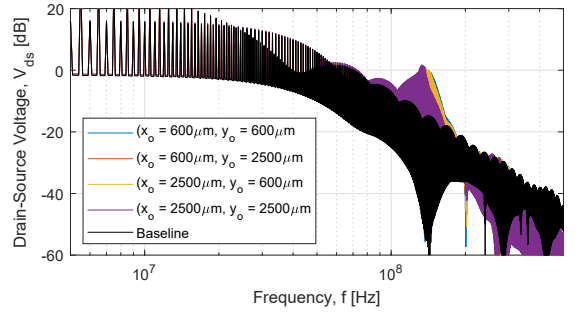


(a)



(b)

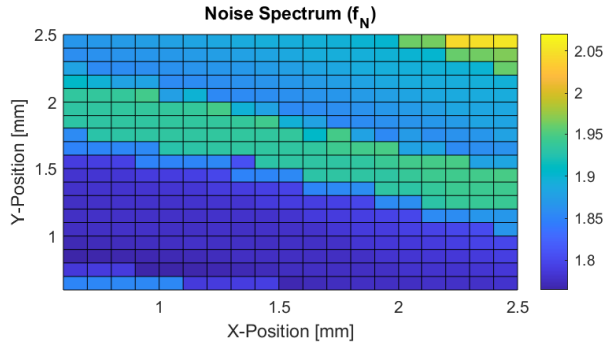
Fig. 8. a) Drain-source voltage across the device evaluated at the baseline, and with the die located at the extremes of the domain; b) the spectral representation of the time-domain waveform showing the high-frequency peaking not present in the baseline.

Algorithm 1: Bayesian Optimization Routine

Simulate baseline circuit (Fig. 2)
Calculate baseline power spectrum (Eq. 2)
procedure BAYESIAN OPTIMIZATION
  Evaluate $f(x_i, y_i)$ for initial training set
  Locate minimum with acquisition function
  Update training set
procedure COST FUNCTION EVALUATION
  Update parametric model with (x_i, y_i)
  Mesh geometry
  Compute PEEC and FDM matrices
  Apply model order reduction (MOR)
  Simulate coupled electromagnetic/thermal (Fig. 3)
  Calculate power spectrum (Eq. 2)
  Evaluate noise term f_N (Eq. 3)
  Evaluate objective function $f(x_i, y_i)$ (Eq. 1)

both in the time and spectral domain. As anticipated, the low frequency peaks in the spectral domain are not present in the baseline V_{ds} due to the lack of resonance caused by package parasitics.

Next, the objective function is evaluated over the entire design domain on a grid of 100 µm in order to assess the shape of each component of the objective function, f_N, f_T, and f_E. Figure 9 shows the shape of each objective function



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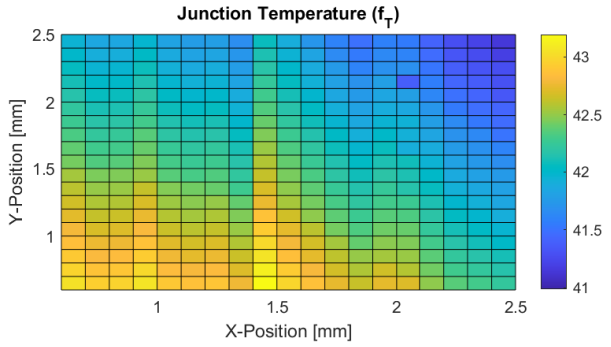

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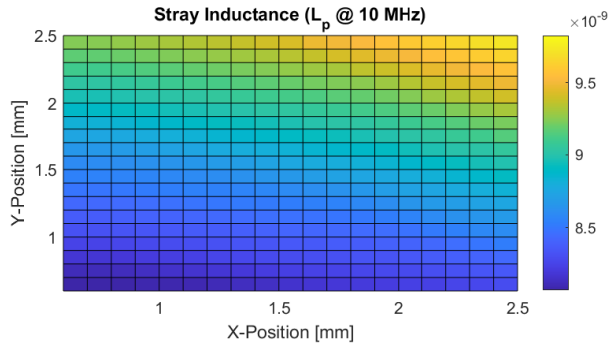
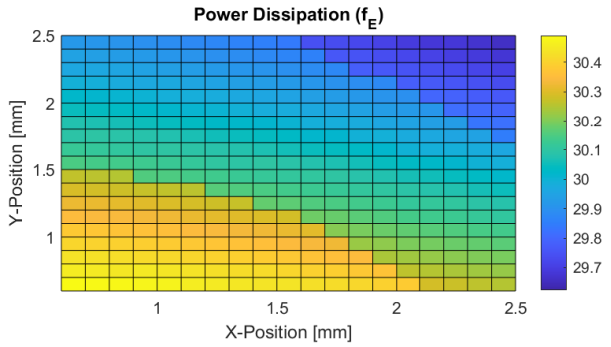


(c)



(d)

Fig. 9. The a) noise spectrum term f_N, b) lifetime term f_T, c) stray inductance L_p, and d) efficiency term f_E evaluated over the entire design range as defined in Figure 7.

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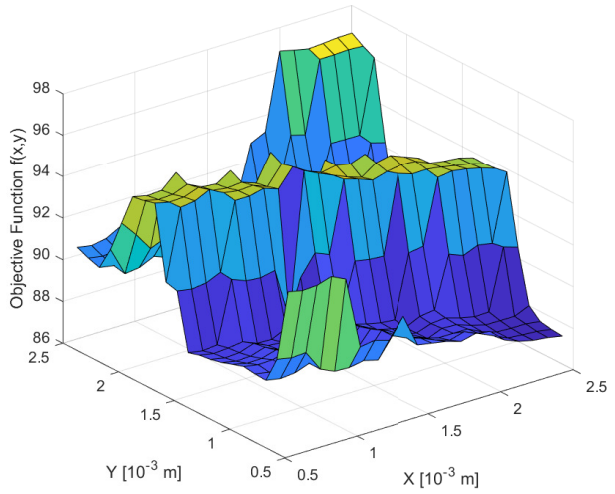

Fig. 10. Cost function as defined in Eq. 1 evaluated over the entire range of die location to illustrate the shape of the domain and the minor non-convexities stemming from the re-meshing of the geometry.

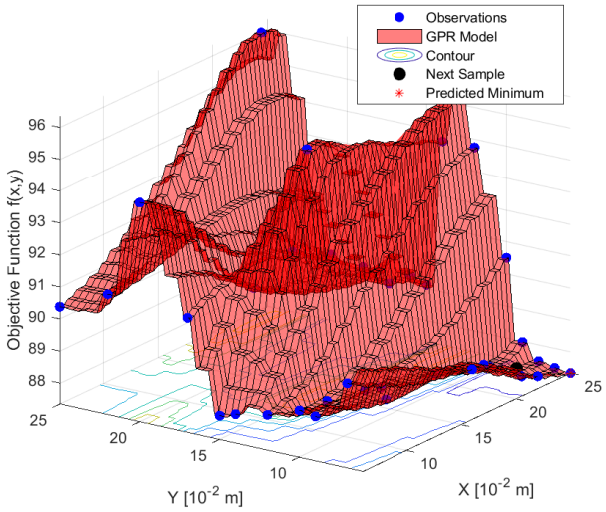

Fig. 11. The result of the Bayesian optimization procedure showing the Gaussian process model fit to the observations of the cost function, as well as the predicted minimum of the domain.

component as well as the stray commutation loop inductance evaluated at 10 MHz. Stray inductance L_p is included in this study to illustrate any variation between the proposed noise term and the more traditional impedance minimization term L_p. The PEEC model results in a full-bandwidth 3D magnetic field model that couples with the equivalent circuit components and does not readily produce a lump equivalent circuit element such as stray inductance. The effective stray inductance for the package was extracted from the PEEC model via a separate post processing routine. Note that while the shape of the f_N and L_p domains vary, they roughly predict the same minimum, located in the lower left-hand corner of the plot.

Figure 10 shows the shape of the objective function when it is assembled using the individual components from Figure 9 per Eq. 1. The plot shows the shape of the objective function which has two trenches, suggesting that classical descent-based techniques will have a sensitivity to starting point and should be avoided when optimizing this structure. The plot also shows some shallow non-convexities that stem from the re-meshing of the part geometry.

Figure 11 shows the result of the optimization of the package where a Bayesian optimization process was used with the proposed cost function. The plot shows the Gaussian process model that was fitted to the data for the purpose of the optimization. Note the shape of the model closely follows that of the actual domain as shown in Figure 10.

The purpose of this implementation is to demonstrate the speed and efficiency with which such an optimization can be completed using the proposed reduced-order lumped-component analysis. On a desktop computer with an i9 4.1 GHz, 8-core processor and 128GB of RAM, each iteration of the optimizer, which includes the parametric model generation, meshing, model construction, MOR, and as well as the steady-state thermal simulation and time-domain electrical simulation (10 µs duration, with 100k time-steps), takes under 15 minutes. The entire optimization process takes approximately eight hours to converge to a minimum.

V. Conclusion

In summary, the high performance of next-generation WBG devices come with demanding packaging needs that result in tight-coupled packages, where effects of the electrical, thermal, and mechanical physics are intertwined and interdependent. This requires a new generation of design tool that can efficiently compute the multi-physics and multi-domain performance of the package and provide deeper insights into how the package will perform in the physical world. This work proposes a multi-physics numerical optimization workflow for power electronics packages which utilizes a reduced-order, lumped component analysis with behavior circuit models to efficiently model the multi-domain performance of a 10 kV SiC MOSFET package in a continuous switching test. A cost function was proposed which utilized the multi-domain simulation result to optimize device lifetime, device efficiency, and conducted noise emissions. The result is a streamlined, multi-physics design workflow suitable for numerical optimization.

Future work includes additional studies on the cost function, and specifically to the noise term f_N, to better understand the underlying mechanisms that result in a discrepancy between the shape of the noise term and the shape of the more traditional stray impedance term. Other tasks include testing the optimization on more complicated packages, with additional degrees of freedom and a wider design range to allow for more variation in performance over which to optimize.

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